EXPERIMENT NUMBER 8

Phase Locked Loop (PLL)

AIM: To study IC 565 PLL and find the following parameters.

1. Lock Range
2. Capture Range.

LEARNING OBJECTIVE:

- To compare the two modes of operation of timer IC 555.
- To classify the types of pulse modulation.

PRIOR CONCEPTS: Types of Modulation, Amplitude modulation, Pulse modulation and Sampling Theorem.

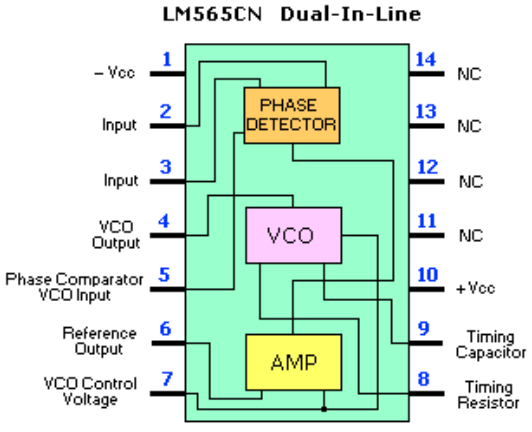
EQUIPMENT REQUIRED

Equipment	Range	Quantity
CRO	(0-20)MHz	1
Function Generator	(0-1)MHz	1
Experiment Kit		1
Dual Power Supply	(0-30)V	1

COMPONENTS REQUIRED

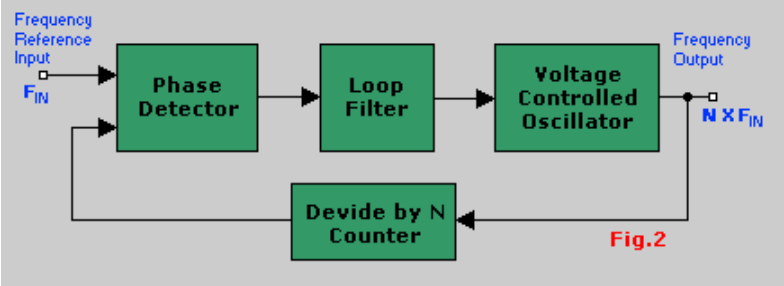
Components	Value	Quantity
IC	IC 565	1
Capacitor	0.01μF	3
	1μF	1
Resistor	6.8KΩ	1

THEORY: Phase-locked loop (PLL) is a feedback loop which locks two waveforms with same frequency but shifted in phase. The fundamental use of this loop is in comparing frequencies of two waveforms and then adjusting the frequency of the waveform in the loop to equal the input waveform frequency. The heart of the PLL is a phase comparator which along with a voltage controlled oscillator (VCO), a filter and an amplifier forms the loop. If the two frequencies are different the output of the phase comparator varies and changes the input to the VCO to make its output frequency equal to the input waveform frequency. The locking of the two frequencies is a nonlinear process but linear approximation can be used to analyse PLL dynamics. The range over which the loop system will follow changes in the input frequency is called the *lock range*. On the other hand, the frequency range in which the loop acquires phase-lock is the *capture range, and is never greater than the lock range.*



The LM565 is a general purpose Phase-Locked Loop IC containing a stable, highly linear voltage controlled oscillator (VCO) for low distortion FM demodulation, and a double balanced phase detector with good carrier suppression. The VCO frequency is set with an external resistor and capacitor, and a tuning range of 10:1 can be obtained with the same capacitor. The characteristics of the closed loop system--bandwidth, response speed, capture and pull in range--may be adjusted over a wide range with an external resistor and capacitor. The loop

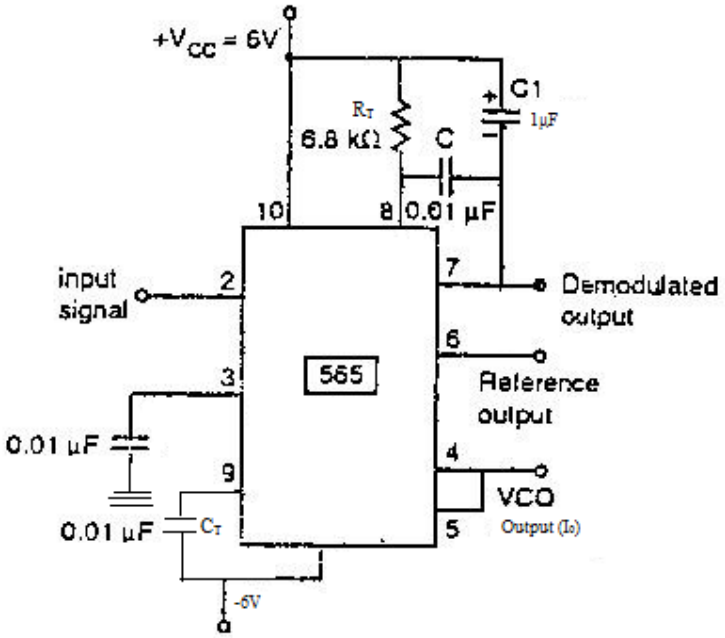
may be broken between the VCO and the phase detector for insertion of a digital frequency divider to obtain frequency multiplication.

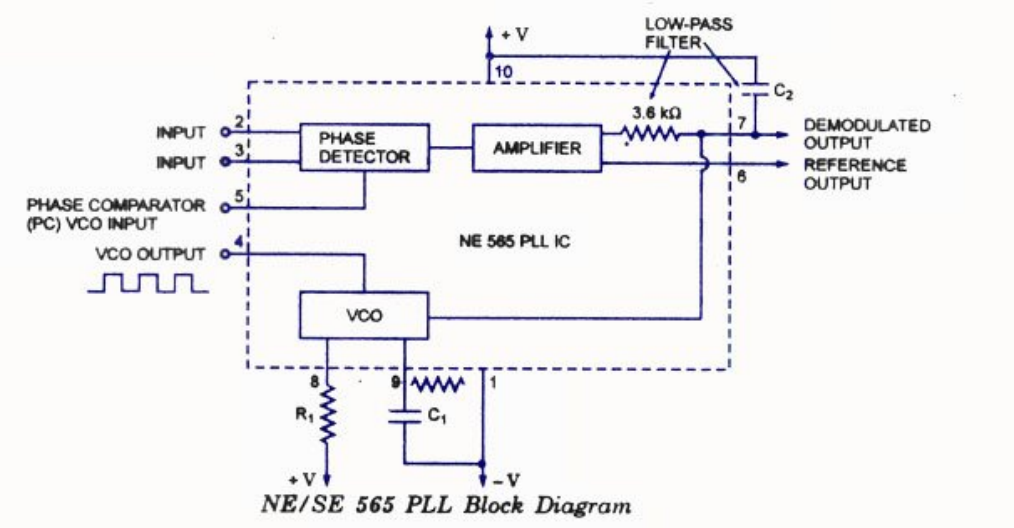


PROCEDURE:

1. Connections are made as shown in the circuit diagram.
2. Measure the free running frequency of IC565 at pin 4 using display with the input signal (say 0V) from the function generator or by shorting pin 2 to ground.
3. Set the input signal say 1V, 1 KHz to pin no. 2 using function generator and observe the corresponding waveform.
4. The frequency is varied till the output signal is 180˚ out of phase with the input. This is the upper end of the lock range.
5. The frequency is reduced till the output is 90˚ out of phase with the input. This is the upper end of the capture range.
6. The frequency is varied till a 90˚ phase shift is obtained in the output with reference to the input once again. This is the lower end of the capture range.
7. As the frequency is decreased further, output goes to 180˚ out of phase with the input once again. This is the lower end of the lock range.
8. The lock range $\Delta f_L = (f_2\text{-}f_1)$
   The capture range $\Delta f_C = (f_3\text{-}f_1)$
9. Compare these values with the theoretical values.

Circuit Diagram





NE/SE 565 PLL Block Diagram

CIRCUIT DESCRIPTION:

- Operating frequency range of the IC: 0.001 Hz to 500 kHz.
- Operating voltage range: ± 6 to ± 12 V.
- Input level required for tracking: 10 mV_{rms} minimum to 3 V peak-to-peak maximum.

As shown in the figure, the PLL system consists of a phase detector or comparator (PC), a voltage-controlled oscillator (VCO), an amplifier and R-C combination forming low-pass filter circuit. The input signals are fed to the phase detector through pins 2 and 3 in differential mode. The input signals can be direct-coupled provided that the dc level at these two pins is made same and dc resistances seen from pins 2 and 3 are equal. By shorting pins 4 and 5 output of VCO is supplied back to the phase comparator (PC). The output of PC is internally connected to amplifier, the output of which is available at pins 6 and 7 through a resistor of 3.6 k Q connected internally. A capacitor C_2 connected between pins 7 and 10 forms a low-pass filter with 3.6 k Q resistor. The filter capacitor C_2 should be large enough so as to eliminate the variations in demodulated output and stabilize the VCO frequency. Voltage available at pin 7 is connected internally to VCO as a control signal. At pin 6 a reference voltage nominally equal to voltage at pin 7 is available allowing both the differential stages to be biased. Pins 1 and 10 are supply pins.
The centre frequency of the PLL is determined by the free-running frequency of the VCO which is given as

$$\mathbf{f_{OUT} = 1.2/4R_tC_t\ Hertz}$$

where R_t and C_t are external resistor and capacitor connected to pins 8 and 9 respectively, as illustrated in figure. The free-running frequency F_{out} of the VCO is adjusted, externally with R_t and C_t, to be at the centre of the input frequency range. Resistor R_t must have a value between 2 and 20 kilo ohm. Capacitor C_t may have any value.
The lock-range of PLL is given as

$$\mathbf{\Delta f_L = \pm 8f_{OUT} / V\ Hertz}$$

where f_{OUT} is free-running frequency of VCO in Hz and V = (+ V) – (- V) and
The capture range is given as

$$\mathbf{\Delta f_C = \pm [\Delta f_L / 2\pi\ (3.6)\ (10)^3\ C]^{1/2}}$$

The lock range usually increases with an increase in input voltage but falls with an increase in supply voltages.

Graphical Relationship between f_{OUT}, f_C and f_L