Praajna Baragur

pgbaragu@uwaterloo.ca | www.linkedin.com/in/praajna | +1 437-985-8358

Education

University of Waterloo September 2021 – April 2026
Bachelor of Applied Science (B.A.Sc.), Honours Computer Engineering *Waterloo, ON*

- **Academics**: Excellent Academic Standing; Term Distinction
- **Relevant Courses**: Systems Programming & Concurrency, Digital Hardware Systems, Compilers, Distributed Computing, Computer Architecture, On-Chip Interconnect, Robot Dynamics & Control
- **Scholarships**: President's Scholarship of Distinction, International Student Entrance Scholarship

Technical Skills

Languages: Python, C, C++, Verilog, Golang, Java, Tcl, Bash, SQL, VHDL, MATLAB
Tools/Technologies: Git/GitLab, Kubernetes, GCP, Docker, Jenkins, ROS/ROS2, EDA Tools

Experience

Infrastructure Engineering Intern - Resiliency September 2025 – Present
Shopify *Toronto, ON*

- Streamlined **Grafana k6** load testing by automating **K8s** secret creation & cleanup, & enabling in-UI configuration & logging in LitmusChaos (**Go/React**), cutting test & debug time by **90%**.
- Developed & refined CPU saturation alerting through incident investigation & **IMOC** shadowing, cutting false positives by **60%** after deployment & improving early detection of performance bottlenecks across services.

Software Engineering Intern February 2025 – April 2025
German Aerospace Center (DLR) *Stuttgart, Germany*

- Led research project to convert **Dymola** & **Simulink** models into Functional Mockup Units (**FMUs**) & automate runs with **Python/FMPy**, enabling portable, tool-agnostic co-simulation.
- Prototyped a simulation framework with automated **energy, power, state of charge, & thermal checks** to validate FMUs against original models, catching simulation anomalies early, & reducing validation time by **35%**.

Infrastructure Engineering Intern (EDA/Chip Design) September 2023 – September 2024
Groq *Toronto, ON (Remote)*

- Developed **CDC & RDC** verification flow, identifying **100+** bugs, critical for on-time tapeout of Groq's chip.
- **Interim Infra HW lead** (2 months): resolved critical cross-team issues; retired **3+ year** legacy flow to deploy a fast, reliable, & deterministic build system; played a key role in HW/SW **monorepo** transition.
- Optimized **Verilog Lint** runtime by **5x** via caching & parallelism; integrated with GitLab **CI/CD**.
- Integrated design constraints (**SDC**) validation, transforming **hours** of manual validation **to seconds**.
- Automated lint waiver creation & improved **Nix**-based RTL filelist creation (**Haskell**); cut **90%** manual work.

Undergraduate Research Assistant May 2023 – Dec 2023
Autonomous Vehicle Research & Intelligence Lab (University of Waterloo) *Waterloo, ON*

- Integrated Velodyne **VLS-128 LIDAR** for point-cloud mapping, enabling autonomous navigation in a Jeep.
- Leveraged **Python** & **ROS2** to seamlessly integrate real-time NMEA **GPS data**, optimizing vehicle localization.
- Engineering & deployed a **YOLOX**-powered **ROS2** node for precise vision based obstacle detection in the vehicle.

ASIC Design Verification Intern May 2022 – September 2022
Groq *Mountain View, CA (Remote)*

- Parallelized build compilations with multi-threading, increased compilation speed **5x** per regression test.
- Improved slurm license management using **Python**, resulting in **2.5x** improvement in regression speed.
- Implemented **Jinja** templates to reduce configuration file sizes by over **90%**, accelerating test preparation.

Projects

Natural Language-Controlled Robot Arm | *Dobot Magician, Python, OpenCV, NumPy, LLM APIs* July 2025

- Implemented a multimodal robot control stack in **Python** that couples a **vision LLM API** for object localization with a **language LLM API** that emits validated robot arm command sequences.
- Calibrated camera-to-robot with **ArUco** and pixel-to-robot SE(3), achieving approx. **89%** pick-and-place success rate with **2–5 mm** placement accuracy.