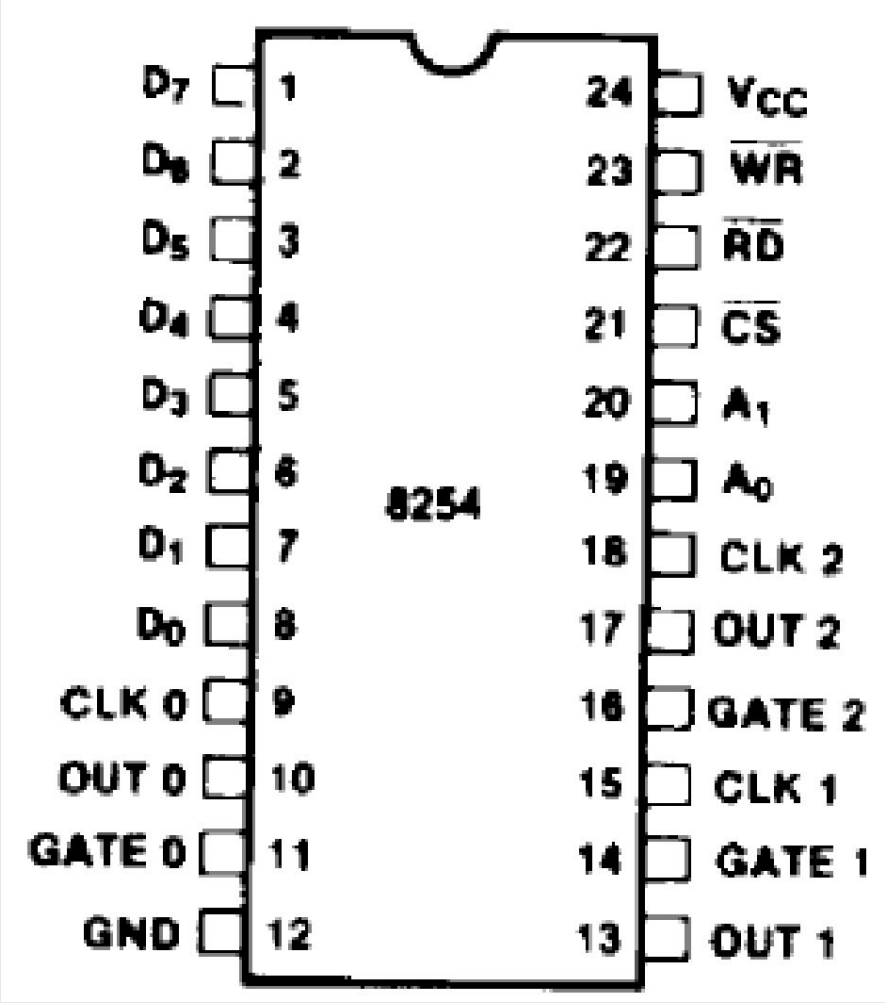
Programmable Interval Timer - 8254

Features

- Three Independent 16-Bit Counters,
- Clock input upto 10 MHz,
- Status Read-Back Command,
- Six Programmable Counter Modes,
- Binary or BCD Counting,
- Single +5V Supply

Pin Diagram


D7 1
D6 2
D5 3
D4 4
D3 5
D2 6
D1 7
D0 8
CLK 0 9
OUT 0 10
GATE 0 11
GND 12
8254
24 VCC
23 WR
22 RD
21 CS
20 A1
19 A0
18 CLK 2
17 OUT 2
16 GATE 2
15 CLK 1
14 GATE 1
13 OUT 1

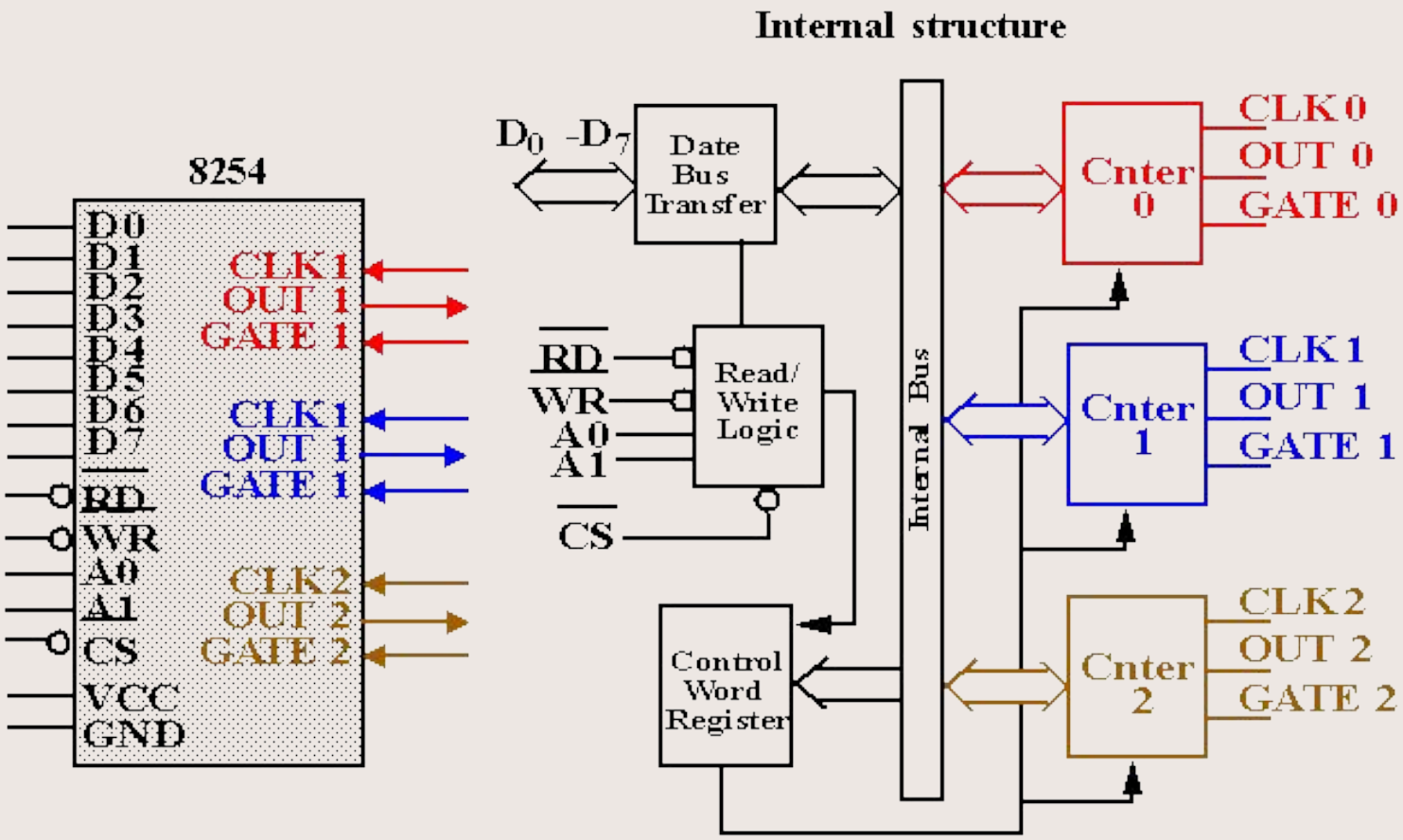
Pin Description

Symbol	Pin No.	Type	Name and Function
D_7–D_0	1–8	I/O	**DATA:** Bi-directional three state data bus lines, connected to system data bus.
CLK 0	9	I	**CLOCK 0:** Clock input of Counter 0.
OUT 0	10	O	**OUTPUT 0:** Output of Counter 0.
GATE 0	11	I	**GATE 0:** Gate input of Counter 0.
GND	12		**GROUND:** Power supply connection.
V_{CC}	24		**POWER:** +5V power supply connection.
$\overline{WR}$	23	I	**WRITE CONTROL:** This input is low during CPU write operations.
$\overline{RD}$	22	I	**READ CONTROL:** This input is low during CPU read operations.
$\overline{CS}$	21	I	**CHIP SELECT:** A low on this input enables the 8254 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
A_1, A_0	20–19	I	**ADDRESS:** Used to select one of the three Counters or the Control Word Register for read or write operations. Normally connected to the system address bus.

A_1	A_0	Selects
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register

CLK 2	18	I	**CLOCK 2:** Clock input of Counter 2.
OUT 2	17	O	**OUT 2:** Output of Counter 2.
GATE 2	16	I	**GATE 2:** Gate input of Counter 2.
CLK 1	15	I	**CLOCK 1:** Clock input of Counter 1.
GATE 1	14	I	**GATE 1:** Gate input of Counter 1.
OUT 1	13	O	**OUT 1:** Output of Counter 1.

Block Diagram of 8254



Internal Blocks of Counter

- **Count Register (CR) to store count (CR_L & CR_M),**
- **Counting elements (CE) are used for counting,**
- **Output Latch (OL_L & OL_M) to latch the count in CE,**
- **The Control Word Register is not part of the Counter itself, but its contents determine how the Counter operates.**
- **The status register, when latched, contains the current contents of the Control Word Register and status of the output and null count flag.**

Internal Block Diagram

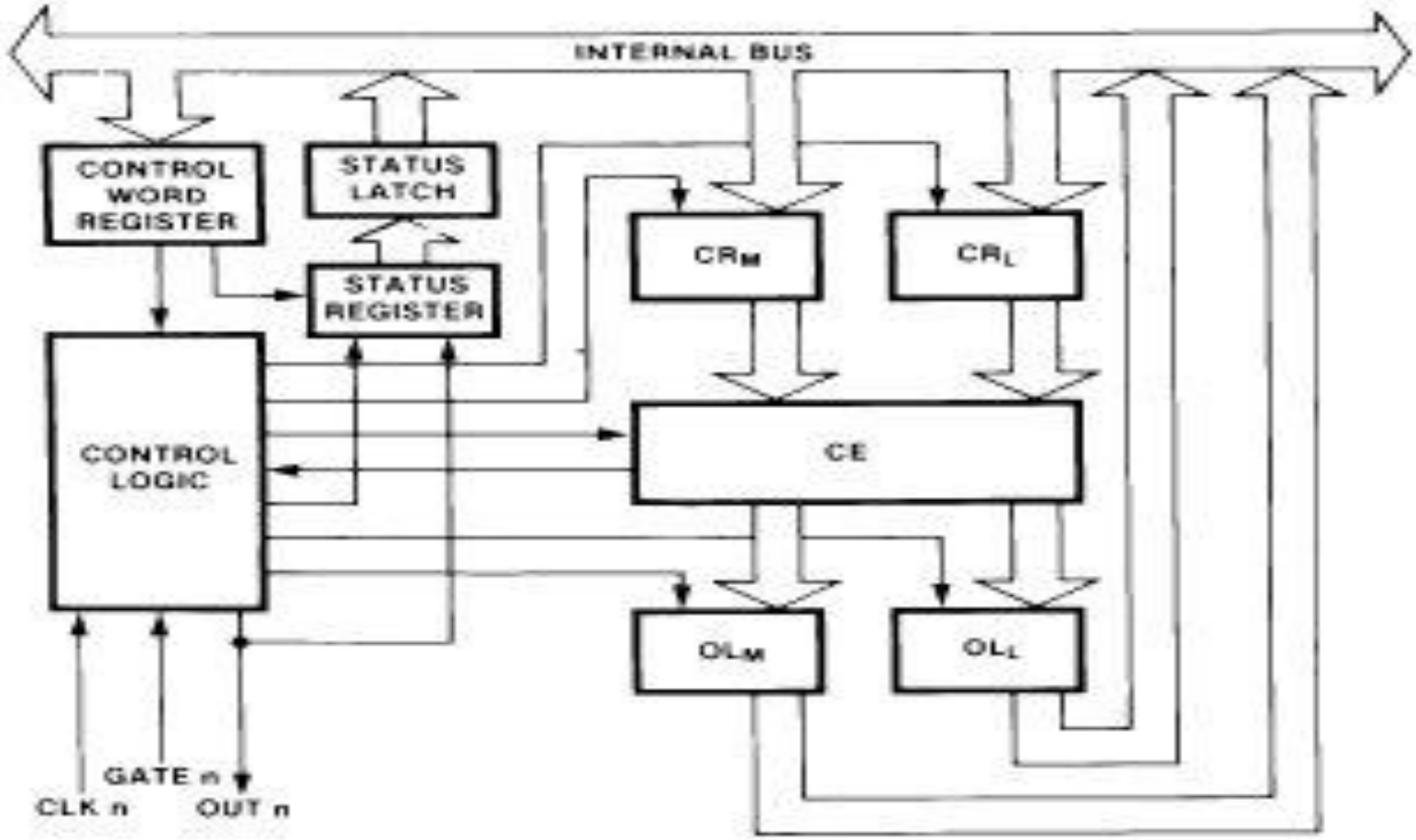


Figure 5. Internal Block Diagram of a Counter

System Interface

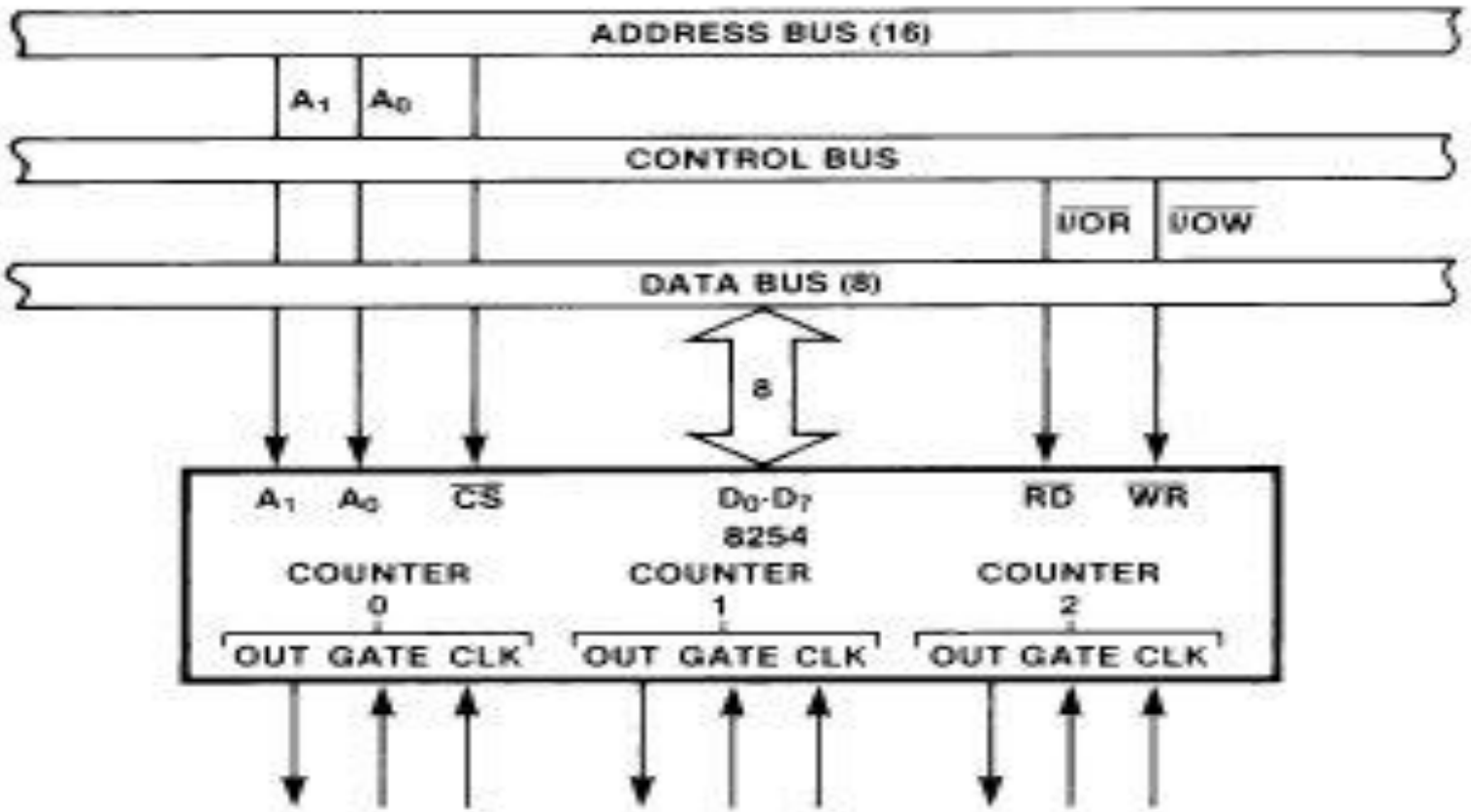
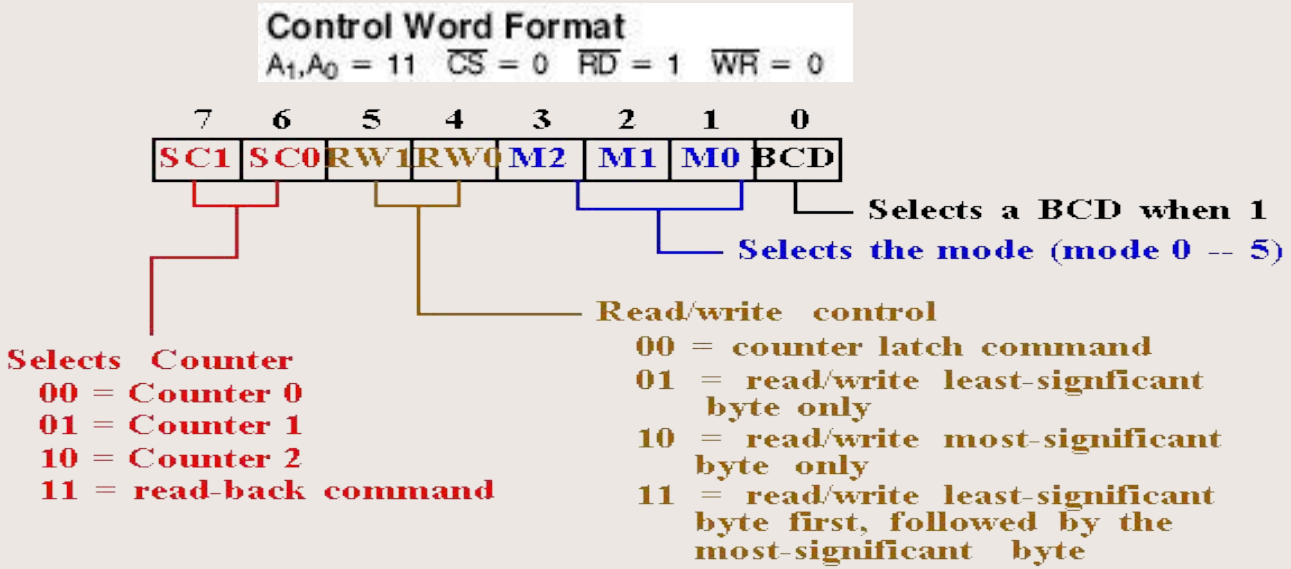


Figure 6. 8254 System Interface

Control Word format



8254 Programming

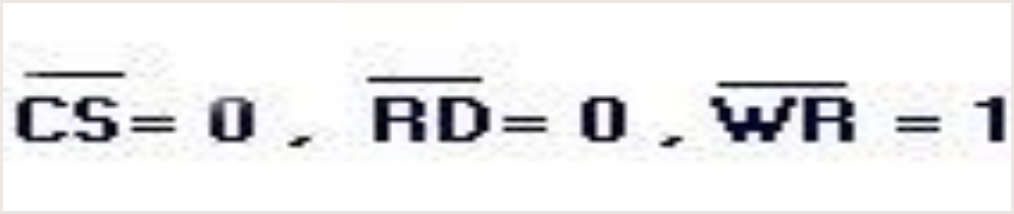
- Each counter is individually programmed by writing a control word, followed by the initial count.
- The control word allows the programmer to select the counter, mode of operation, binary or BCD count and type of operation (read/write).

WRITE Operation

$\overline{CS} = 0 \quad \overline{RD} = 1 \quad \overline{WR} = 0$

- Control Word to Control register
- Initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

READ Operation



Three Possible Methods to read counters

- Simple Read Operation,
- Counter Latch Command,
- Read Back Command.

Note: Two I/O read operations have to be performed to get first Lower Byte and then higher byte of count.

Simple Read Operation:

After inhibiting counter using GATE or CLK input we can read count

Counter Latch Command:

$A_1, A_0 = 11$; CS = 0; RD = 1; WR = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	0	0	X	X	X	X

D5 D4 = 0 0 Designates the counter latch command

SC1 SC2 = Specify counter to be latched.

X – Don't care bits must be 0 to ensure compatibility with future Intel products.

Read Back Command:

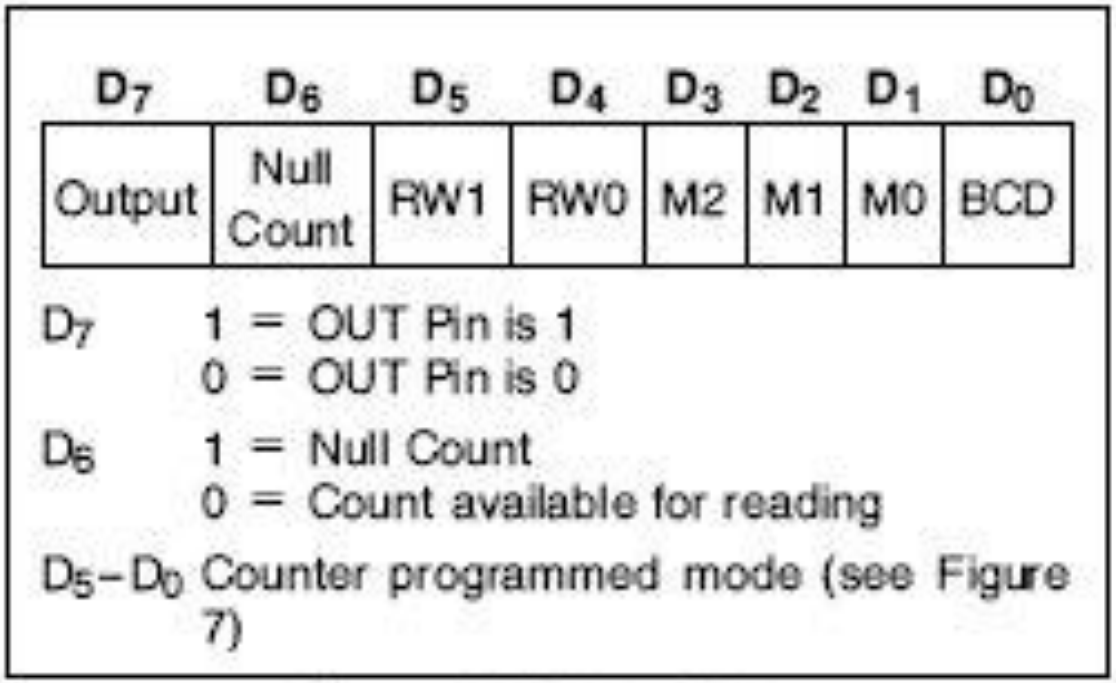
A0, A1 = 11 $\overline{CS}$ = 0 $\overline{RD}$ = 1 $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	$\overline{COUNT}$	$\overline{STATUS}$	CNT 2	CNT 1	CNT 0	0

D_5: 0 – Latch count of selected counter(s)
D_4: 0 – Latch status of selected counters(s)
D_3: 1 – Select Counter 2
D_2: 1 – Select Counter 1
D_1: 1 – Select Counter 0
D_0: Reserved for future expansion; Must be 0

Figure 10. Read-Back Command Format

Status Byte



D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Output	Null Count	RW1	RW0	M2	M1	M0	BCD

D_7 1 = OUT Pin is 1
0 = OUT Pin is 0

D_6 1 = Null Count
0 = Count available for reading

D_5–D_0 Counter programmed mode (see Figure 7)

Figure 11. Status Byte

Read-back command example

Command								Description	Result
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	1	0	0	0	0	1	0	Read back count and status of Counter 0	Count and status latched for Counter 0
1	1	1	0	0	1	0	0	Read back status of Counter 1	Status latched for Counter 1
1	1	1	0	1	1	0	0	Read back status of Counters 2, 1	Status latched for Counter 2, but not Counter 1
1	1	0	1	1	0	0	0	Read back count of Counter 2	Count latched for Counter 2
1	1	0	0	0	1	0	0	Read back count and status of Counter 1	Count latched for Counter 1, but not status
1	1	1	0	0	0	1	0	Read back status of Counter 1	Command ignored, status already latched for Counter 1

Interleaved Read and Write Operations:

Valid sequence for read and write of the same counter set for two byte count:

1. Read least significant byte,
2. Write new least significant byte,
3. Read most significant byte,
4. Write new most significant byte.

Modes of 8254

Six Different Modes

- Mode 0: Interrupt On Terminal Count
- Mode 1: Hardware Retriggerable One-shot
- Mode 2: Rate Generator
- Mode 3: Square Wave Mode
- Mode 4: Software Triggered Strobe
- Mode 5: Hardware Triggered Strobe (Retriggerable)

Applications of 8254

- Real time clock
- Event-counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

References

- Microprocessors and Interfacing by Douglas V. Hall, TMH Publication.
- Intel 8254 data sheet (www.datasheetcatalog.com)