Inspiring Excellence

CSE460

VLSI Design

Lab Assignment : 02

Submitted By

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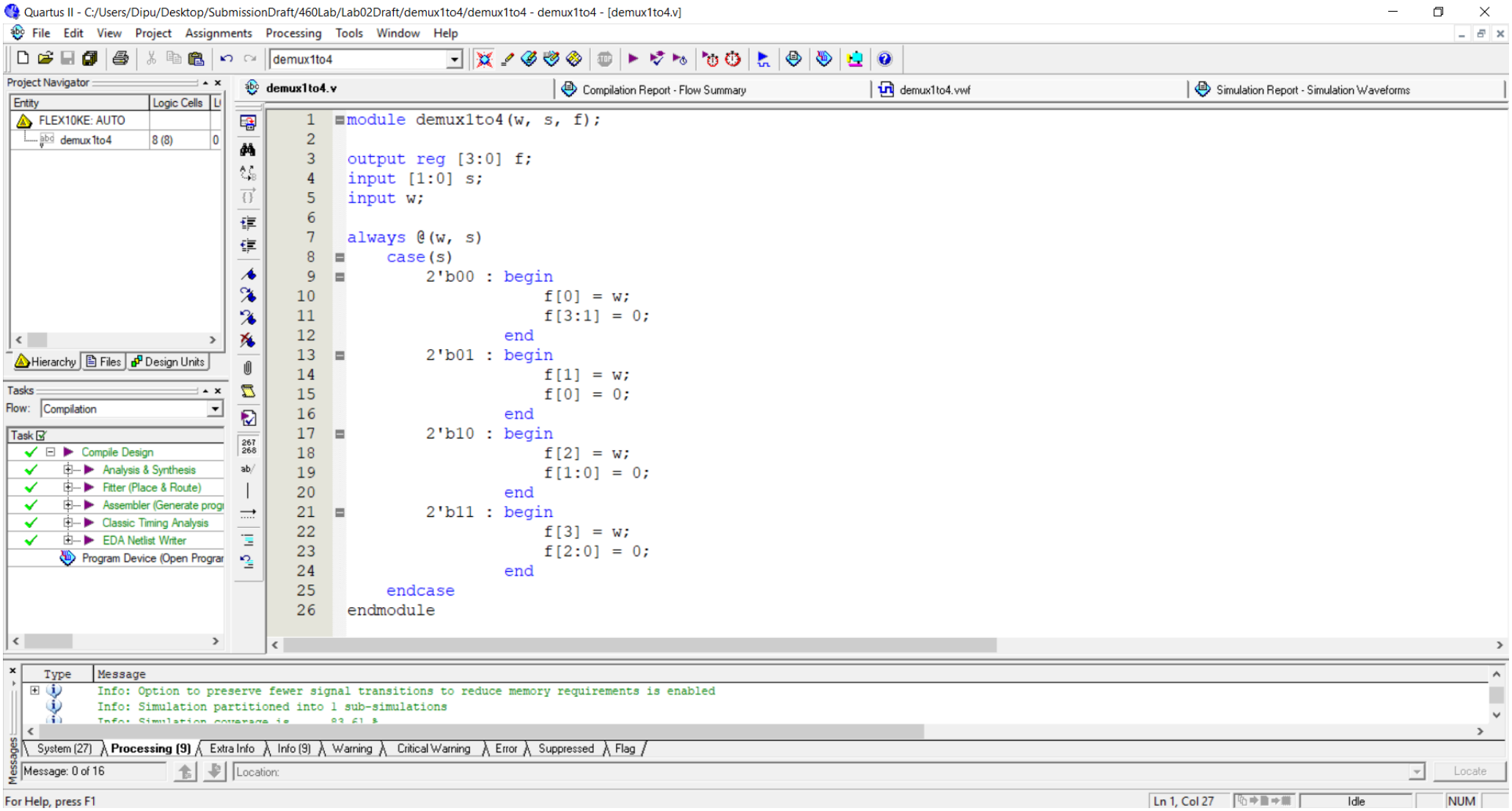
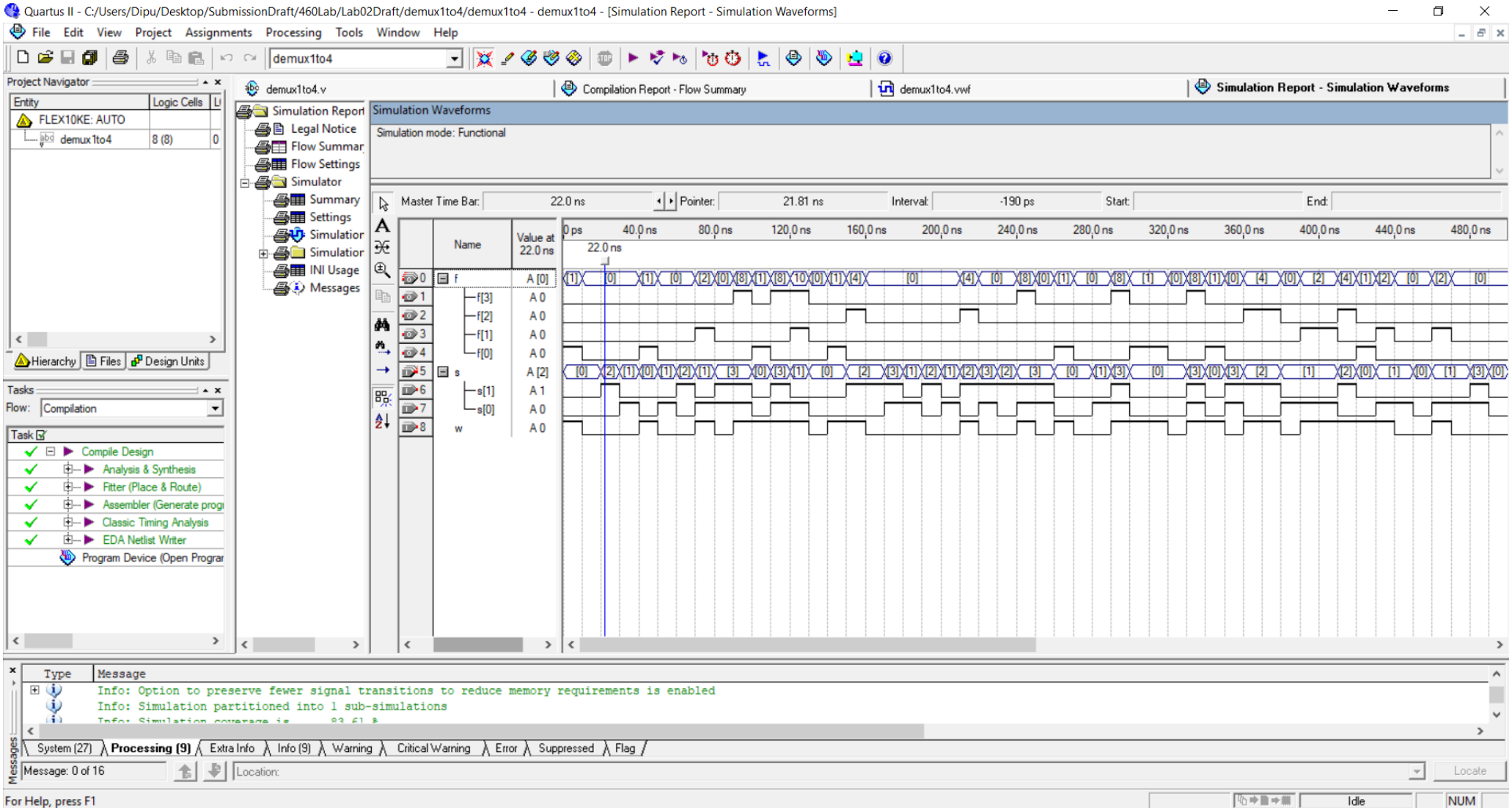
Lab Assignment 02

Home Work 01 Verilog Code



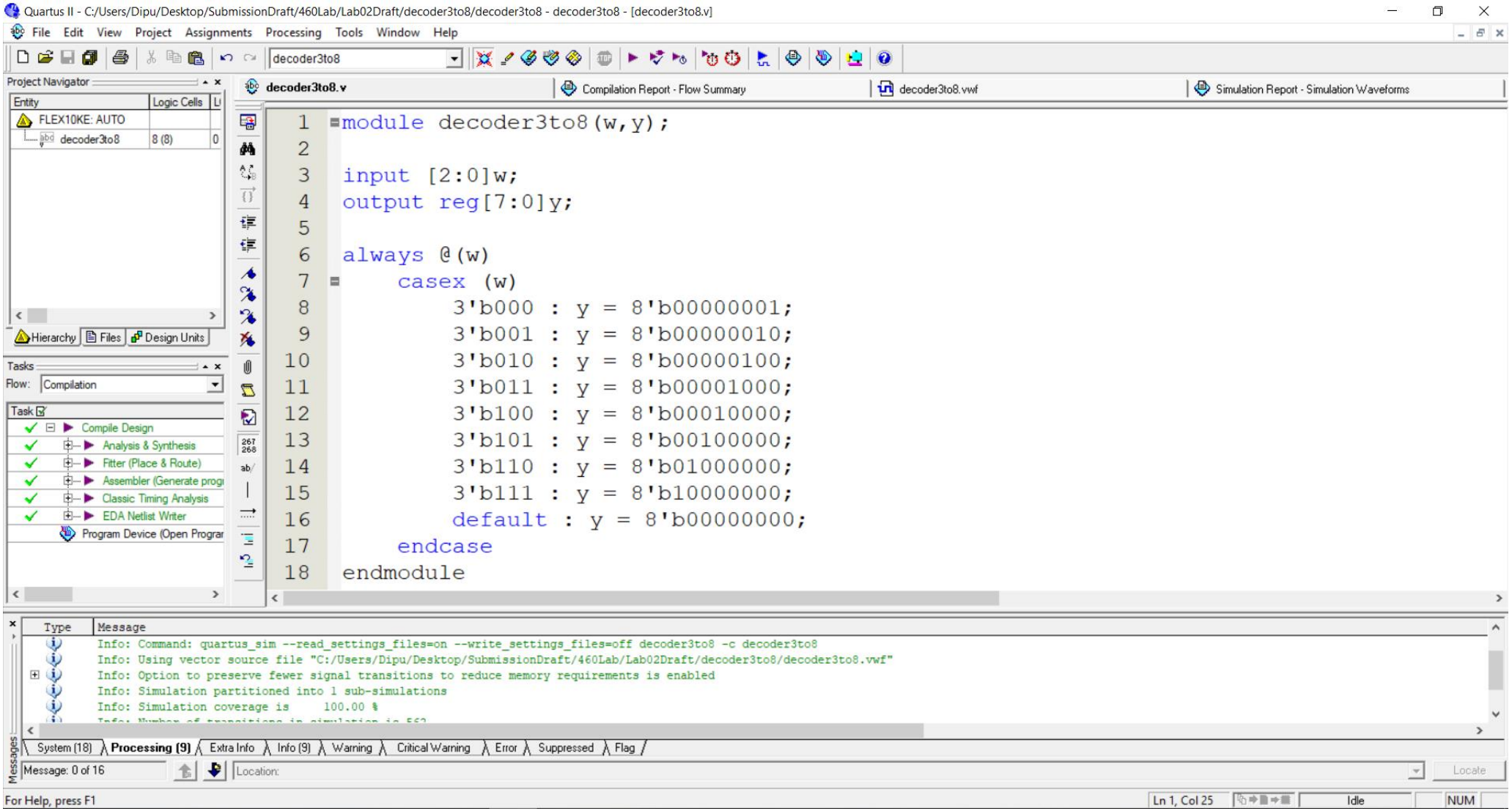
Home Work 01 Vector Waveform



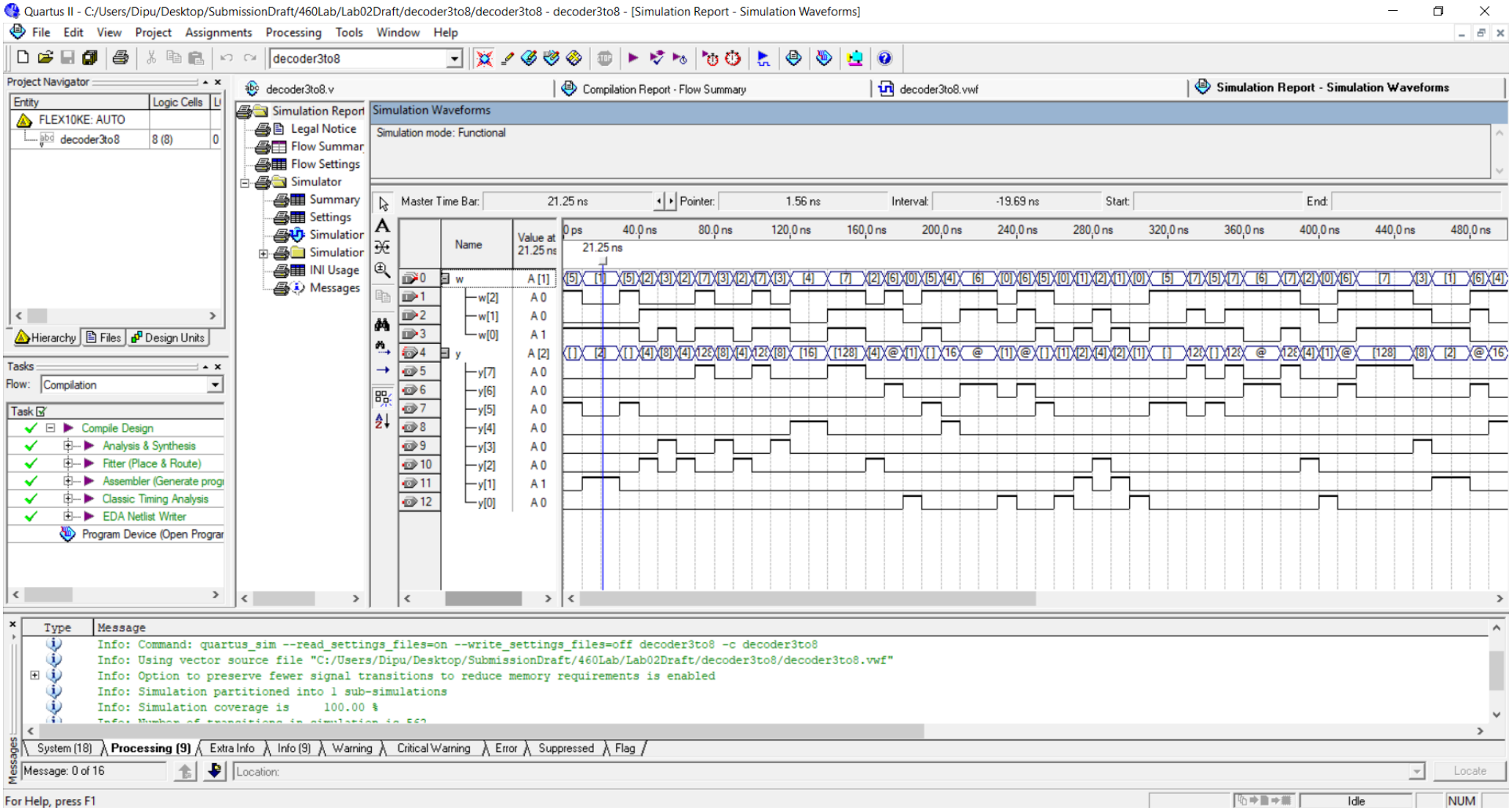
Home Work 01 Discussion

It is a 1 to 4 DEMUX. It takes an 1 bit input, w and 2 bit input, s which is selector and provides a 4 bit output, f. Depending on the combination of selector, it provides 1 output among 4 available options.

Home Work 02 Verilog Code



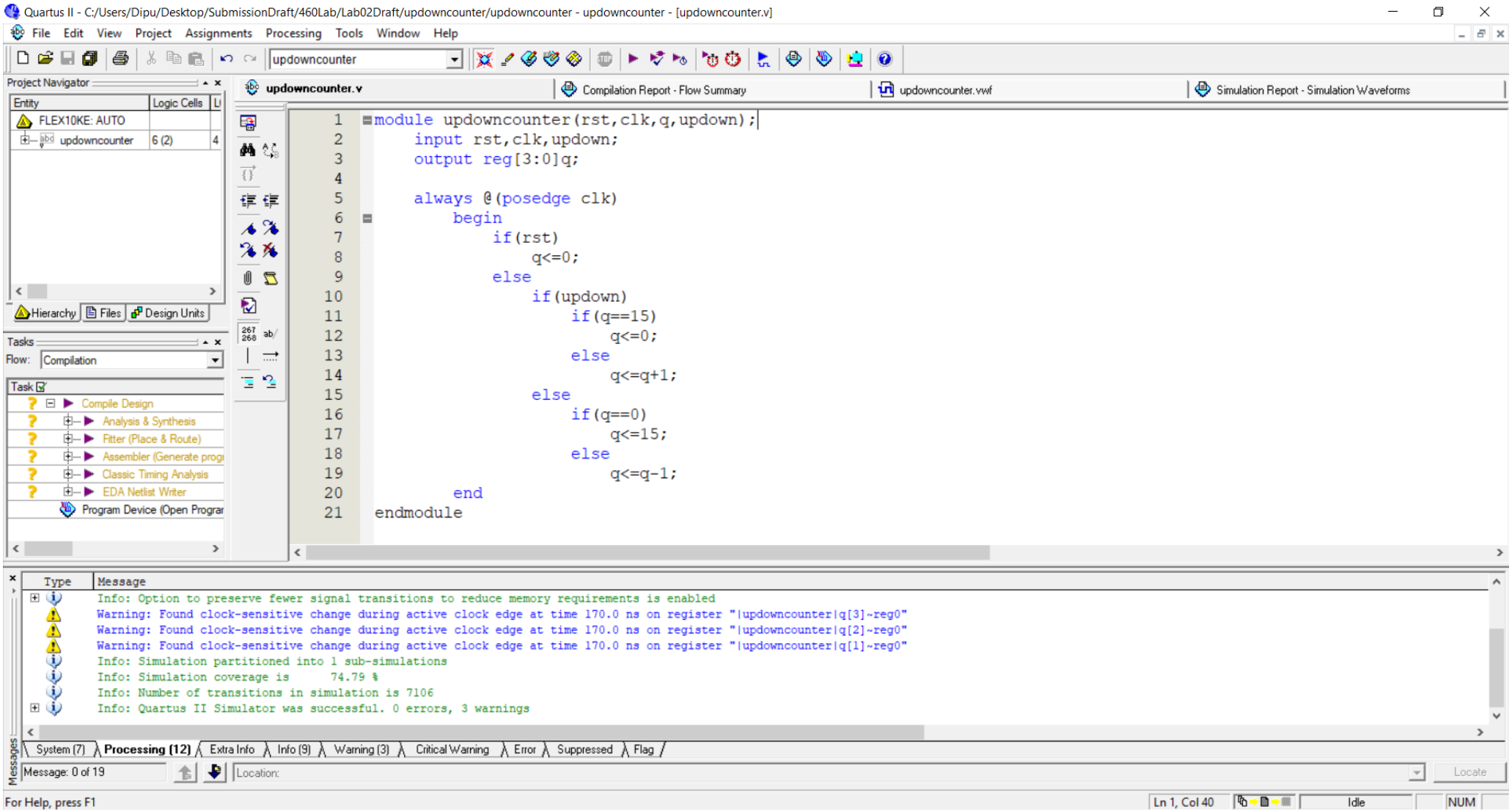
Home Work 02 Vector Waveform



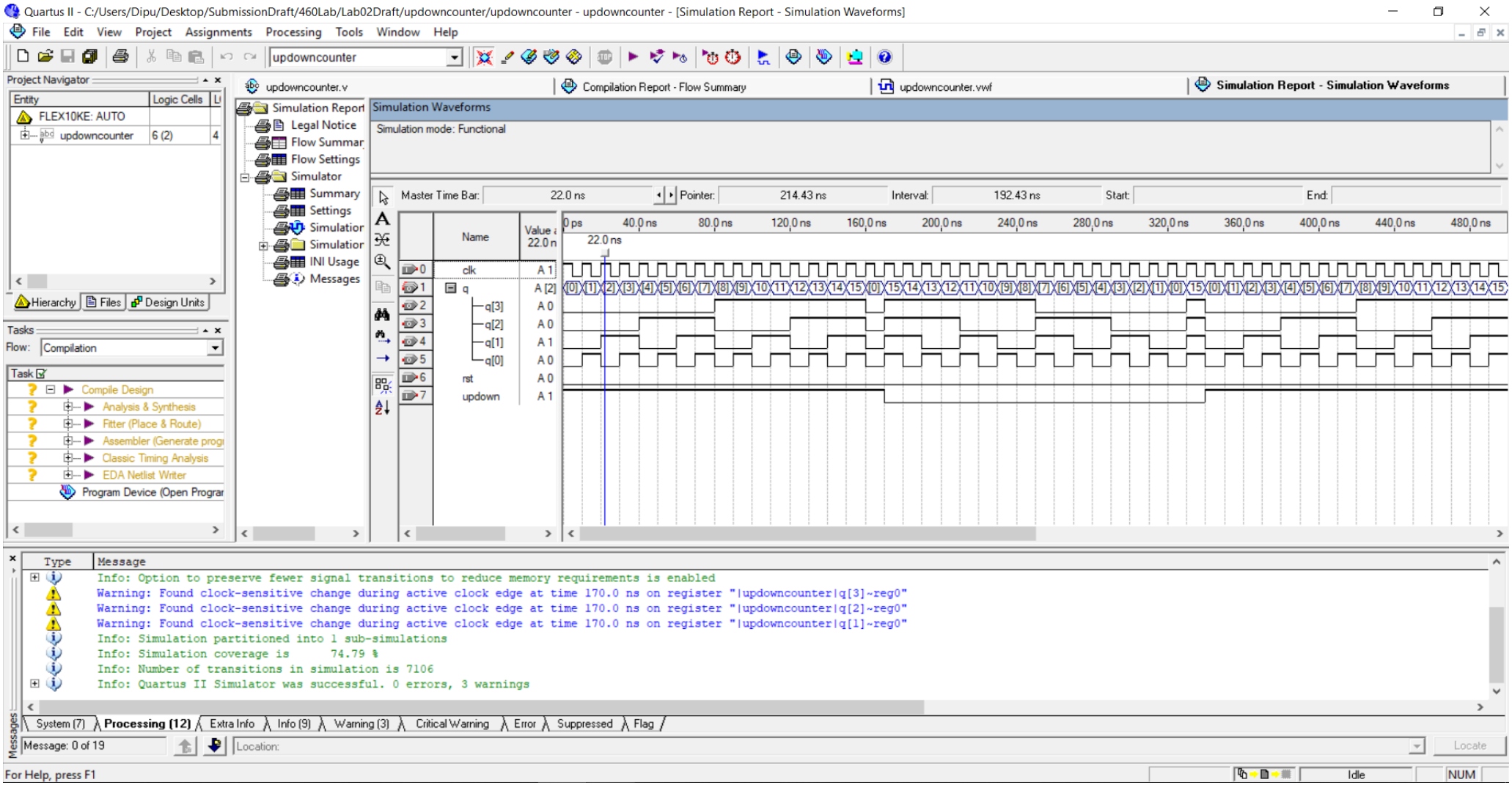
Home Work 02 Discussion

It is a 3 to 8 decoder. It takes 3 bits input w and provides an output which have 8 bits. Depending on the combinations of 3 bits input w, it provides a single output represented in 8 bits.

Home Work 03 Verilog Code



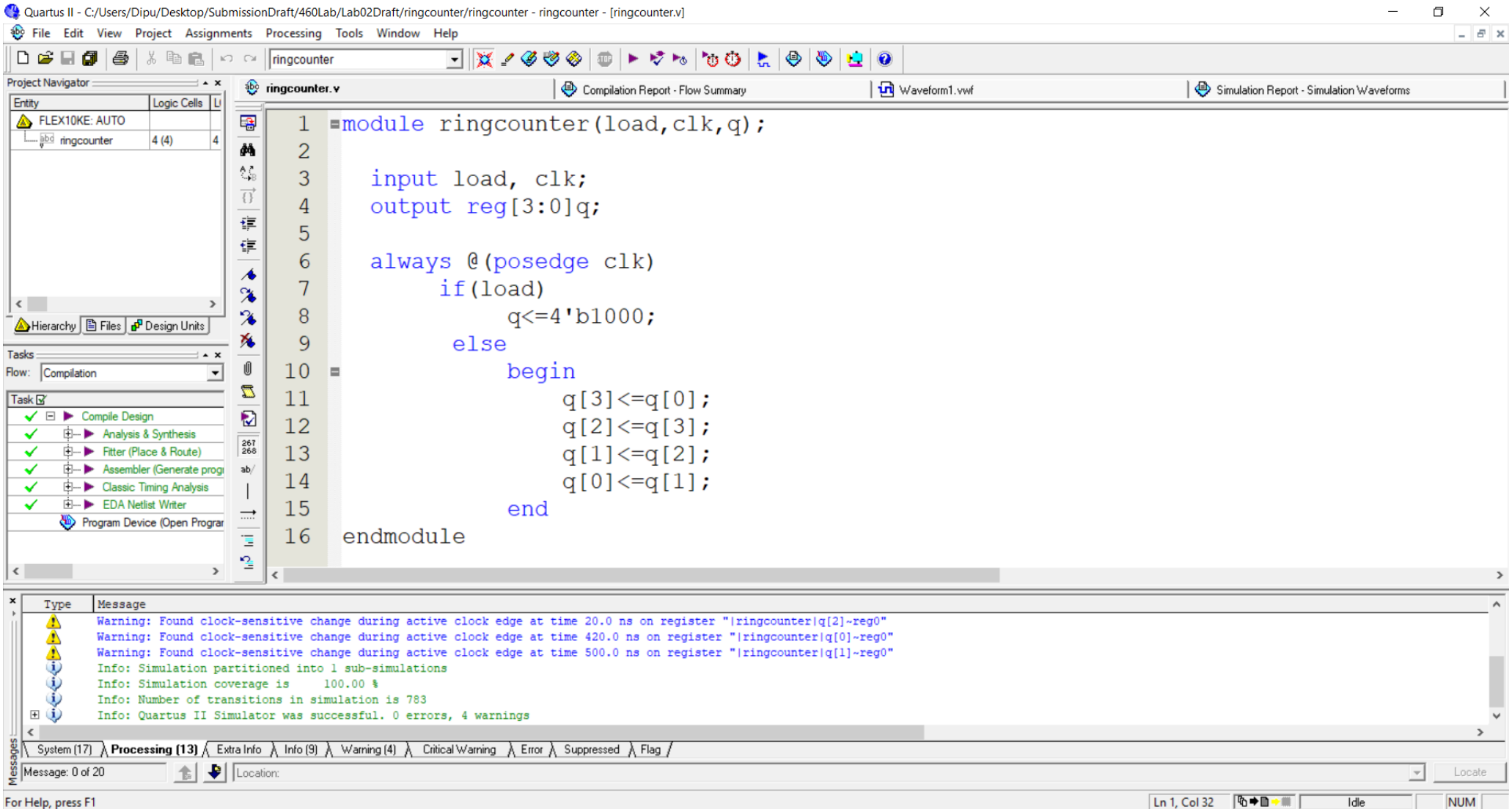
Home Work 03 Vector Waveform



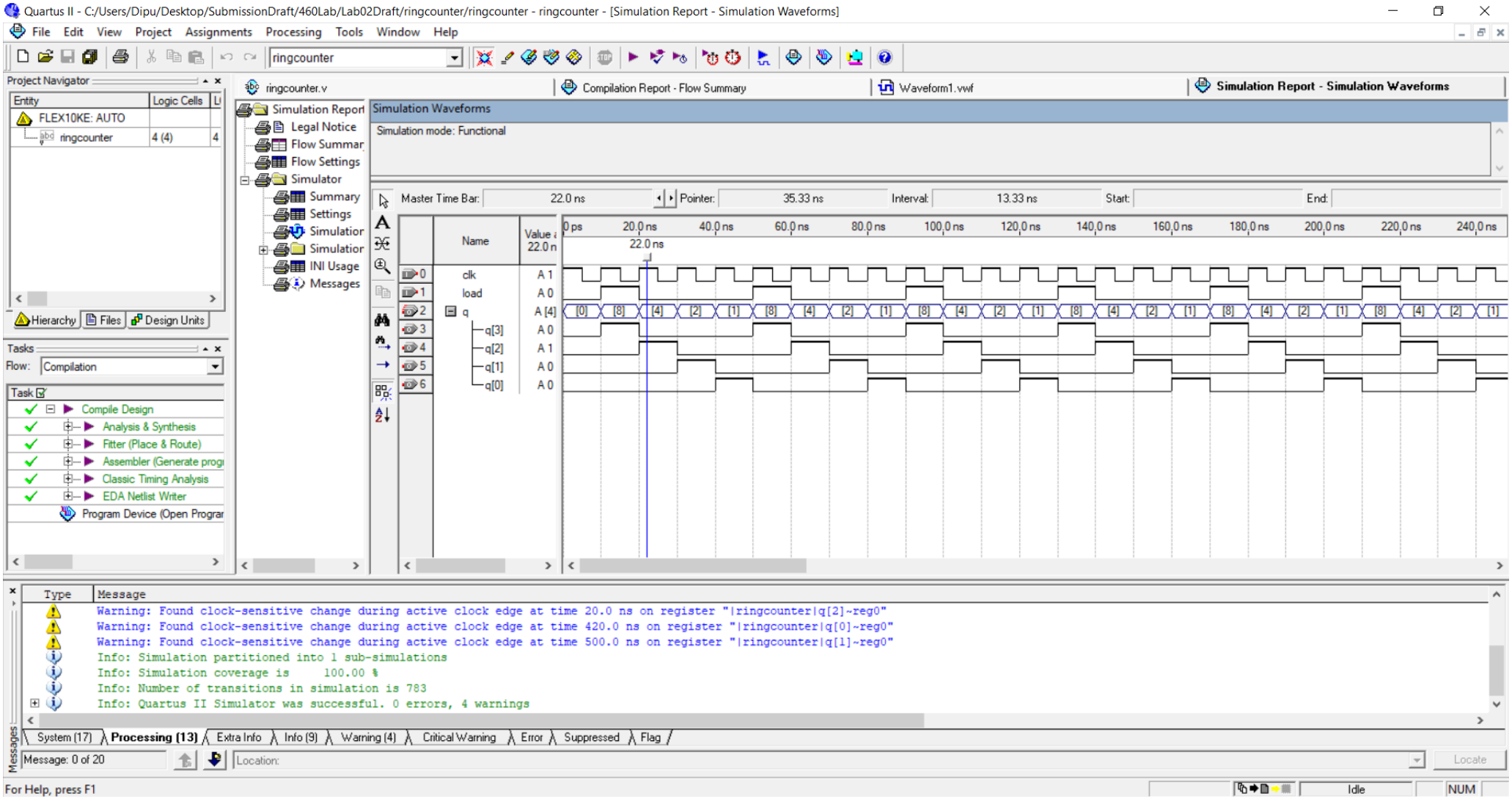
Home Work 03 Discussion

It is an Up Down Counter. When we provide input value 1 for 'updown' it works as Up Counter. It counts from 0 to 15 & again 0 to 15 till updown=1. When we provide input value 0 for 'updown' it works as Down Counter, counts from 15 to 0 & again 15 to 0 till updown=0. To reset the counter we will have to provide rst=1.

Home Work 04 Verilog Code



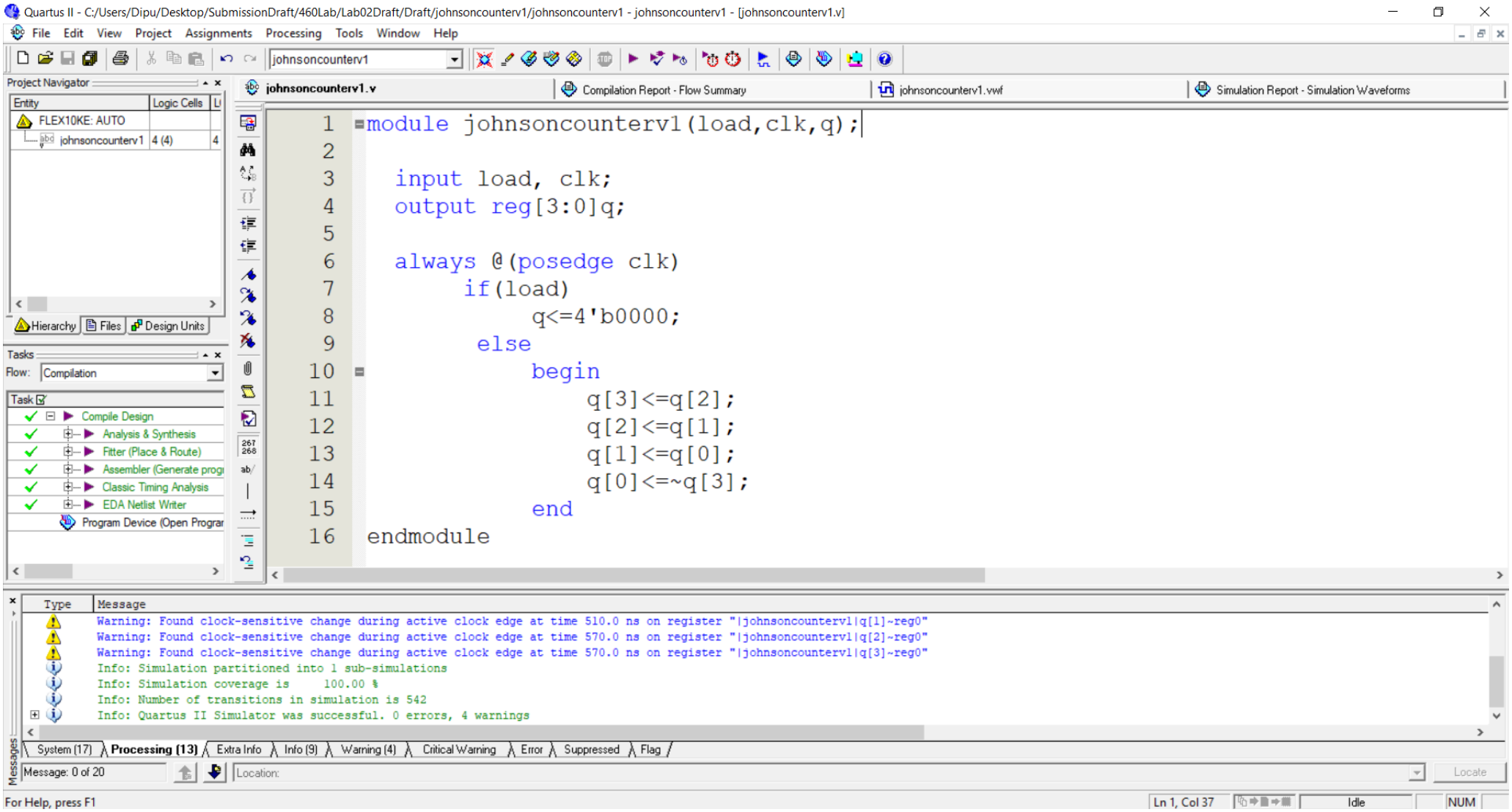
Home Work 04 Vector Waveform



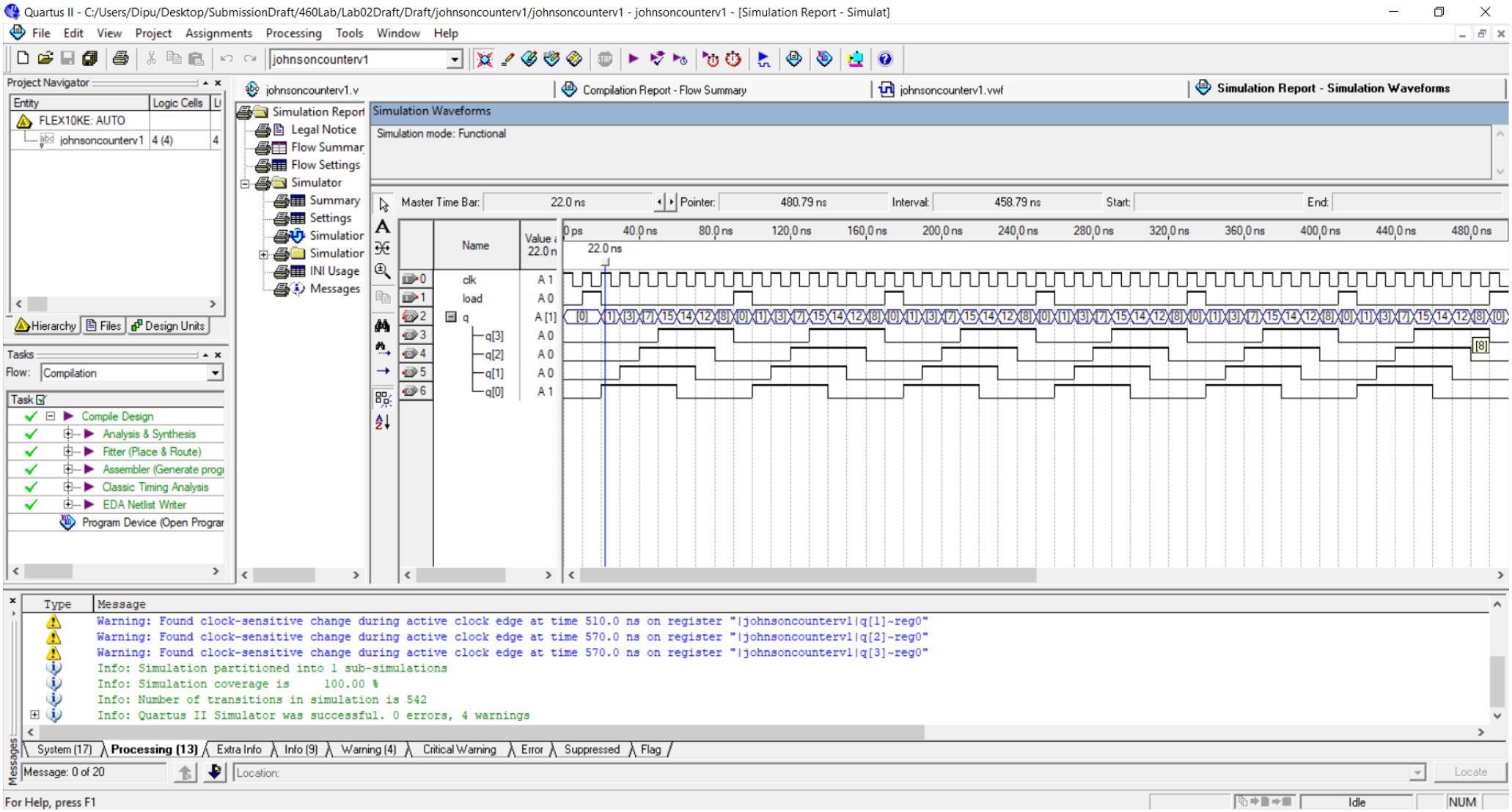
Home Work 04 Discussion

It is a Ring Counter. A straight ring counter, also known as a one-hot counter, connects the output of the last shift register to the first shift register input and circulates a single one (or zero) bit around the ring. When load will be high & Clock Pulse will have Positive Edge, 1000(8) will be loaded and then the next values will be 0100(4), 0010(2), 0001(1), 1000(8),.....

Home Work 05 Verilog Code



Home Work 05 Vector Waveform



Home Work 05 Discussion

It is a Johnson Counter. A twisted ring counter which connects the complement of the output of the last shift register to the input of the first register and circulates a stream of ones followed by zeros around the ring. When load will be high & Clock Pulse will have Positive Edge, 0000(0) will be loaded and then the next values will be 0001(1), 0011(3), 0111(7), 1111(15), 1110(14), 1100(12), 1000(8), 0000(0), 0001(1),.....