CSE460

VLSI Design

Lab Assignment : 03

Submitted By

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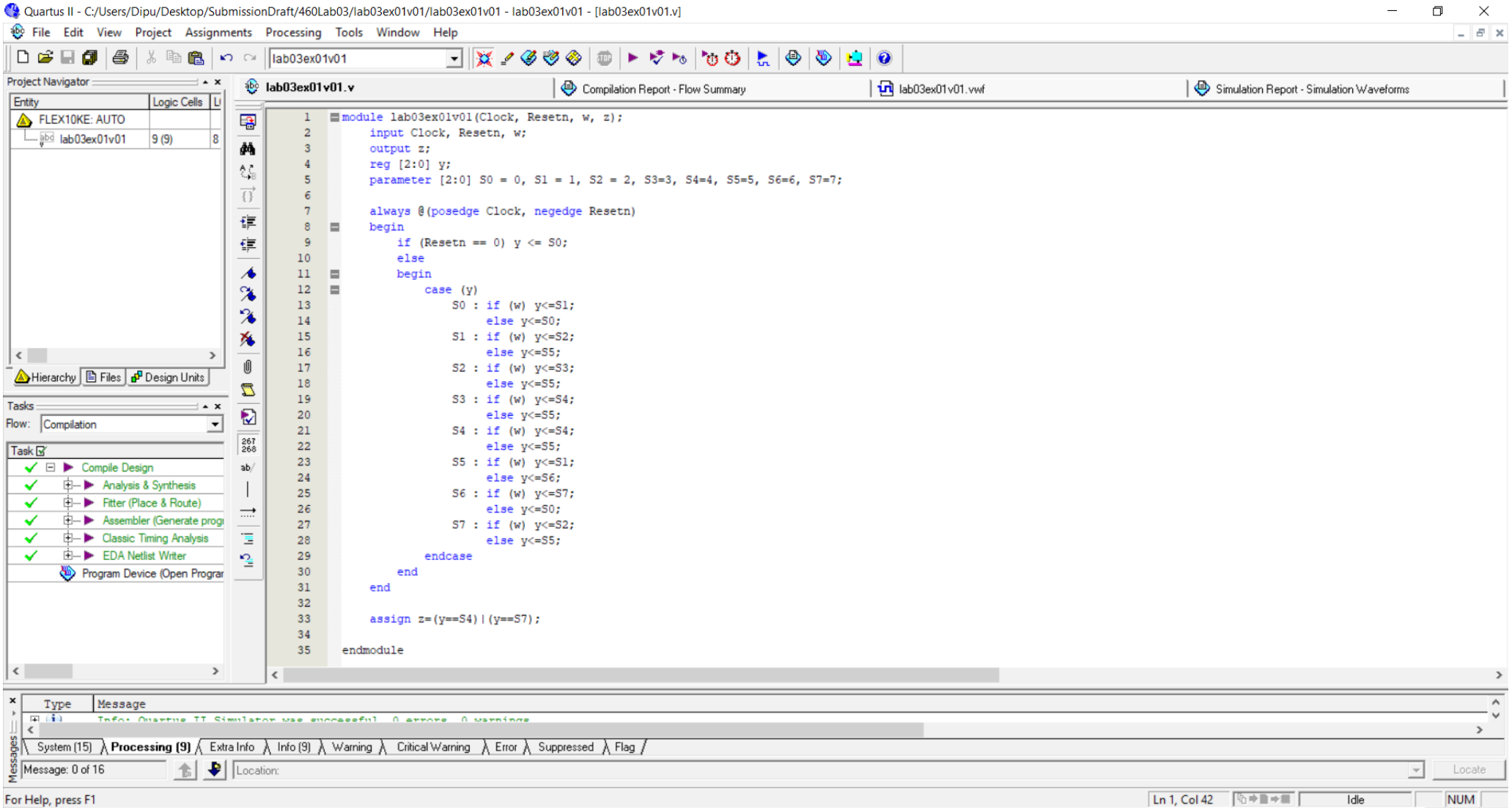
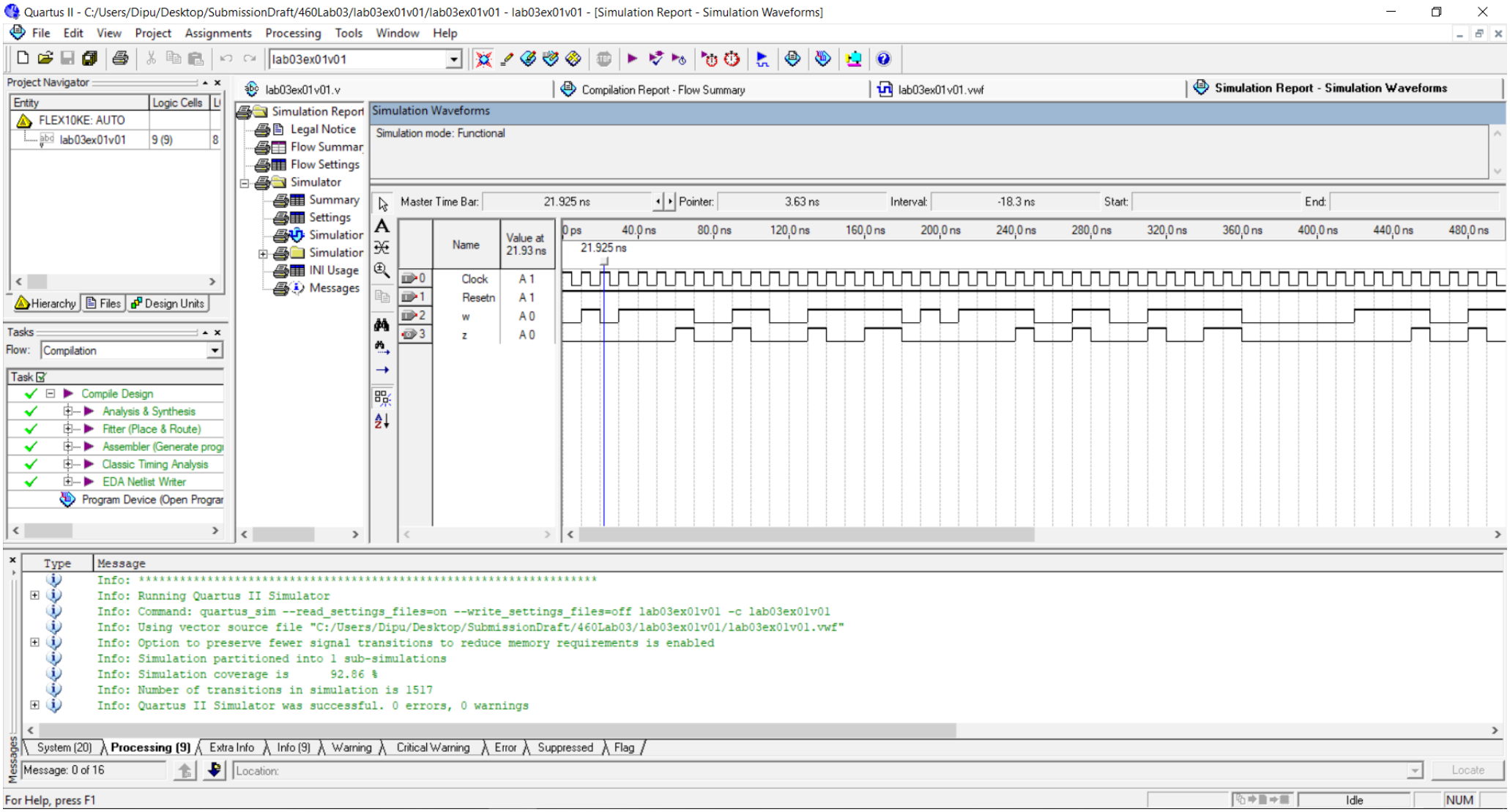
Lab 03 Assignment
Example 01 Verilog Code



Example 01 Vector Waveform



Example 01 Discussion

This FSM is a Mealy Type FSM as outputs of this Machine depends both on the state of the circuit and the present values of its input.

If previous four values of input were either 1001 or 1111, it will generate an output value of 1, otherwise 0. It can keep track of overlapping sequence & provides output accordingly.
There are 8 states of this FSM & S0 is the Reset state of this FSM. If Reset receives a value of 0, this FSM will go back to its Reset state.

Homework 01 State Diagram

To compare individual bits, let, $K = W_1 \oplus W_2$

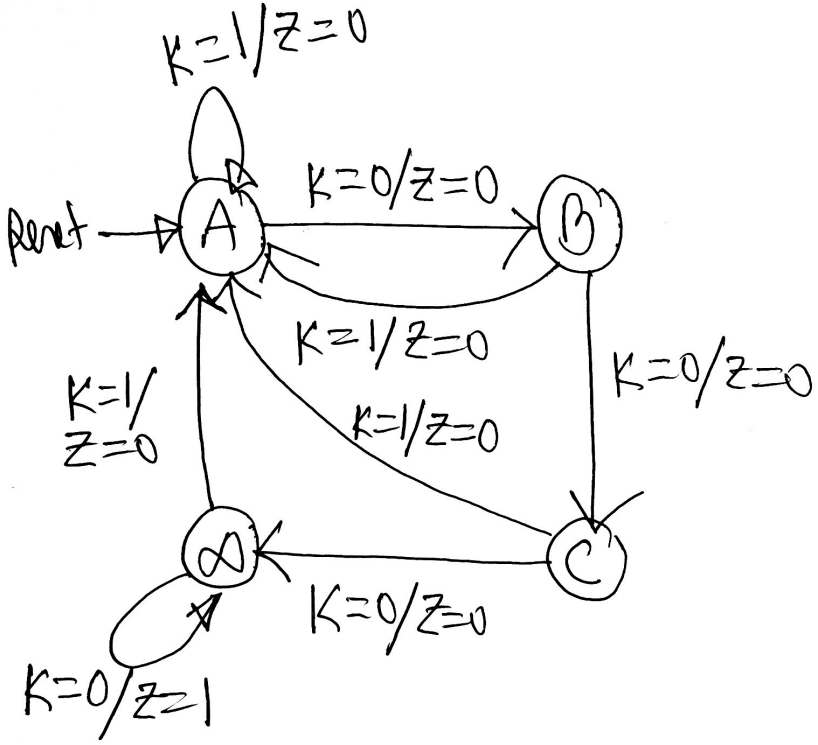


Fig: State diagram.

Home Work 01

State Table

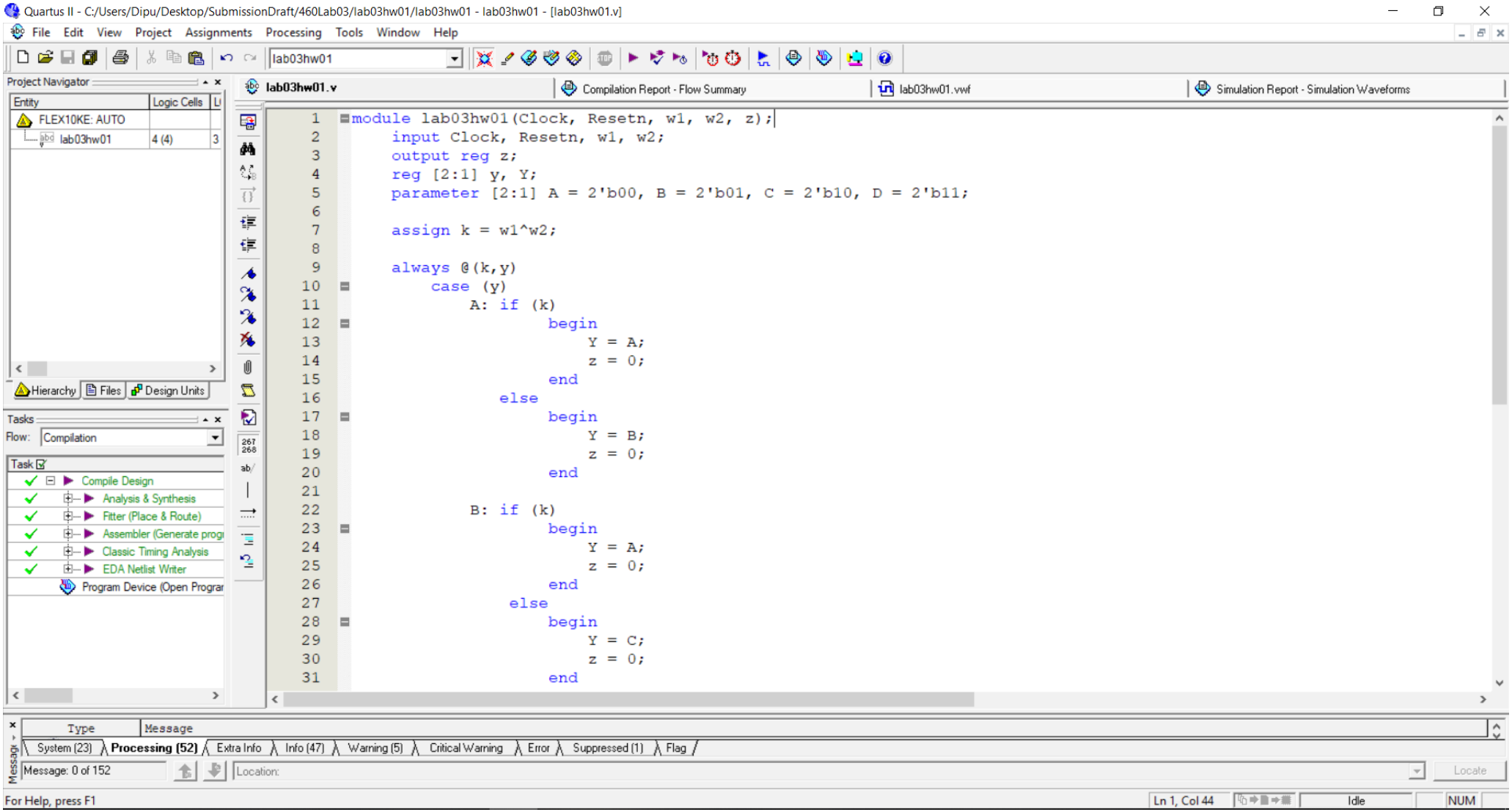
~~Let, K~~

To compare individual bits, let $K = W_1 \oplus W_2$.

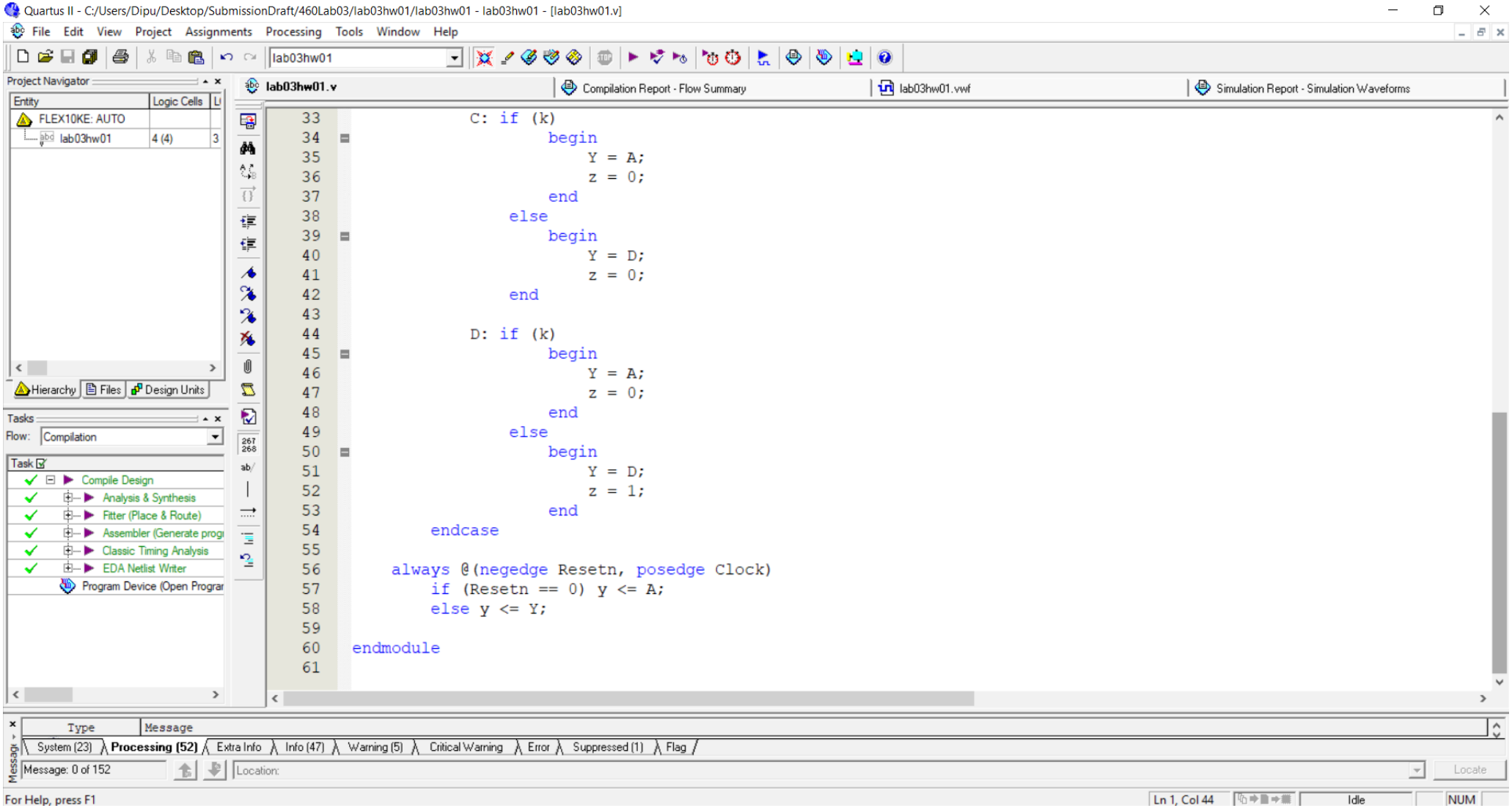
So, Truth Table for that,

Present State	Next State		Output Z	
	K=0	K=1	K=0	K=1
A	B	A	0	0
B	C	A	0	0
C	D	A	0	0
D	D	A	1	0

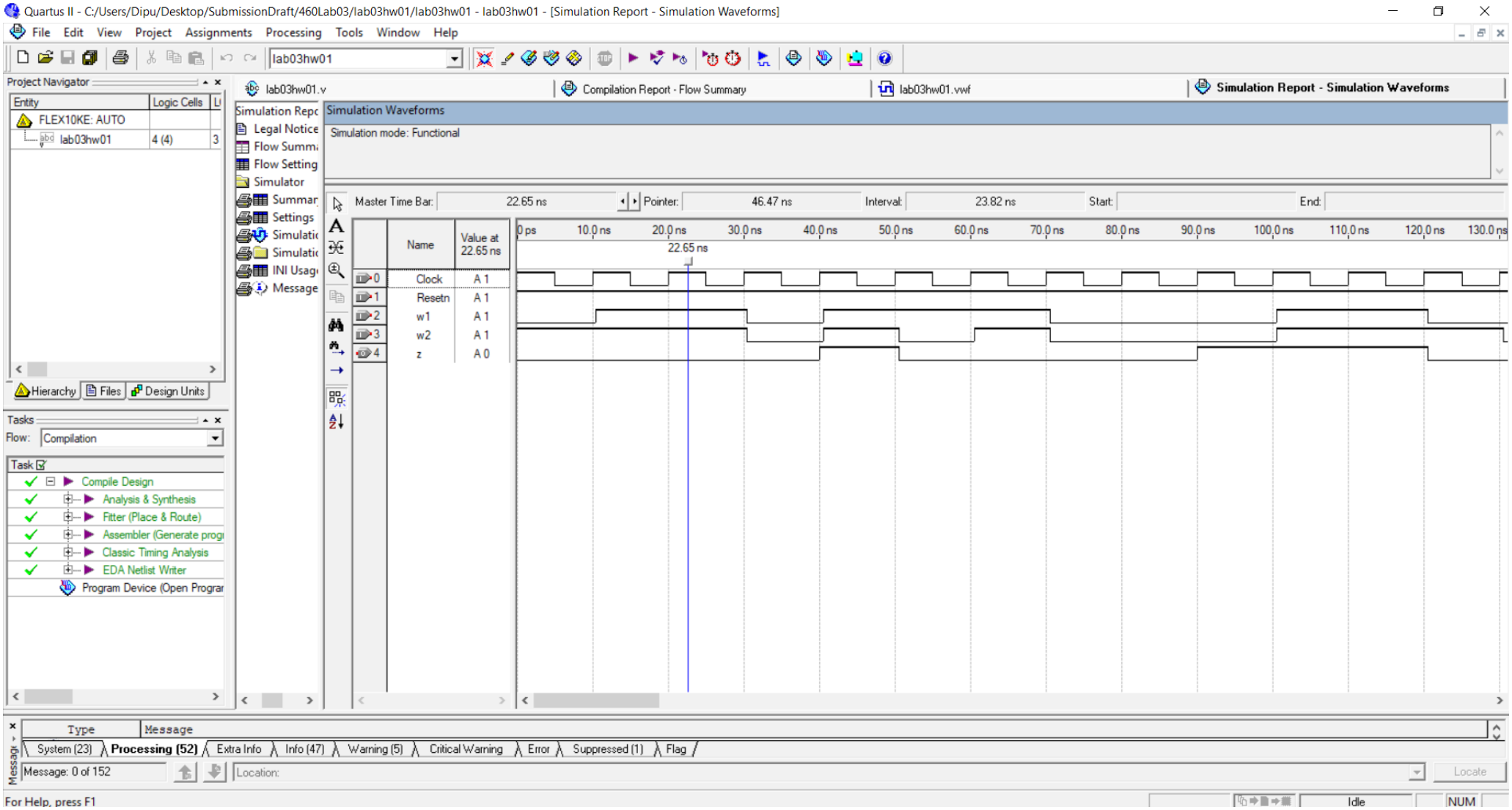
Homework 01 Verilog Code Part I



Homework 01 Verilog Code Part II



Homework 01 Vector Waveform



Homework 01 Discussion

This sequential circuit acts as a Mealy Type Finite State Machine. It takes two inputs, w1 & w2. And, then, it compares them using XOR operation. If the value of XOR operation is 0, that means on that particular clock cycle both inputs got matched, then it can proceed to next state other than Reset state A. If XOR operation provides a value of 1, that means inputs are not same on that clock cycle & we will have to get back to reset state.

If w1 = w2 during any four consecutive clock cycles, then, this FSM provides an output value 1, otherwise 0. It can keep track of overlapping sequence & provides output accordingly.

A is the Reset state of this FSM. If Reset receives a value of 0, this FSM will go back to its Reset state.

Homework 02 State Diagram

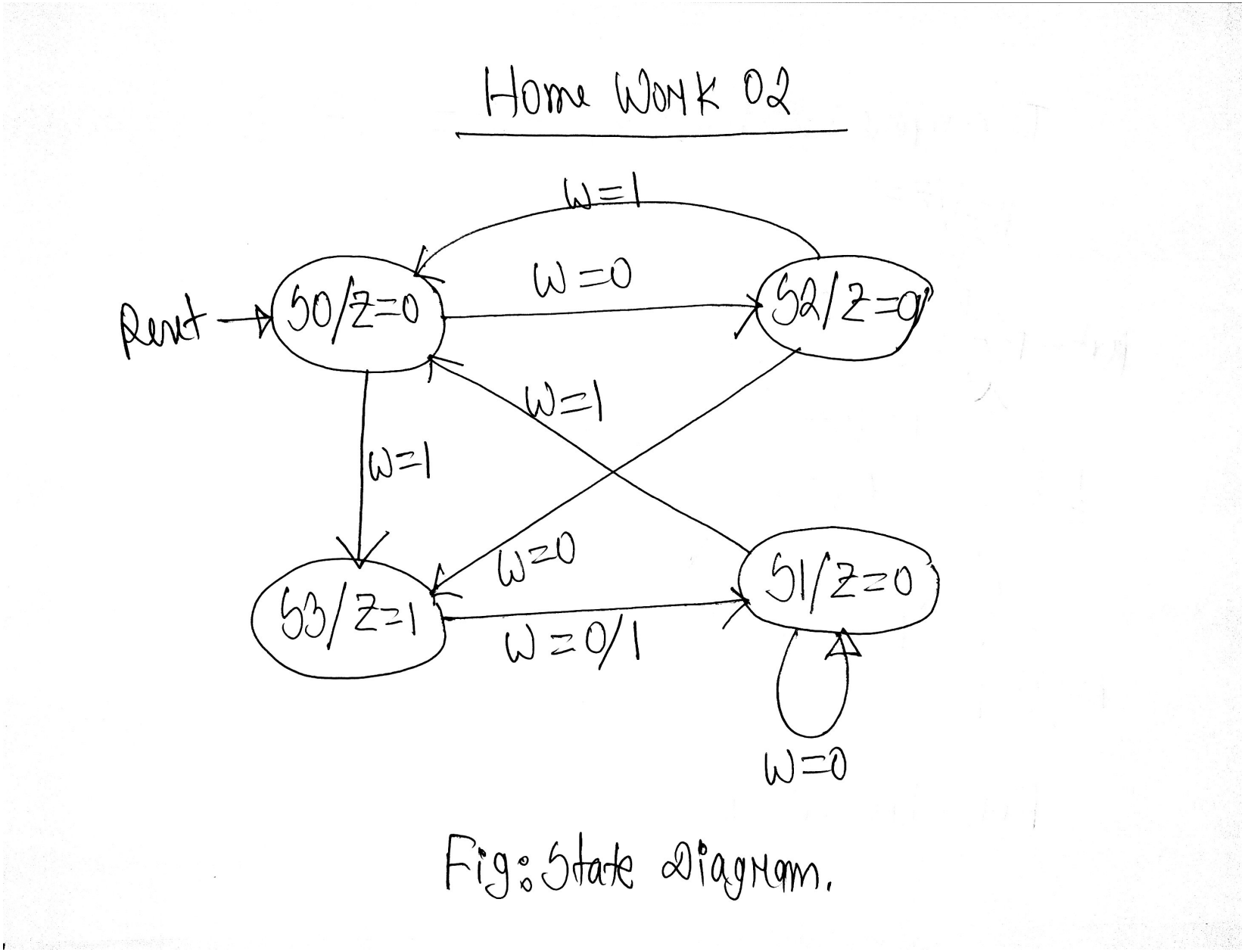
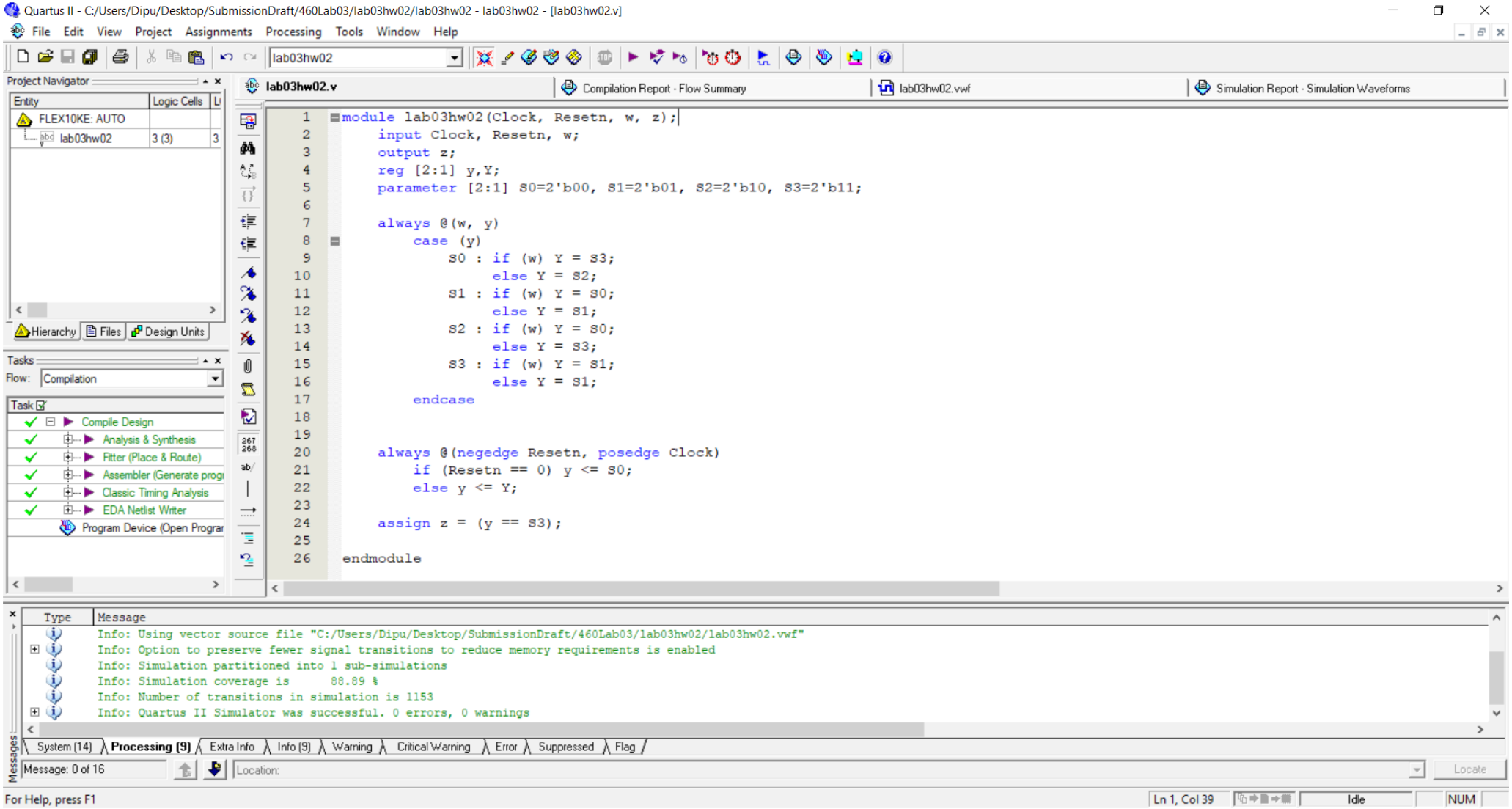
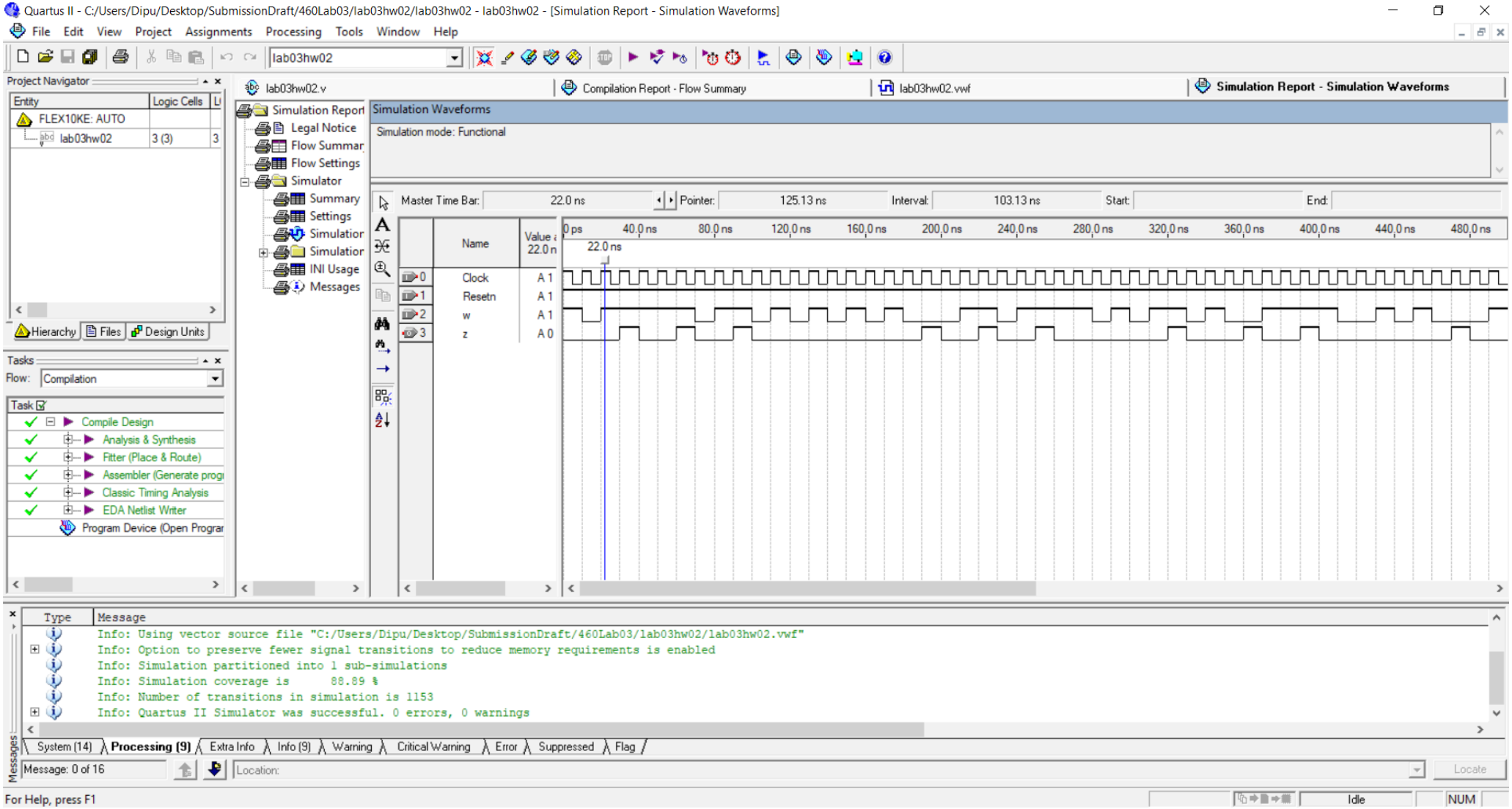


Fig: State diagram.

Homework 02 Verilog Code



Homework 02 Vector Waveform



Homework 02 Discussion

This FSM is a Moore Type FSM as outputs of this Machine depends only on the state of the circuit. Unlike Mealy, its output doesn't depend on the present values of inputs. S3 is the only accepting state of this Machine which will provide output 1, in other states, output will be 0.

If S0 receives 1 as input, it will go to S3, otherwise will go to S2. If S1 receives 1 as input, it will go to S0, otherwise will go to S1. If S2 receives 1 as input, it will go to S0, otherwise will go to S3. And, If S3 receives either 0 or 1 as input, it will go to only one state, S1.

S0 is the Reset state of this FSM. If Reset receives a value of 0, this FSM will go back to its Reset state.