



Inspiring Excellence

CSE460

VLSI Design

Lab Assignment : 02

Submitted By

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Lab Assignment 02

Home Work 01 Verilog Code

Quartus II - C:/Users/Dipu/Desktop/SubmissionDraft/460Lab/Lab02Draft/demux1to4/demux1to4 - demux1to4 - [demux1to4.v]

File Edit View Project Assignments Processing Tools Window Help

demux1to4

Project Navigator

Entity	Logic Cells	LI
FLEX10KE: AUTO		
demux1to4	8 (8)	0

Hierarchy Files Design Units

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Program)

```
1 module demux1to4(w, s, f);
2
3     output reg [3:0] f;
4     input [1:0] s;
5     input w;
6
7     always @(w, s)
8     case(s)
9     2'b00 : begin
10         f[0] = w;
11         f[3:1] = 0;
12     end
13     2'b01 : begin
14         f[1] = w;
15         f[0] = 0;
16     end
17     2'b10 : begin
18         f[2] = w;
19         f[1:0] = 0;
20     end
21     2'b11 : begin
22         f[3] = w;
23         f[2:0] = 0;
24     end
25     endcase
26 endmodule
```

Messages

Type Message

- Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
- Info: Simulation partitioned into 1 sub-simulations
- Info: Simulation coverage is 93.61 %

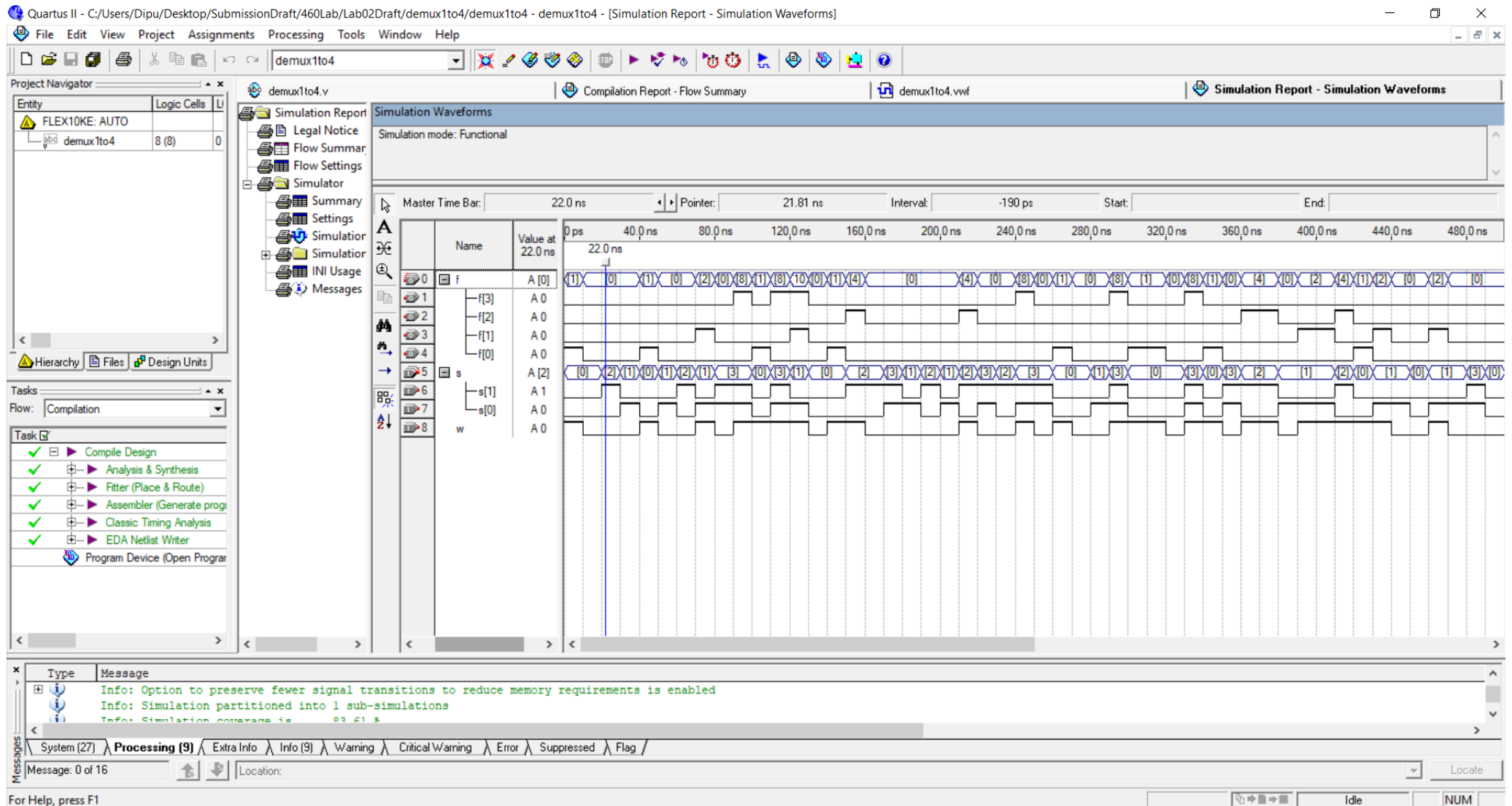
System (27) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag

Message: 0 of 16 Location: Locate

For Help, press F1

Ln 1, Col 27 Idle NUM

Home Work 01 Vector Waveform



Home Work 01 Discussion

It is a 1 to 4 DEMUX. It takes an 1 bit input, w and 2 bit input, s which is selector and provides a 4 bit output, f. Depending on the combination of selector, it provides 1 output among 4 available options.

Home Work 02 Verilog Code

Quartus II - C:/Users/Dipu/Desktop/SubmissionDraft/460Lab/Lab02Draft/decoder3to8/decoder3to8 - decoder3to8.v

File Edit View Project Assignments Processing Tools Window Help

decoder3to8

Project Navigator

Entity	Logic Cells	LI
FLEX10KE: AUTO		
decoder3to8	8 (8)	0

Hierarchy Files Design Units

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Programmer)

decoder3to8.v

```
1 module decoder3to8(w,y);
2
3 input [2:0]w;
4 output reg[7:0]y;
5
6 always @(w)
7     case (w)
8         3'b000 : y = 8'b00000001;
9         3'b001 : y = 8'b00000010;
10        3'b010 : y = 8'b00000100;
11        3'b011 : y = 8'b00001000;
12        3'b100 : y = 8'b00010000;
13        3'b101 : y = 8'b00100000;
14        3'b110 : y = 8'b01000000;
15        3'b111 : y = 8'b10000000;
16        default : y = 8'b00000000;
17    endcase
18 endmodule
```

Simulation Report - Simulation Waveforms

Messages

Type	Message
Info	Command: quartus_sim --read_settings_files=on --write_settings_files=off decoder3to8 -c decoder3to8
Info	Using vector source file "C:/Users/Dipu/Desktop/SubmissionDraft/460Lab/Lab02Draft/decoder3to8/decoder3to8.vwf"
Info	Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Simulation partitioned into 1 sub-simulations
Info	Simulation coverage is 100.00 %
Info	Number of transitions in simulation is 563

System (18) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag

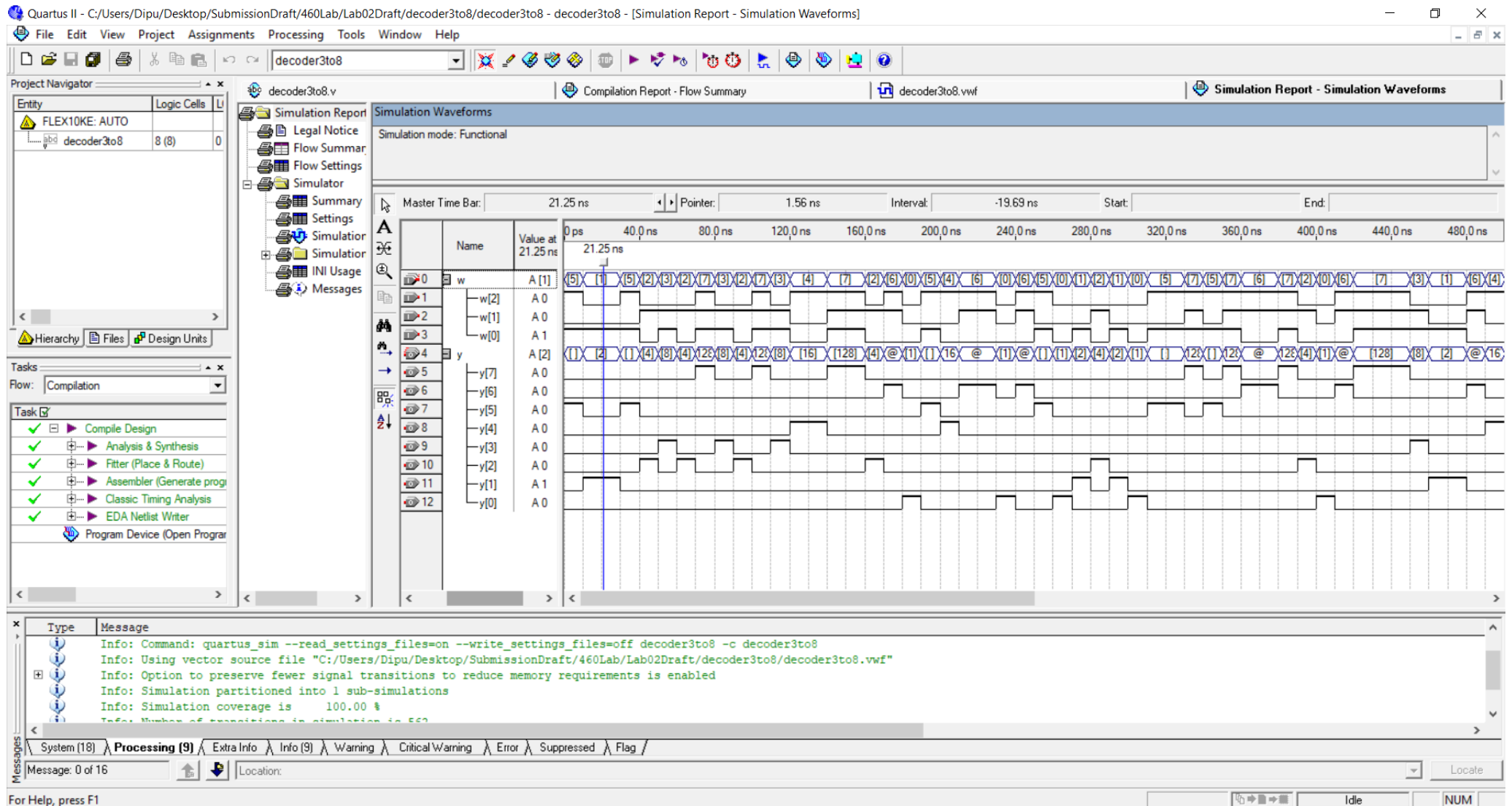
Message: 0 of 16

Location:

For Help, press F1

Ln 1, Col 25 Idle NUM

Home Work 02 Vector Waveform



Home Work 02 Discussion

It is a 3 to 8 decoder. It takes 3 bits input w and provides an output which have 8 bits. Depending on the combinations of 3 bits input w, it provides a single output represented in 8 bits.

Home Work 03 Verilog Code

Quartus II - C:/Users/Dipu/Desktop/SubmissionDraft/460Lab/Lab02Draft/updowncounter/updowncounter - updowncounter.v

File Edit View Project Assignments Processing Tools Window Help

updowncounter

Project Navigator

Entity	Logic Cells	U
FLEX10KE: AUTO		
updowncounter	6 (2)	4

Hierarchy Files Design Units

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Programmer)

updowncounter.v

```
1 module updowncounter(rst,clk,q,updown);
2     input rst,clk,updown;
3     output reg[3:0]q;
4
5     always @(posedge clk)
6     begin
7         if(rst)
8             q<=0;
9         else
10            if(updown)
11                if(q==15)
12                    q<=0;
13                else
14                    q<=q+1;
15            else
16                if(q==0)
17                    q<=15;
18                else
19                    q<=q-1;
20        end
21    endmodule
```

Simulation Report - Simulation Waveforms

Messages

Type	Message
Info	Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Warning	Warning: Found clock-sensitive change during active clock edge at time 170.0 ns on register " updowncounter q[3]-reg0"
Warning	Warning: Found clock-sensitive change during active clock edge at time 170.0 ns on register " updowncounter q[2]-reg0"
Warning	Warning: Found clock-sensitive change during active clock edge at time 170.0 ns on register " updowncounter q[1]-reg0"
Info	Info: Simulation partitioned into 1 sub-simulations
Info	Info: Simulation coverage is 74.79 %
Info	Info: Number of transitions in simulation is 7106
Info	Info: Quartus II Simulator was successful. 0 errors, 3 warnings

System (7) Processing (12) Extra Info Info (9) Warning (3) Critical Warning Error Suppressed Flag

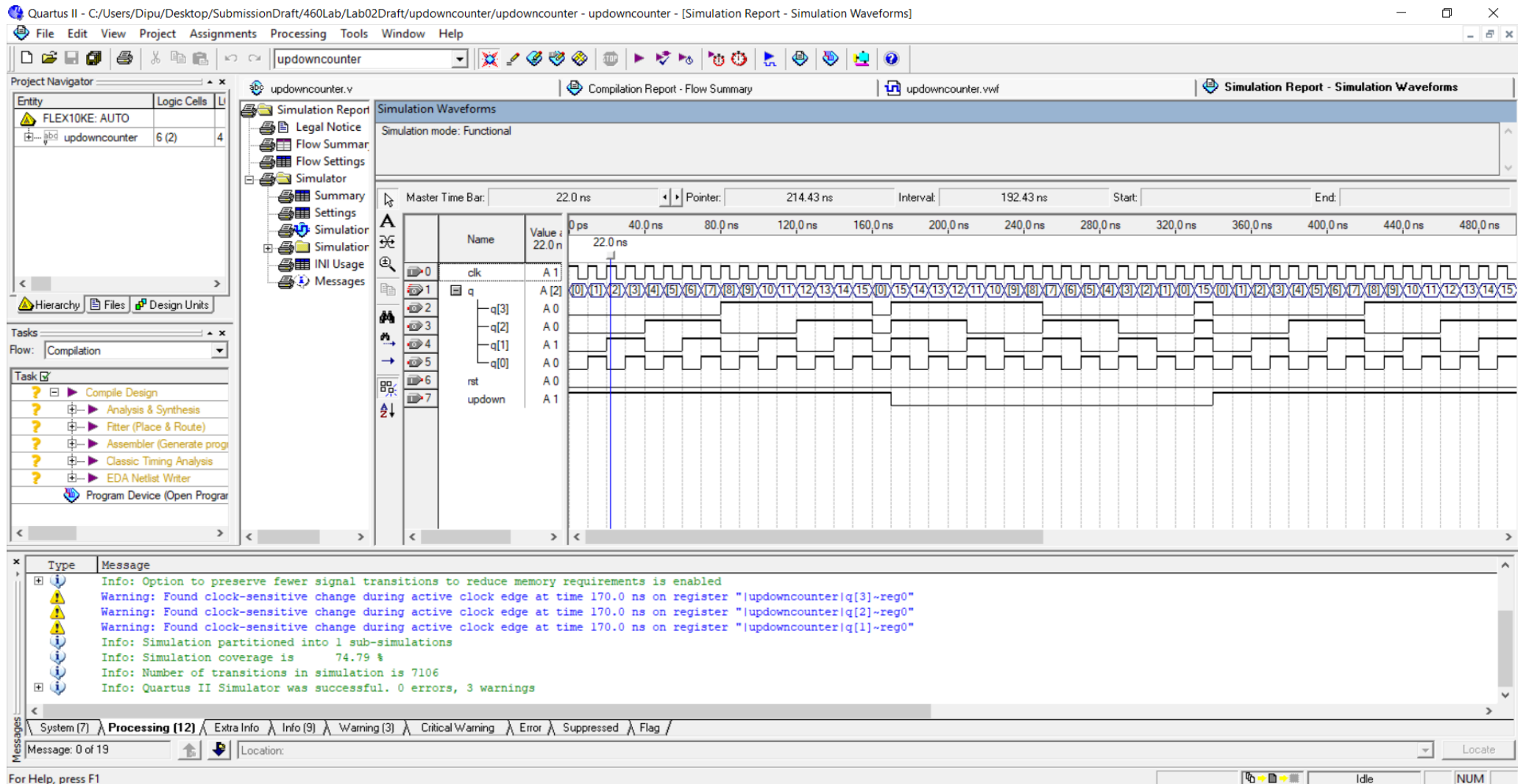
Message: 0 of 19

Location:

For Help, press F1

Ln 1, Col 40 Idle NUM

Home Work 03 Vector Waveform



Home Work 03 Discussion

It is an Up Down Counter. When we provide input value 1 for 'updown' it works as Up Counter. It counts from 0 to 15 & again 0 to 15 till updown=1. When we provide input value 0 for 'updown' it works as Down Counter, counts from 15 to 0 & again 15 to 0 till updown=0. To reset the counter we will have to provide rst=1.

Home Work 04 Verilog Code

Quartus II - C:/Users/Dipu/Desktop/SubmissionDraft/460Lab/Lab02Draft/ringcounter/ringcounter - ringcounter.v

File Edit View Project Assignments Processing Tools Window Help

ringcounter

Project Navigator

Entity	Logic Cells	U
FLEX10KE: AUTO		
ringcounter	4 (4)	4

Hierarchy Files Design Units

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Program)

```
1 module ringcounter(load,clk,q);
2
3     input load, clk;
4     output reg[3:0]q;
5
6     always @(posedge clk)
7         if(load)
8             q<=4'b1000;
9         else
10            begin
11                q[3]<=q[0];
12                q[2]<=q[3];
13                q[1]<=q[2];
14                q[0]<=q[1];
15            end
16 endmodule
```

Messages

System (17) Processing (13) Extra Info Info (9) Warning (4) Critical Warning Error Suppressed Flag

Message: 0 of 20

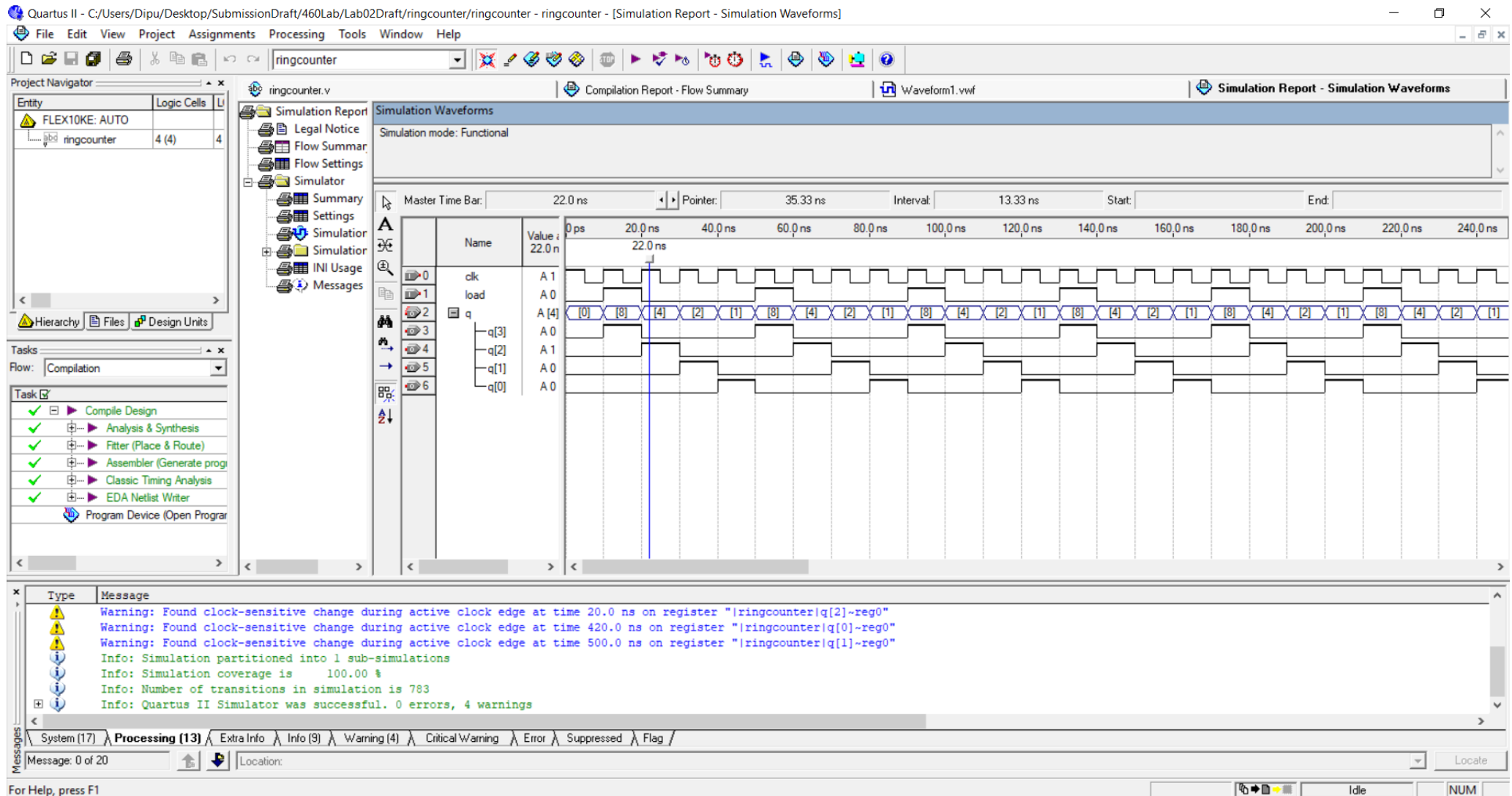
Location:

For Help, press F1

Ln 1, Col 32 Idle NUM

Warning: Found clock-sensitive change during active clock edge at time 20.0 ns on register "|ringcounter|q[2]-reg0"
Warning: Found clock-sensitive change during active clock edge at time 420.0 ns on register "|ringcounter|q[0]-reg0"
Warning: Found clock-sensitive change during active clock edge at time 500.0 ns on register "|ringcounter|q[1]-reg0"
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is 100.00 %
Info: Number of transitions in simulation is 783
Info: Quartus II Simulator was successful. 0 errors, 4 warnings

Home Work 04 Vector Waveform



Home Work 04 Discussion

It is a Ring Counter. A straight ring counter, also known as a one-hot counter, connects the output of the last shift register to the first shift register input and circulates a single one (or zero) bit around the ring. When load will be high & Clock Pulse will have Positive Edge, 1000(8) will be loaded and then the next values will be 0100(4), 0010(2), 0001(1), 1000(8),.....

Home Work 05 Verilog Code

Quartus II - C:/Users/Dipu/Desktop/SubmissionDraft/460Lab/Lab02Draft/Draft/johnsoncounterv1/johnsoncounterv1 - johnsoncounterv1 - [johnsoncounterv1.v]

File Edit View Project Assignments Processing Tools Window Help

johnsoncounterv1

Project Navigator

Entity	Logic Cells	U
FLEX10KE: AUTO		
johnsoncounterv1	4 (4)	4

Hierarchy Files Design Units

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Program)

```
1 module johnsoncounterv1(load,clk,q);
2
3     input load, clk;
4     output reg[3:0]q;
5
6     always @(posedge clk)
7         if(load)
8             q<=4'b0000;
9         else
10            begin
11                q[3]<=q[2];
12                q[2]<=q[1];
13                q[1]<=q[0];
14                q[0]<=~q[3];
15            end
16 endmodule
```

Messages

Type	Message
Warning	Warning: Found clock-sensitive change during active clock edge at time 510.0 ns on register " johnsoncounterv1 q[1]-reg0"
Warning	Warning: Found clock-sensitive change during active clock edge at time 570.0 ns on register " johnsoncounterv1 q[2]-reg0"
Warning	Warning: Found clock-sensitive change during active clock edge at time 570.0 ns on register " johnsoncounterv1 q[3]-reg0"
Info	Info: Simulation partitioned into 1 sub-simulations
Info	Info: Simulation coverage is 100.00 %
Info	Info: Number of transitions in simulation is 542
Info	Info: Quartus II Simulator was successful. 0 errors, 4 warnings

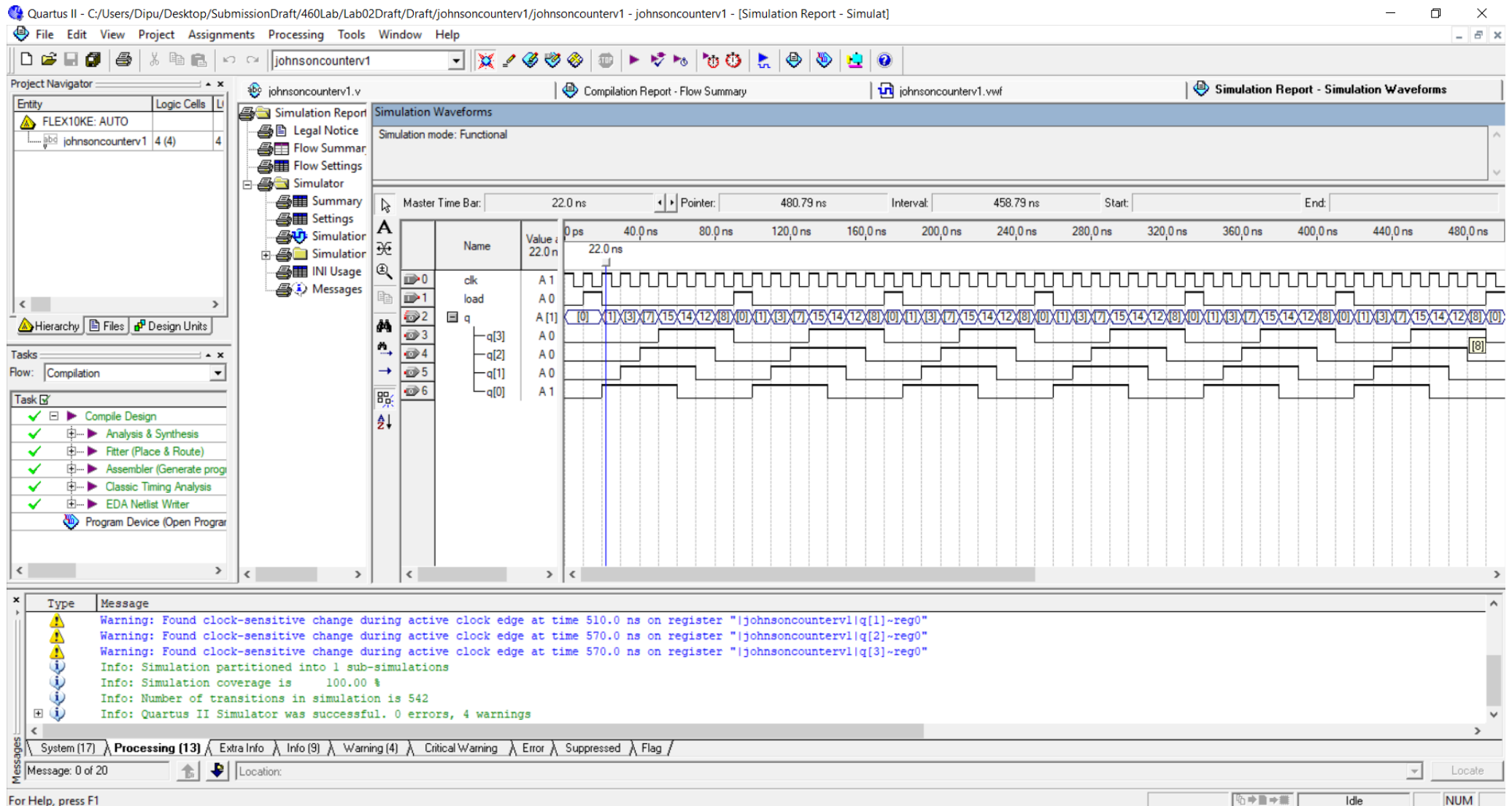
System (17) Processing (13) Extra Info Info (9) Warning (4) Critical Warning Error Suppressed Flag

Message: 0 of 20 Location: Locate

For Help, press F1

Ln 1, Col 37 Idle NUM

Home Work 05 Vector Waveform



Home Work 05 Discussion

It is a Johnson Counter. A twisted ring counter which connects the complement of the output of the last shift register to the input of the first register and circulates a stream of ones followed by zeros around the ring. When load will be high & Clock Pulse will have Positive Edge, 0000(0) will be loaded and then the next values will be 0001(1), 0011(3), 0111(7), 1111(15), 1110(14), 1100(12), 1000(8), 0000(0), 0001(1),.....