



Inspiring Excellence

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**CSE460**

**VLSI Design**

**Lab Assignment : 01**

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**Submitted By**

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## Lab Assignment 01

### Home Work 01 Verilog Code

Quartus II - C:/Users/Dipu/Desktop/SubmissionDraft/460Lab/Lab01Draft/mux4to1/mux4to1 - mux4to1 - [mux4to1.v]

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Entity	Logic Cells	LU
FLEX10KE: AUTO		
abg mux4to1	2 (2)	0

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate progi
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Progra

```
1 module mux4to1(w,s,f);
2
3 input [3:0]w;
4 input [1:0]s;
5 output reg f;
6
7 always @(w,s)
8     case(s)
9         0: f=w[0];
10        1: f=w[1];
11        2: f=w[2];
12        3: f=w[3];
13        default: f=1'bx;
14    endcase
15 endmodule
```

Messages

Type	Message
Info	Command: quartus_sim --read_settings_files=on --write_settings_files=off mux4to1 -c mux4to1
Info	Using vector source file "C:/Users/Dipu/Desktop/SubmissionDraft/460Lab/Lab01Draft/mux4to1/mux4to1.vwf"
Info	Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Simulation partitioned into 1 sub-simulations
Info	Simulation coverage is 100.00 %
Info	Number of transitions in simulation is 981

System [9] Processing [9] Extra Info Info [9] Warning Critical Warning Error Suppressed Flag

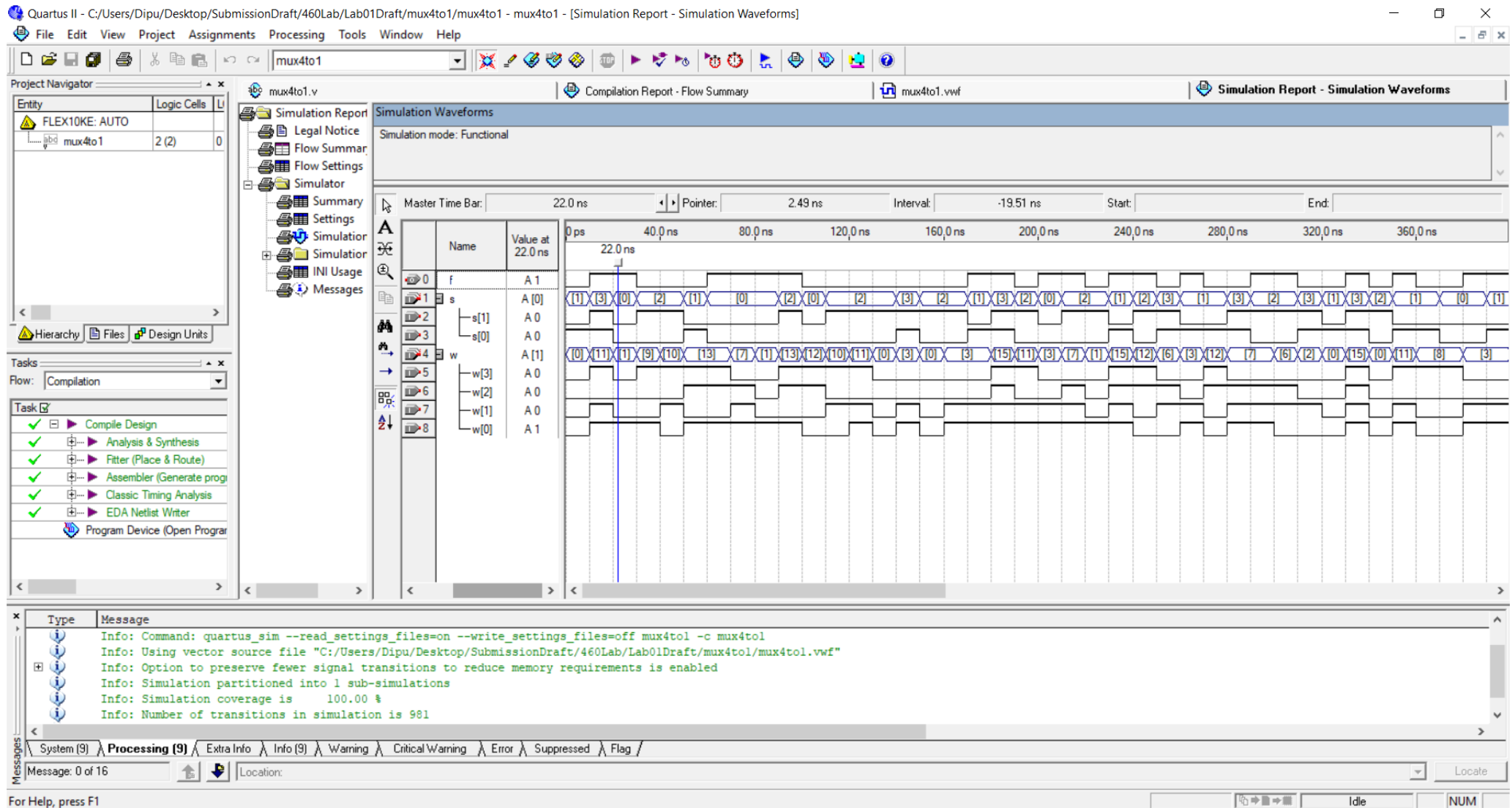
Message: 0 of 16

Location:

Ln 1, Col 23 Idle NUM

For Help, press F1

## Home Work 01 Vector Waveform



## Home Work 01 Discussion

It is a 4 to 1 MUX which takes 4 inputs and provides 1 output(f). It has two bit selector through which we get four binary combinations(00,01,10,11) which are 0,1,2,3 case in the Code. If we select 0(00), it will provide out the input it will have in w[0] and w[1], w[2] & w[3] for the cases 1(01), 2(10) & 3(11) respectively.

## Home Work 02 Verilog Code

Quartus II - C:/Users/Dipu/Desktop/SubmissionDraft/460Lab/Lab01Draft/prioenc/prioenc - prioenc.v [prioenc.v]

File Edit View Project Assignments Processing Tools Window Help

prioenc

Project Navigator

Entity	Logic Cells	LI
FLEX10KE: AUTO		
prioenc	5 (5)	0

Hierarchy Files Design Units

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate progi
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Progra

prioenc.v

```
1 module prioenc(w,y);
2
3   input [3:0]w;
4   output reg[1:0]y;
5
6   always @(w)
7   =   casex (w)
8       4'b1xxx: y=3;
9       4'b0x1x: y=1;
10      4'b0x01: y=0;
11      4'b0100: y=2;
12      endcase
13 endmodule
```

Compilation Report - Flow Summary

prioenc.vwf

Simulation Report - Simulation Waveforms

Type Message

- Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
- Info: Simulation partitioned into 1 sub-simulations
- Info: Simulation coverage is 78.87 %
- Info: Number of transitions in simulation is 8190
- Info: Quartus II Simulator was successful. 0 errors, 0 warnings

System (31) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag

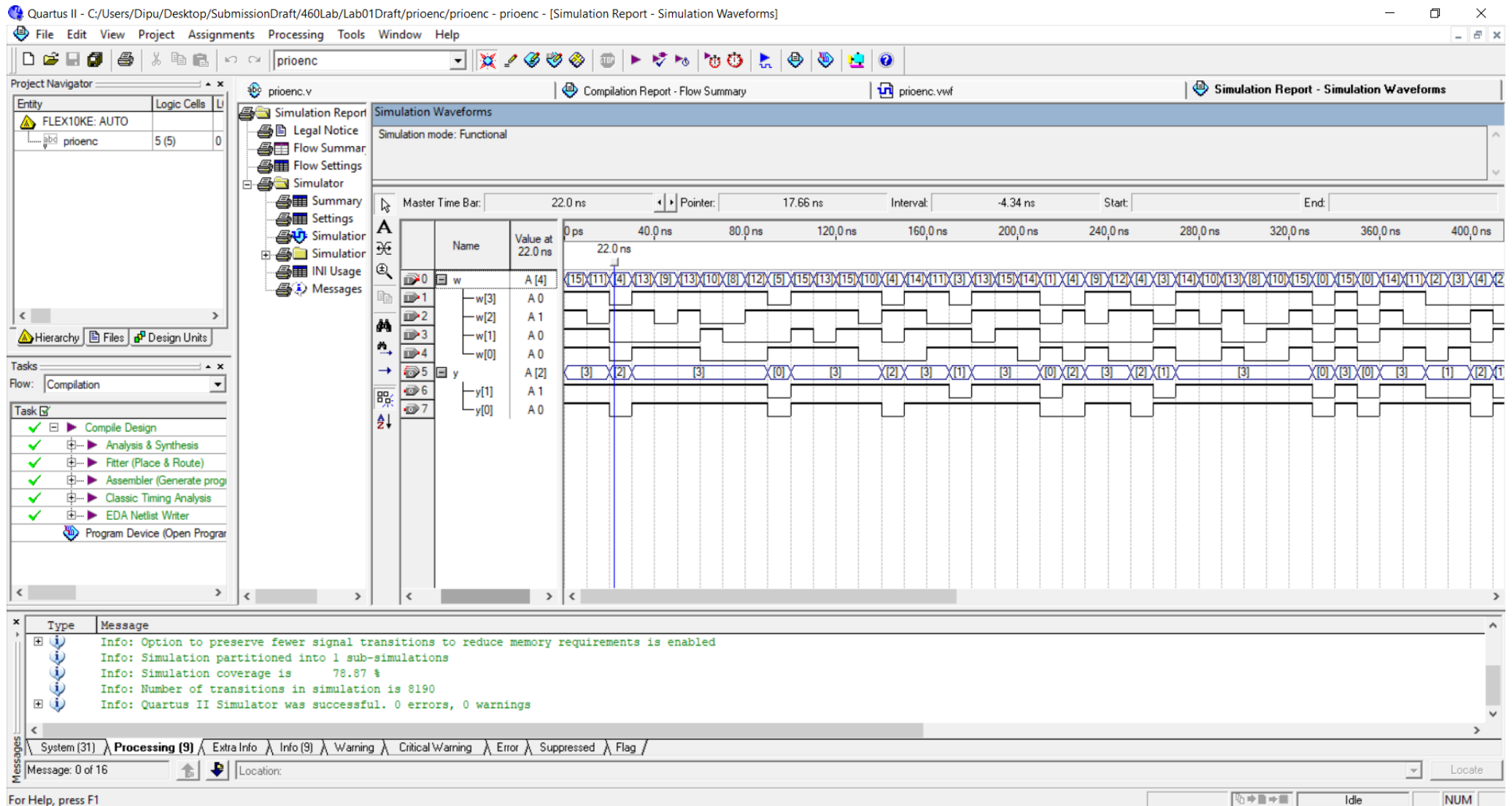
Message: 0 of 16

Location:

For Help, press F1

Ln 1, Col 21 Idle NUM

## Home Work 02 Vector Waveform



## Home Work 02 Discussion

It is a Priority Encoder having priority order  $3 > 1 > 0 > 2$ . It takes a 4 bits input & provides a 2 bits output. To appear in output, the corresponding bit of that number will have to high(1) & the corresponding bit(s) of higher priority number(s) will have to be low(0) & it won't care about the other bits.

## Home Work 03 Verilog Code

Quartus II - C:/Users/Dipu/Desktop/SubmissionDraft/460Lab/Lab01Draft/decoder2to4/decoder2to4 - decoder2to4.v

File Edit View Project Assignments Processing Tools Window Help

decoder2to4

Project Navigator

Entity	Logic Cells	LC Regs
FLEX10KE: AUTO		
decoder2to4	4 (4)	0

Hierarchy Files Design Units

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Programmer)

decoder2to4.v

```
1 module decoder2to4(w,y);
2
3   input [1:0]w;
4   output reg[3:0]y;
5
6   always @(w)
7   =   case (w)
8       2'd0: y=4'b0001;
9       2'd1: y=4'b0010;
10      2'd2: y=4'b0100;
11      2'd3: y=4'b1000;
12      default: y=4'b0000;
13  endcase
14 endmodule
```

Simulation Report - Simulation Waveforms

Messages

Type	Message
Info	Command: quartus_sim --read_settings_files=on --write_settings_files=off decoder2to4 -c decoder2to4
Info	Using vector source file "C:/Users/Dipu/Desktop/SubmissionDraft/460Lab/Lab01Draft/decoder2to4/decoder2to4.vwf"
Info	Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Simulation partitioned into 1 sub-simulations
Info	Simulation coverage is 100.00 %
Info	Number of transitions in simulation is 504
Info	Quartus II Simulator was successful. 0 errors, 0 warnings

System (13) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag

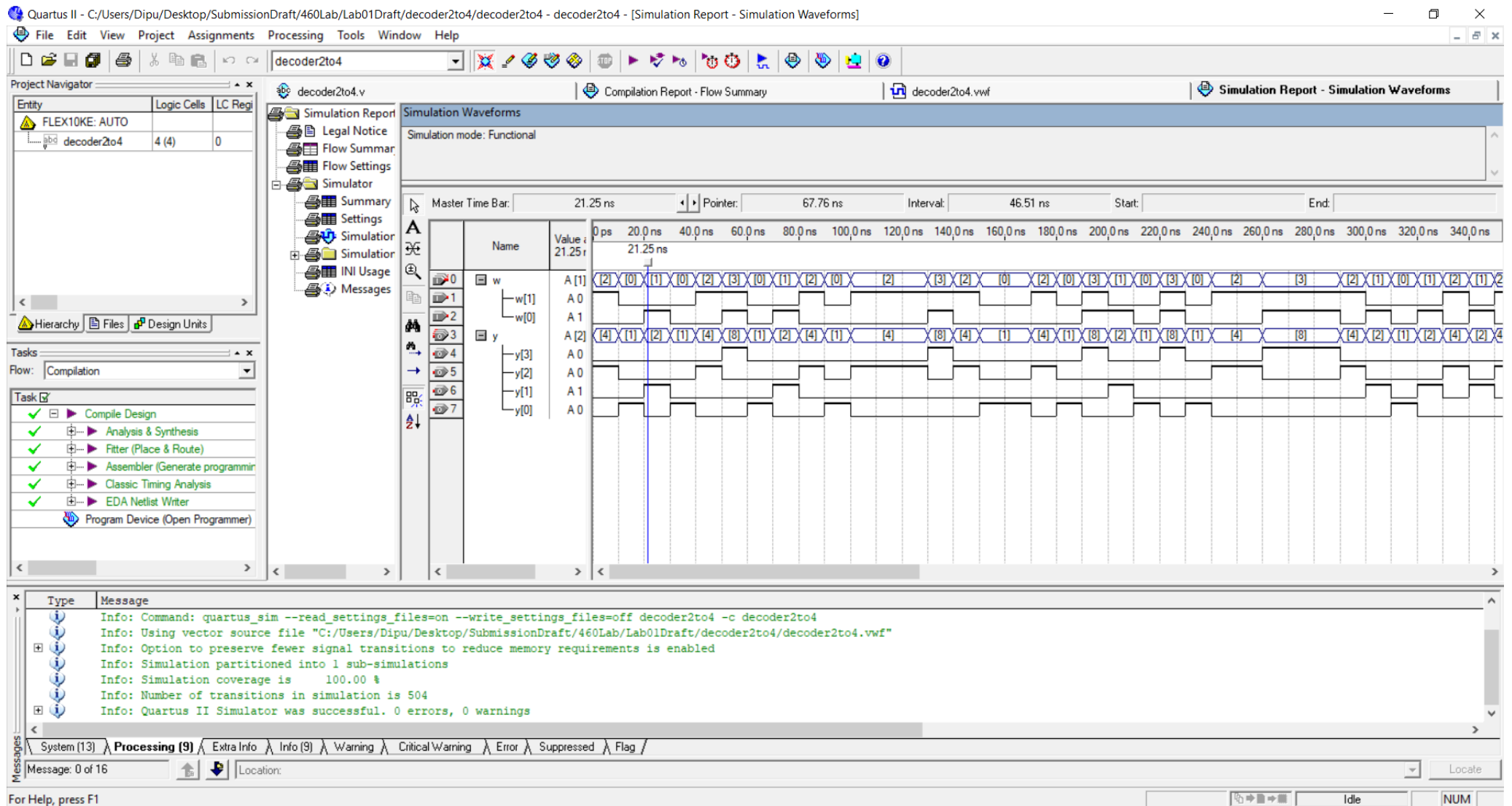
Message: 0 of 16

Location: Locate

For Help, press F1

Ln 1, Col 25 Idle NUM

## Home Work 03 Vector Waveform



## Home Work 03 Discussion

It is a 2 to 4 Decoder which takes 2 bits input and provides an output of 4 bits. Based on the 2 bits input, it will provide one output which will be represented in 4 bits. If none of the specific case is provided as input, it will provide an output value of 0 (0000 in 4 bit binary).

## Home Work 04 Verilog Code

Quartus II - C:/Users/Dipu/Desktop/SubmissionDraft/460Lab/Lab01Draft/addersubtractor/addersubtractor - addersubtractor.v

File Edit View Project Assignments Processing Tools Window Help

addersubtractor

Project Navigator

Entity	Logic Cells	L
FLEX10KE: AUTO		
addersubtractor	9 (1)	0

Hierarchy Files Design Units

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Programmer)

addersubtractor.v

```
1 module addersubtractor(S, Cout, A, B, Cin, V);
2     input [3:0]A,B;
3     input Cin;
4
5     output [3:0]S;
6     output Cout;
7     output V;
8
9     wire [3:1]C;
10    wire [3:0]BX;
11
12    assign BX[0] = B[0] ^ Cin;
13    assign BX[1] = B[1] ^ Cin;
14    assign BX[2] = B[2] ^ Cin;
15    assign BX[3] = B[3] ^ Cin;
16    assign V = C[3] ^ Cout;
17
18    // Cout <- |FA4| <- C3 <- |FA3| <- C2 <- |FA2| <- C1 <- |FA1| <- Cin
19
20    fulladd stage0 (S[0], C[1], A[0], BX[0], Cin);
21    fulladd stage1 (S[1], C[2], A[1], BX[1], C[1]);
22    fulladd stage2 (S[2], C[3], A[2], BX[2], C[2]);
23    fulladd stage3 (S[3], Cout, A[3], BX[3], C[3]);
24
25 endmodule
26
27 module fulladd(S, Cout, A, B, Cin);
28     input A, B, Cin;
29     output S, Cout;
30
31     assign S = A ^ B ^ Cin;
32     assign Cout = (A & B) | (Cin & (A ^ B));
33
34 endmodule
```

Message: 0 of 90

Location:

For Help, press F1

Ln 1, Col 47

Idle

NUM



## Home Work 04 Vector Waveform : Addition

Quartus II - C:/Users/Dipu/Desktop/SubmissionDraft/460Lab/Lab01Draft/addersubtractor/addersubtractor - addersubtractor - [Simulation Report - Simulation Wavef]

File Edit View Project Assignments Processing Tools Window Help

addersubtractor

Project Navigator

Entity	Logic Cells	U
FLEX10KE: AUTO		
addersubtractor	9 (1)	0

Simulation Report

- Legal Notice
- Flow Summary
- Flow Settings
- Simulator
  - Summary
  - Settings
  - Simulation
  - Simulation
  - INI Usage
  - Messages

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate progi
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Prograr

Simulation Waveforms

Simulation mode: Functional

Master Time Bar: 22.65 ns Pointer: 55.8 ns Interval: 33.15 ns Start: End:

Name	Value at 22.65 ns
A	H 9
B	H 6
Cin	A 0
Cout	A 0
S	A [15]
V	A 0

Messages

Type Message

- Info: \*\*\*\*\*
- Info: Running Quartus II Simulator
- Info: Command: quartus\_sim --read\_settings\_files=on --write\_settings\_files=off addersubtractor -c addersubtractor
- Info: Using vector source file "C:/Users/Dipu/Desktop/SubmissionDraft/460Lab/Lab01Draft/addersubtractor/addersubtractor.vwf"
- Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
- Info: Simulation partitioned into 1 sub-simulations
- Info: Simulation coverage is 0.00 %
- Info: Number of transitions in simulation is 0
- Info: Quartus II Simulator was successful. 0 errors, 0 warnings

System (12) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag

Message: 0 of 16 Location: Locate

For Help, press F1

Idle NUM

## Home Work 04 Vector Waveform : Subtraction

Quartus II - C:/Users/Dipu/Desktop/SubmissionDraft/460Lab/Lab01Draft/addersubtractor/addersubtractor - addersubtractor - [Simulation Report - Simulation Wavef]

File Edit View Project Assignments Processing Tools Window Help

addersubtractor

Project Navigator

Entity	Logic Cells	U
FLEX10KE: AUTO		
addersubtractor	9 (1)	0

Simulation Report

- Legal Notice
- Flow Summary
- Flow Settings
- Simulator
  - Summary
  - Settings
  - Simulation
  - Simulation
  - INI Usage
  - Messages

Simulation Waveforms

Simulation mode: Functional

Master Time Bar: 22.65 ns Pointer: 46.71 ns Interval: 24.06 ns Start: End:

Name	Value	0 ps	10.0 ns	20.0 ns	30.0 ns	40.0 ns	50.0 ns	60.0 ns	70.0 ns
A	H					9			
B	H					6			
Cin	A								
Cout	A								
S	A					[3]			
V	A								

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate progi
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Progr

Messages

Type	Message
Info	*****
Info	Running Quartus II Simulator
Info	Command: quartus_sim --read_settings_files=on --write_settings_files=off addersubtractor -c addersubtractor
Info	Using vector source file "C:/Users/Dipu/Desktop/SubmissionDraft/460Lab/Lab01Draft/addersubtractor/addersubtractor.vwf"
Info	Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Simulation partitioned into 1 sub-simulations
Info	Simulation coverage is 0.00 %
Info	Number of transitions in simulation is 0
Info	Quartus II Simulator was successful. 0 errors, 0 warnings

System (7) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag

Message: 0 of 16

Location:

For Help, press F1

Idle NUM

### **Home Work 04 Discussion**

It is a 4 bit ripple carry adder & subtractor which can take input as two 4 bits number. If we provide 0 in Cin, it will perform Addition Operation & for Cin=1, it will perform Subtraction Operation. This has been implemented in Code using a subcircuit 'fulladd'. Here S will have the value of Addition or Subtraction, Cout will have the value of Carry Out of last full adder & V will provide us idea about Overflow Status. Here we do perform XOR operation between the input value of Cin & each bit of input B.