



Inspiring Excellence

---

**CSE460**

**VLSI Design**

**Lab Assignment : 03**

---

**Submitted By**

Shoaib Ahmed Dipu

Student ID : 17101482

CSE460-13, Summer 2020

Submission Date : 11 Sept 2020

## Lab 03 Assignment

### Example 01 Verilog Code

Quartus II - C:/Users/Dipu/Desktop/SubmissionDraft/460Lab03/lab03ex01v01/lab03ex01v01 - lab03ex01v01 - [lab03ex01v01.v]

File Edit View Project Assignments Processing Tools Window Help

lab03ex01v01

lab03ex01v01.v Compilation Report - Flow Summary lab03ex01v01.vwf Simulation Report - Simulation Waveforms

Entity Logic Cells L

Entity	Logic Cells	L
FLEX10KE: AUTO		
lab03ex01v01	9 (9)	8

Hierarchy Files Design Units

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Program)

```
1 module lab03ex01v01(Clock, Resetn, w, z);
2     input Clock, Resetn, w;
3     output z;
4     reg [2:0] y;
5     parameter [2:0] S0 = 0, S1 = 1, S2 = 2, S3=3, S4=4, S5=5, S6=6, S7=7;
6
7     always @(posedge Clock, negedge Resetn)
8     begin
9         if (Resetn == 0) y <= S0;
10        else
11            begin
12                case (y)
13                    S0 : if (w) y<=S1;
14                        else y<=S0;
15                    S1 : if (w) y<=S2;
16                        else y<=S5;
17                    S2 : if (w) y<=S3;
18                        else y<=S5;
19                    S3 : if (w) y<=S4;
20                        else y<=S5;
21                    S4 : if (w) y<=S4;
22                        else y<=S5;
23                    S5 : if (w) y<=S1;
24                        else y<=S6;
25                    S6 : if (w) y<=S7;
26                        else y<=S0;
27                    S7 : if (w) y<=S2;
28                        else y<=S5;
29                endcase
30            end
31        end
32
33        assign z=(y==S4) | (y==S7);
34
35    endmodule
```

Messages

Type Message

Info: Quartus II Simulator was successful. 0 errors, 0 warnings.

System (15) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag

Message: 0 of 16

Location: Locate

For Help, press F1

Ln 1, Col 42 Idle NUM

## Example 01 Vector Waveform

Quartus II - C:/Users/Dipu/Desktop/SubmissionDraft/460Lab03/lab03ex01v01/lab03ex01v01 - lab03ex01v01 - [Simulation Report - Simulation Waveforms]

File Edit View Project Assignments Processing Tools Window Help

lab03ex01v01

Project Navigator

Entity	Logic Cells	U
FLEX10KE: AUTO		
lab03ex01v01	9 (9)	8

Simulation Report

- Legal Notice
- Flow Summary
- Flow Settings
- Simulator
  - Summary
  - Settings
  - Simulation
  - Simulation
  - INI Usage
  - Messages

Simulation Waveforms

Simulation mode: Functional

Master Time Bar: 21.925 ns Pointer: 3.63 ns Interval: -18.3 ns Start: End:

Name	Value at 21.93 ns
0 Clock	A 1
1 Resetn	A 1
2 w	A 0
3 z	A 0

0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns 320.0 ns 360.0 ns 400.0 ns 440.0 ns 480.0 ns

21.925 ns

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Program)

Messages

Type	Message
Info	*****
Info	Running Quartus II Simulator
Info	Command: quartus_sim --read_settings_files=on --write_settings_files=off lab03ex01v01 -c lab03ex01v01
Info	Using vector source file "C:/Users/Dipu/Desktop/SubmissionDraft/460Lab03/lab03ex01v01/lab03ex01v01.vwf"
Info	Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Simulation partitioned into 1 sub-simulations
Info	Simulation coverage is 92.86 %
Info	Number of transitions in simulation is 1517
Info	Quartus II Simulator was successful. 0 errors, 0 warnings

System (20) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag

Message: 0 of 16 Location: Locate

For Help, press F1

Idle NUM

### **Example 01 Discussion**

This FSM is a Mealy Type FSM as outputs of this Machine depends both on the state of the circuit and the present values of its input.

If previous four values of input were either 1001 or 1111, it will generate an output value of 1, otherwise 0. It can keep track of overlapping sequence & provides output accordingly. There are 8 states of this FSM & S0 is the Reset state of this FSM. If Reset receives a value of 0, this FSM will go back to its Reset state.

# Homework 01 State Diagram

To compare individual bits, let,  $K = w_1 \oplus w_2$

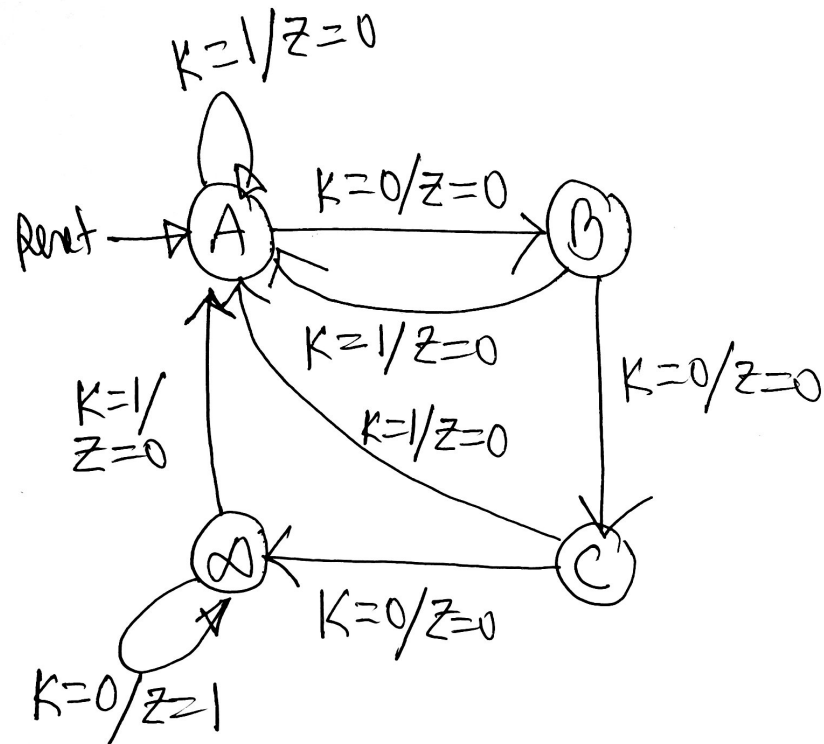


Fig: State diagram.

# Homework 01 State Table

## Home Work 01

### State Table

Let, ~~K~~

To compare individual bits, let  $K = w_1 \oplus w_2$ .  
So, Truth Table for that,

Present State	Next State		Output Z	
	K=0	K=1	K=0	K=1
A	B	A	0	0
B	C	A	0	0
C	A	A	0	0
A	A	A	1	0

## Homework 01 Verilog Code Part I

Quartus II - C:/Users/Dipu/Desktop/SubmissionDraft/460Lab03/lab03hw01/lab03hw01 - lab03hw01 - [lab03hw01.v]

File Edit View Project Assignments Processing Tools Window Help

lab03hw01

Project Navigator

Entity	Logic Cells	U
FLEX10KE: AUTO		
lab03hw01	4 (4)	3

Hierarchy Files Design Units

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Programmer)

lab03hw01.v

```
1 module lab03hw01(Clock, Resetn, w1, w2, z);
2     input Clock, Resetn, w1, w2;
3     output reg z;
4     reg [2:1] y, Y;
5     parameter [2:1] A = 2'b00, B = 2'b01, C = 2'b10, D = 2'b11;
6
7     assign k = w1^w2;
8
9     always @(k, Y)
10         case (Y)
11             A: if (k)
12                 begin
13                     Y = A;
14                     z = 0;
15                 end
16             else
17                 begin
18                     Y = B;
19                     z = 0;
20                 end
21             B: if (k)
22                 begin
23                     Y = A;
24                     z = 0;
25                 end
26             else
27                 begin
28                     Y = C;
29                     z = 0;
30                 end
31             end
```

Message

Type Message

System (23) Processing (52) Extra Info Info (47) Warning (5) Critical Warning Error Suppressed (1) Flag

Message: 0 of 152

Location:

Locate

For Help, press F1

Ln 1, Col 44 Idle NUM

## Homework 01 Verilog Code Part II

Quartus II - C:/Users/Dipu/Desktop/SubmissionDraft/460Lab03/lab03hw01/lab03hw01 - lab03hw01 - [lab03hw01.v]

File Edit View Project Assignments Processing Tools Window Help

lab03hw01

Project Navigator

Entity	Logic Cells	U
FLEX10KE: AUTO		
lab03hw01	4 (4)	3

lab03hw01.v

Compilation Report - Flow Summary

lab03hw01.vwf

Simulation Report - Simulation Waveforms

```
33      C: if (k)
34          begin
35              Y = A;
36              z = 0;
37          end
38      else
39          begin
40              Y = D;
41              z = 0;
42          end
43
44      D: if (k)
45          begin
46              Y = A;
47              z = 0;
48          end
49      else
50          begin
51              Y = D;
52              z = 1;
53          end
54      endcase
55
56      always @(negedge Resetn, posedge Clock)
57          if (Resetn == 0) y <= A;
58          else y <= Y;
59
60  endmodule
61
```

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate prog)
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Programmer)

Message: 0 of 152

Location:

For Help, press F1

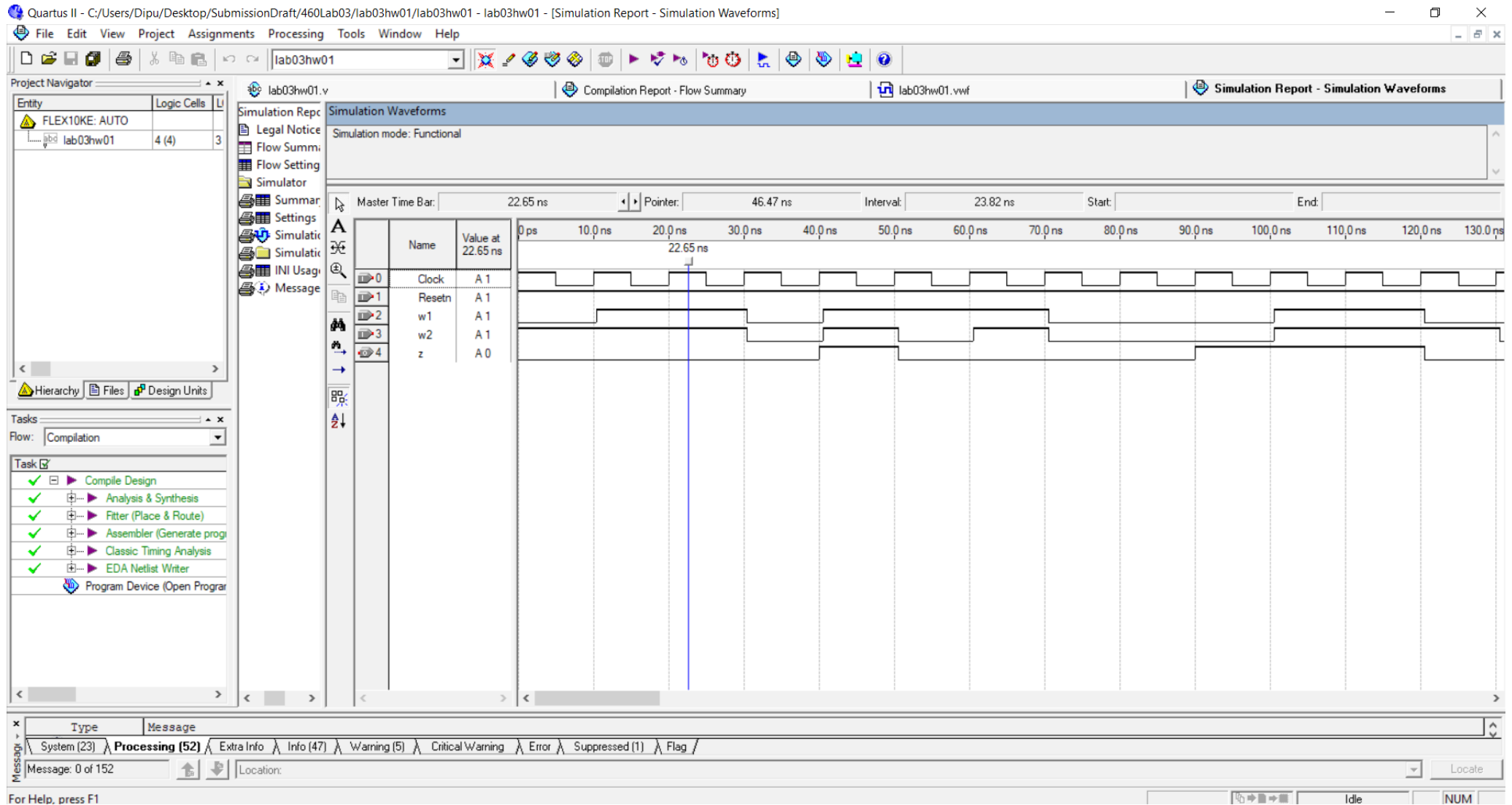
Ln 1, Col 44

Idle

NUM



## Homework 01 Vector Waveform



### **Homework 01 Discussion**

This sequential circuit acts as a Mealy Type Finite State Machine. It takes two inputs,  $w1$  &  $w2$ . And, then, it compares them using XOR operation. If the value of XOR operation is 0, that means on that particular clock cycle both inputs got matched, then it can proceed to next state other than Reset state A. If XOR operation provides a value of 1, that means inputs are not same on that clock cycle & we will have to get back to reset state.

If  $w1 = w2$  during any four consecutive clock cycles, then, this FSM provides an output value 1, otherwise 0. It can keep track of overlapping sequence & provides output accordingly.

A is the Reset state of this FSM. If Reset receives a value of 0, this FSM will go back to its Reset state.

## Homework 02 State Diagram

Home Work 02

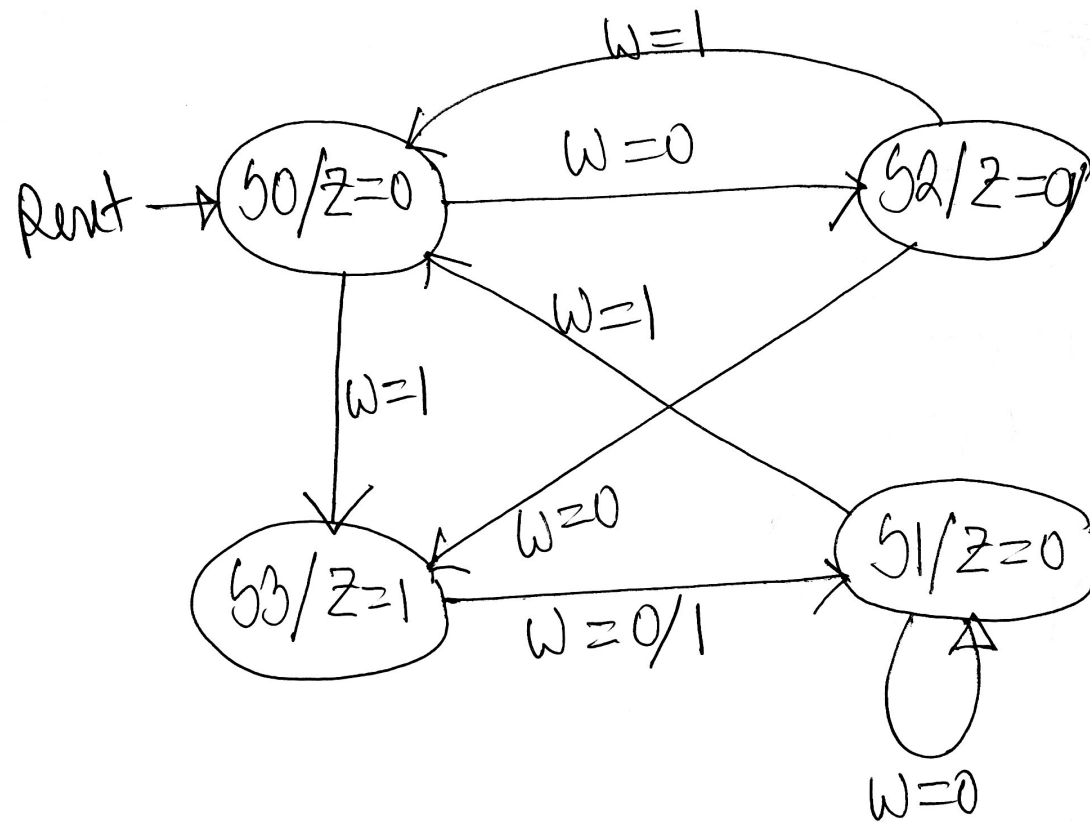


Fig: State Diagram.

## Homework 02 Verilog Code

Quartus II - C:/Users/Dipu/Desktop/SubmissionDraft/460Lab03/lab03hw02/lab03hw02 - lab03hw02 - [lab03hw02.v]

File Edit View Project Assignments Processing Tools Window Help

lab03hw02

lab03hw02.v

Compilation Report - Flow Summary

lab03hw02.vwf

Simulation Report - Simulation Waveforms

Entity Logic Cells U

FLEX10KE: AUTO

lab03hw02 3 (3) 3

Hierarchy Files Design Units

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Programmer)

```
1 module lab03hw02(Clock, Resetn, w, z);
2     input Clock, Resetn, w;
3     output z;
4     reg [2:1] y,Y;
5     parameter [2:1] s0=2'b00, s1=2'b01, s2=2'b10, s3=2'b11;
6
7     always @(w, y)
8     case (y)
9         s0 : if (w) Y = s3;
10            else Y = s2;
11        s1 : if (w) Y = s0;
12            else Y = s1;
13        s2 : if (w) Y = s0;
14            else Y = s3;
15        s3 : if (w) Y = s1;
16            else Y = s1;
17    endcase
18
19
20    always @(negedge Resetn, posedge Clock)
21        if (Resetn == 0) y <= s0;
22        else y <= Y;
23
24    assign z = (y == s3);
25
26 endmodule
```

267 266

ab/

Messages

Type Message

- Info: Using vector source file "C:/Users/Dipu/Desktop/SubmissionDraft/460Lab03/lab03hw02/lab03hw02.vwf"
- Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
- Info: Simulation partitioned into 1 sub-simulations
- Info: Simulation coverage is 88.89 %
- Info: Number of transitions in simulation is 1153
- Info: Quartus II Simulator was successful. 0 errors, 0 warnings

System (14) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag

Message: 0 of 16

Location:

Locate

For Help, press F1

Ln 1, Col 39

Idle

NUM

## Homework 02 Vector Waveform

Quartus II - C:/Users/Dipu/Desktop/SubmissionDraft/460Lab03/lab03hw02/lab03hw02 - [Simulation Report - Simulation Waveforms]

File Edit View Project Assignments Processing Tools Window Help

lab03hw02

Project Navigator

Entity	Logic Cells	U
FLEX10KE: AUTO		
lab03hw02	3 (3)	3

lab03hw02.v

Simulation Report - Flow Summary

Simulation Waveforms

Simulation mode: Functional

Master Time Bar: 22.0 ns Pointer: 125.13 ns Interval: 103.13 ns Start: End:

Name	Value
Clock	A 1
Resetrn	A 1
w	A 1
z	A 0

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate prog)
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Program)

Messages

System (14) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag

Message: 0 of 16

Location: Locate

For Help, press F1

Idle NUM

## Homework 02 Discussion

This FSM is a Moore Type FSM as outputs of this Machine depends only on the state of the circuit. Unlike Mealy, its output doesn't depend on the present values of inputs. S3 is the only accepting state of this Machine which will provide output 1, in other states, output will be 0.

If S0 receives 1 as input, it will go to S3, otherwise will go to S2. If S1 receives 1 as input, it will go to S0, otherwise will go to S1. If S2 receives 1 as input, it will go to S0, otherwise will go to S3. And, If S3 receives either 0 or 1 as input, it will go to only one state, S1.

S0 is the Reset state of this FSM. If Reset receives a value of 0, this FSM will go back to its Reset state.