Inspiring Excellence

CSE460

VLSI Design

Lab Assignment : 05

Layout Design On Microwind

Submitted By

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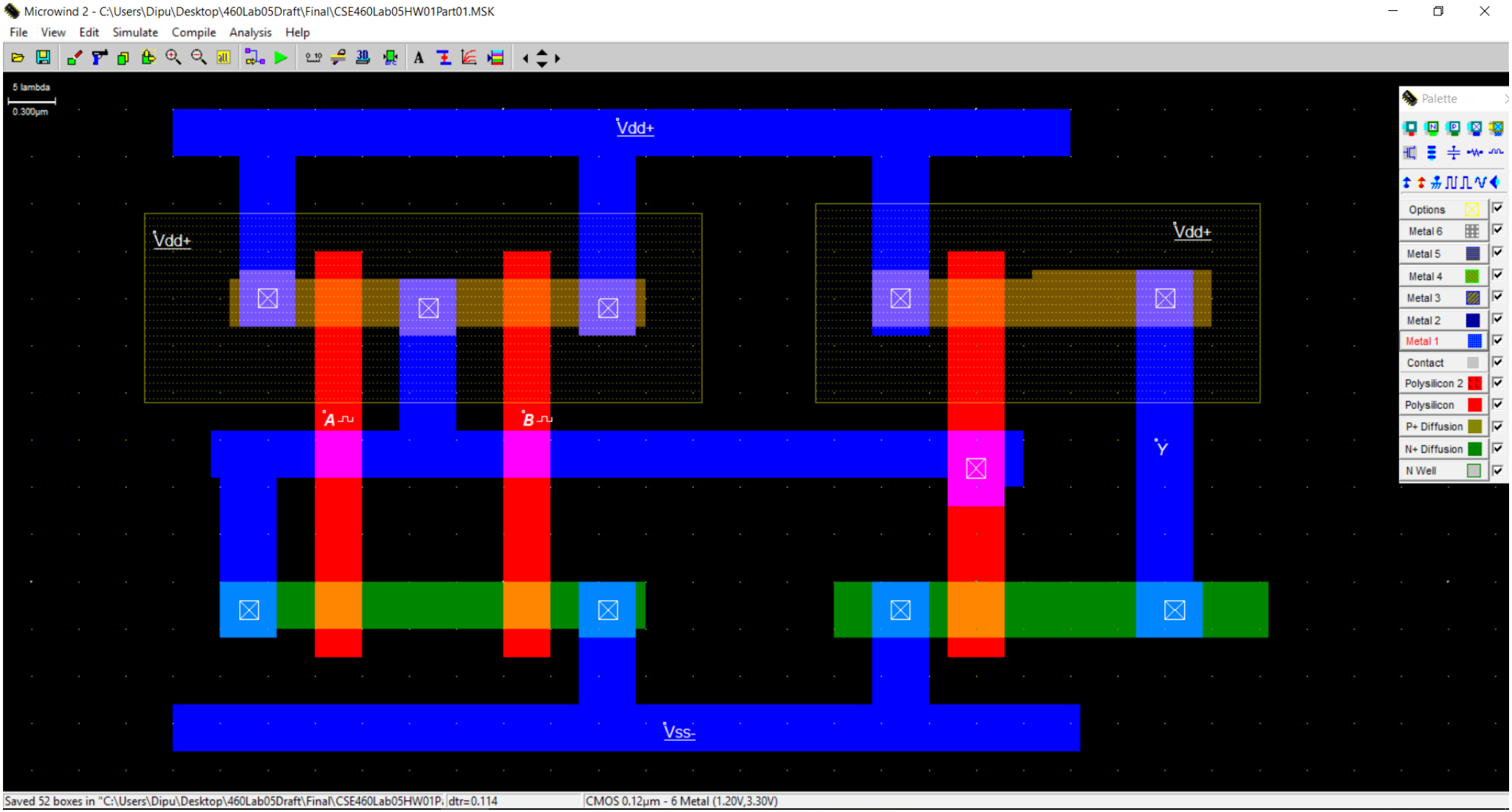
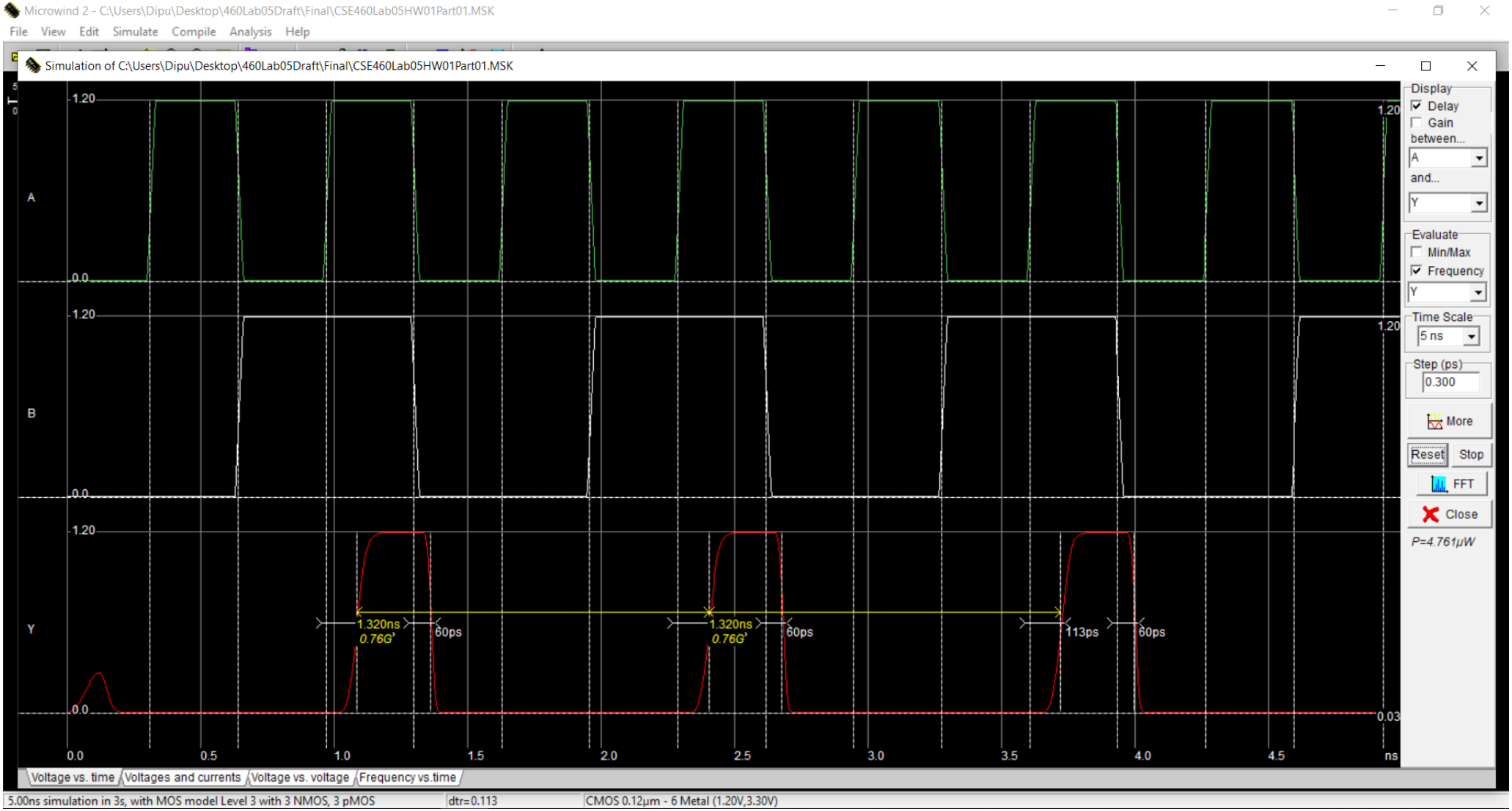
CSE460 Lab 05 Assignment
Home Work 01 Part 01 (CMOS AND) Layout



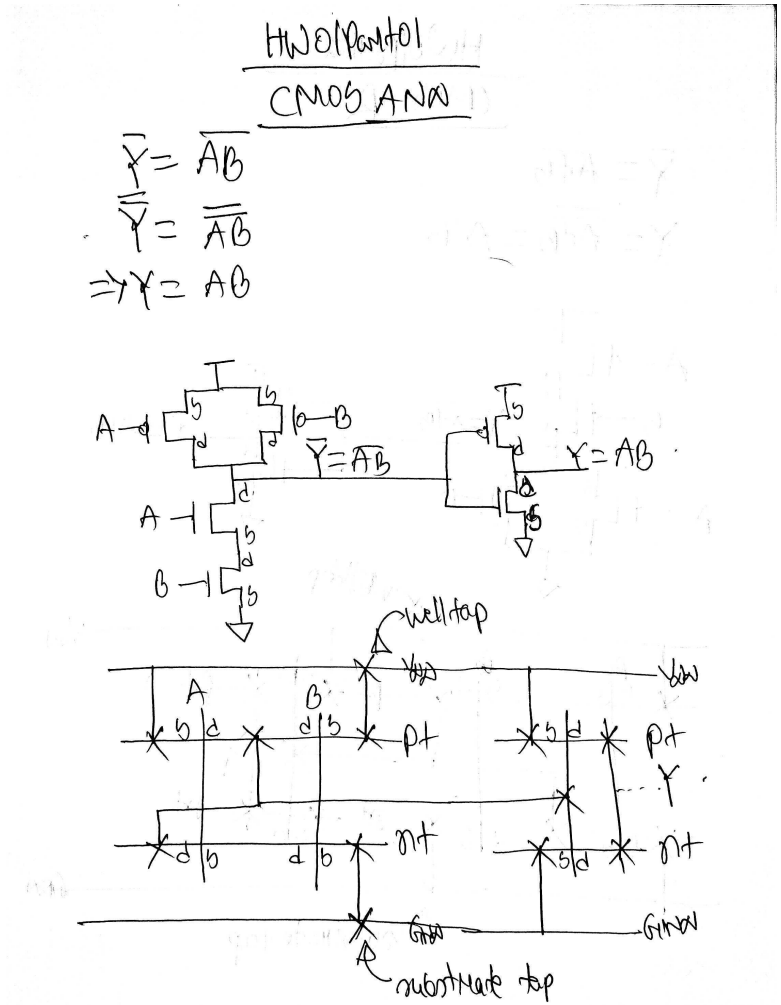
Home Work 01 Part 01 (CMOS AND) Timing Diagram



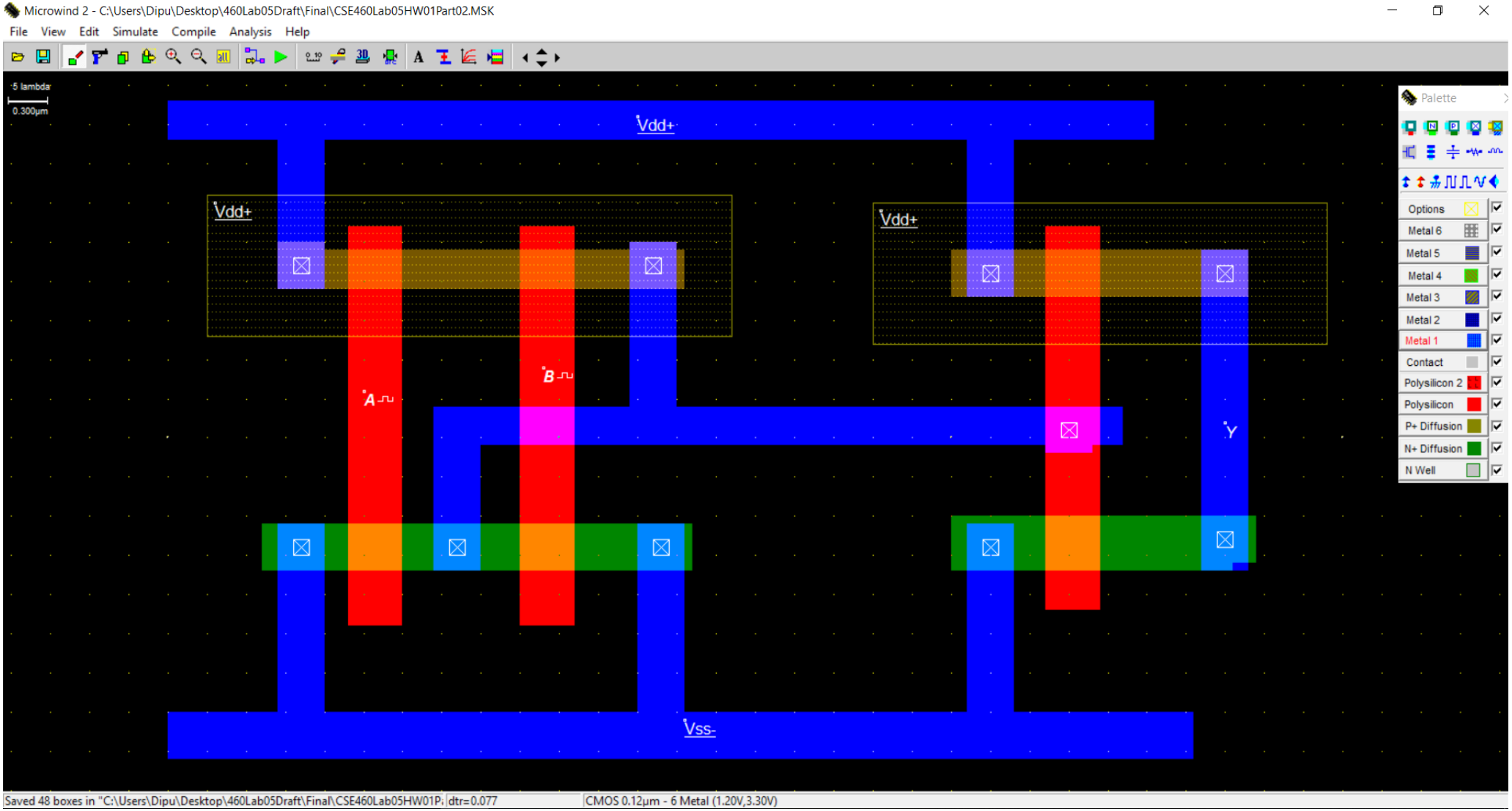
Home Work 01 Part 01 (CMOS AND) Output Explanation

It's a 2 Input CMOS AND gate. When both of the inputs, A & B will be at High Level, Output Y will be at High Level & vice versa.

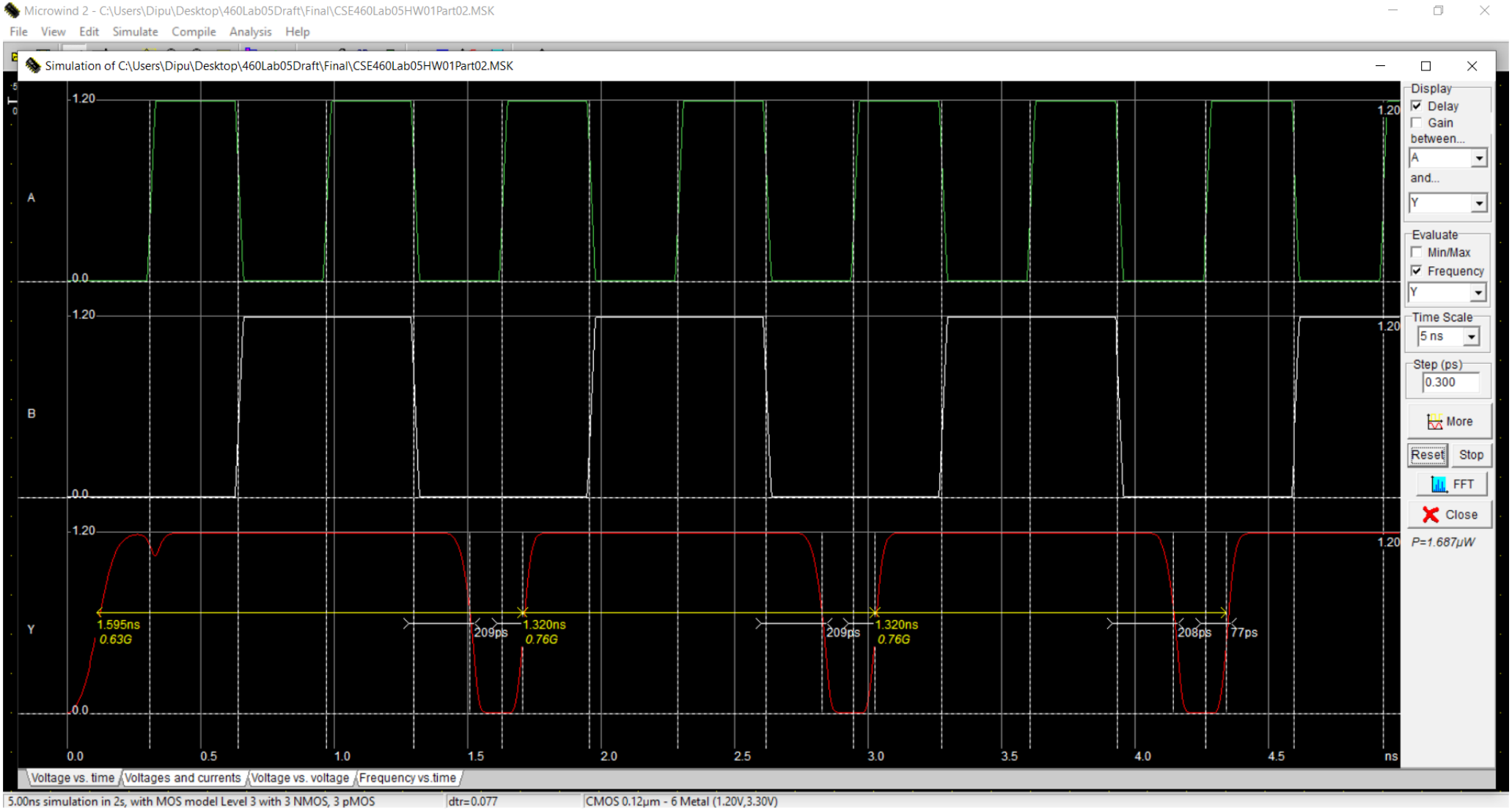
Home Work 01 Part 01 (CMOS AND) Discussion



Home Work 01 Part 02 (CMOS OR) Layout



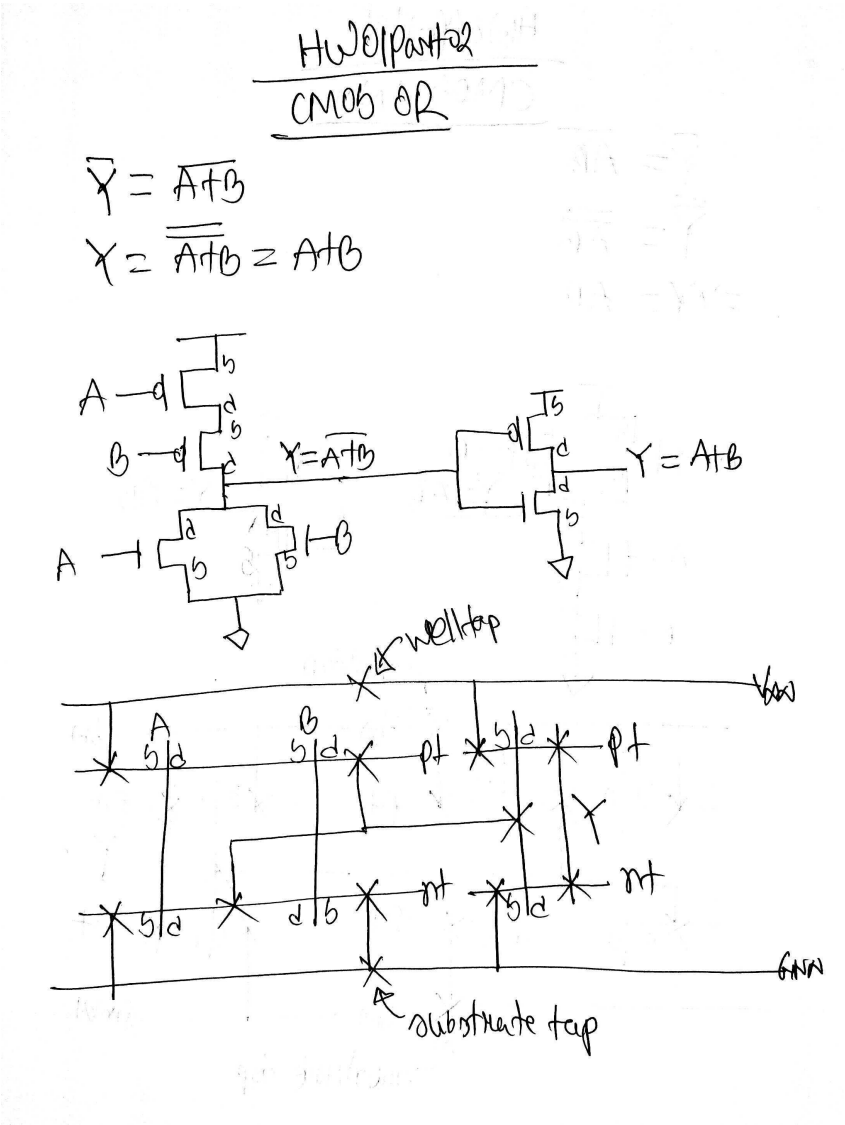
Home Work 01 Part 02 (CMOS OR) Timing Diagram



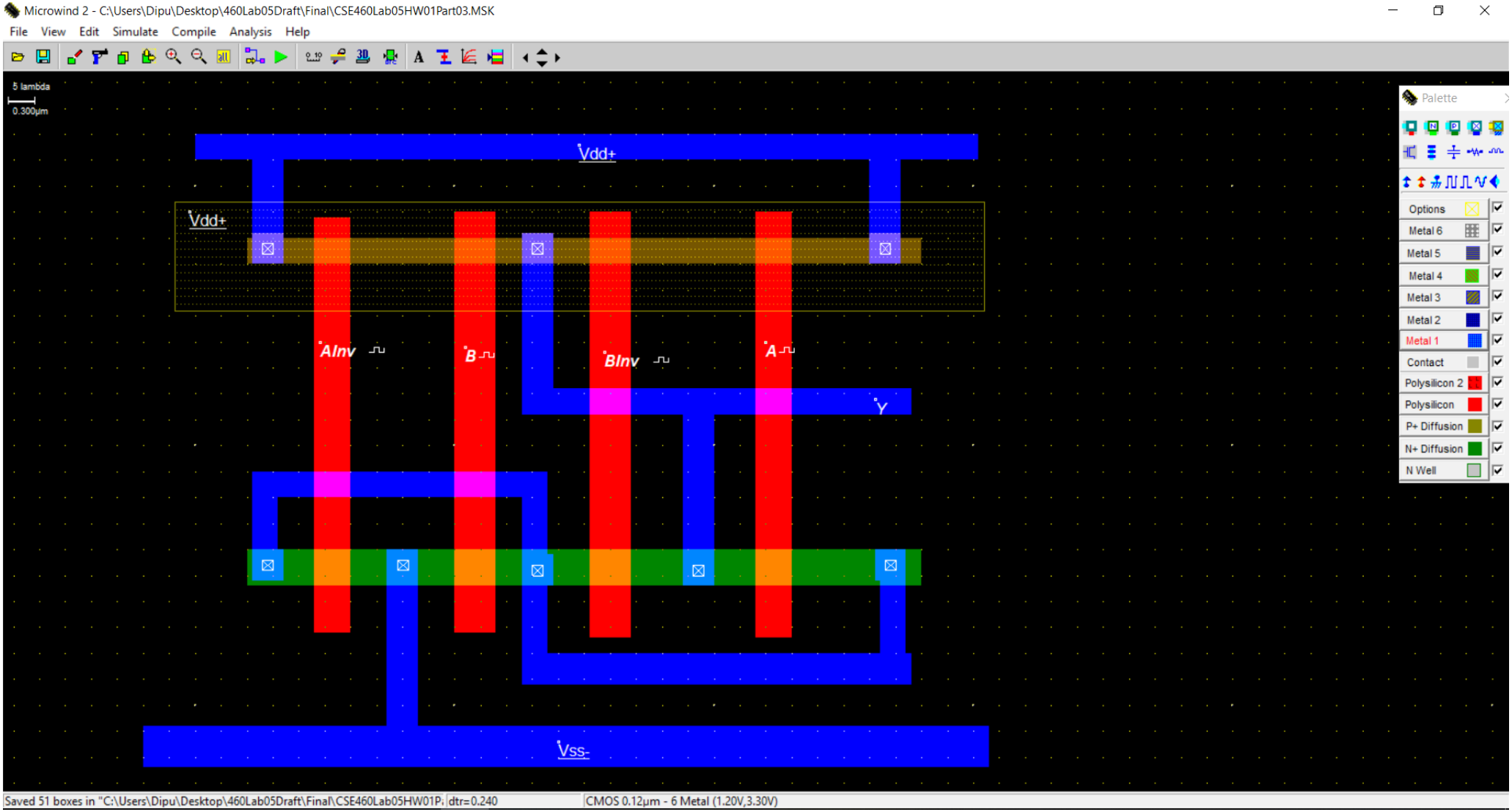
Home Work 01 Part 02 (CMOS OR) Output Explanation

It's a 2 Input CMOS OR gate. When any of the inputs or, both of the inputs, A or B or both will be at High Level, Output Y will be at High Level. When both of the inputs will be at Low Level, Output Y will be at Low Level.

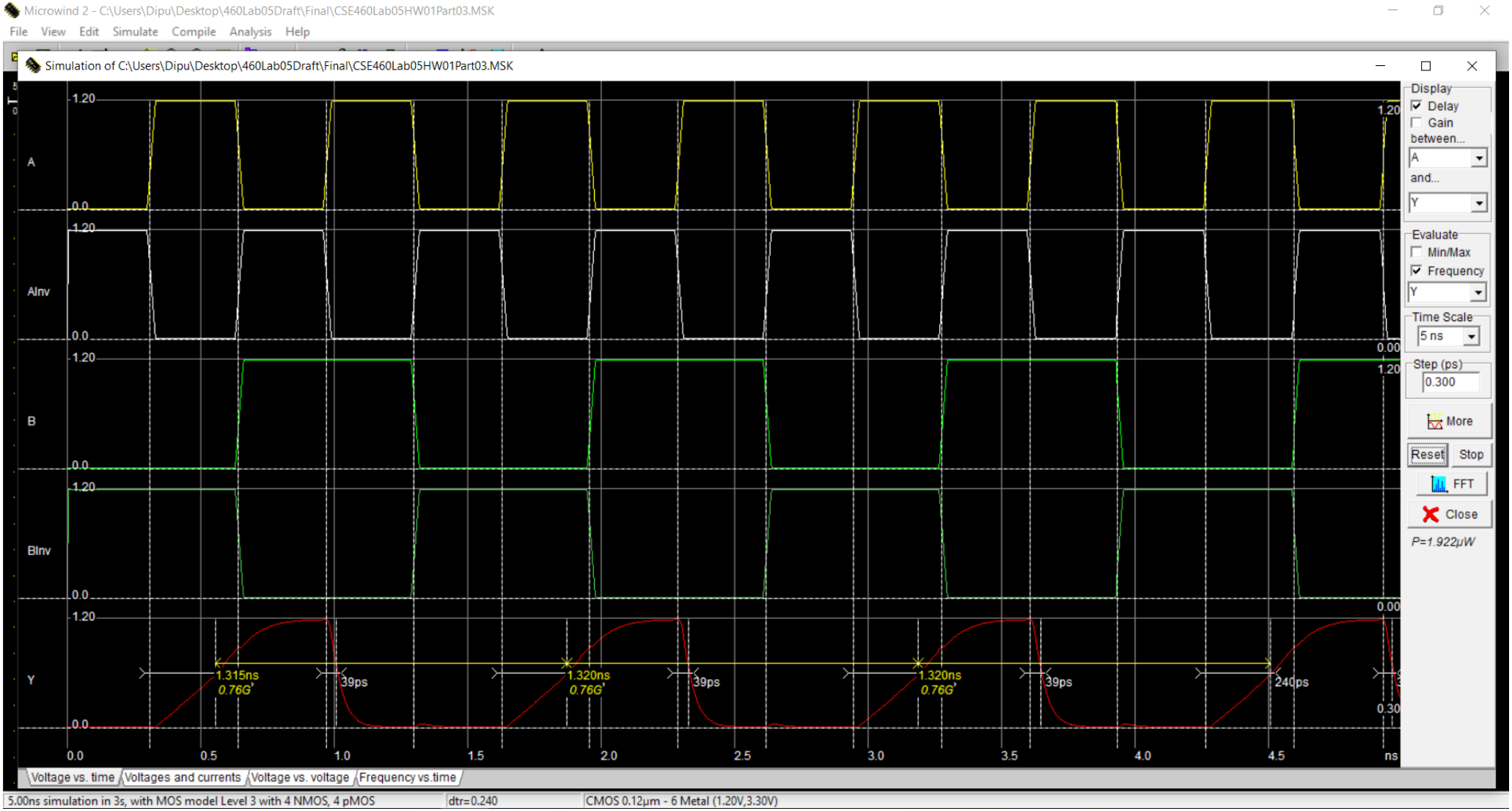
Home Work 01 Part 02 (CMOS OR) Discussion



Home Work 01 Part 03 (CMOS XOR) Layout



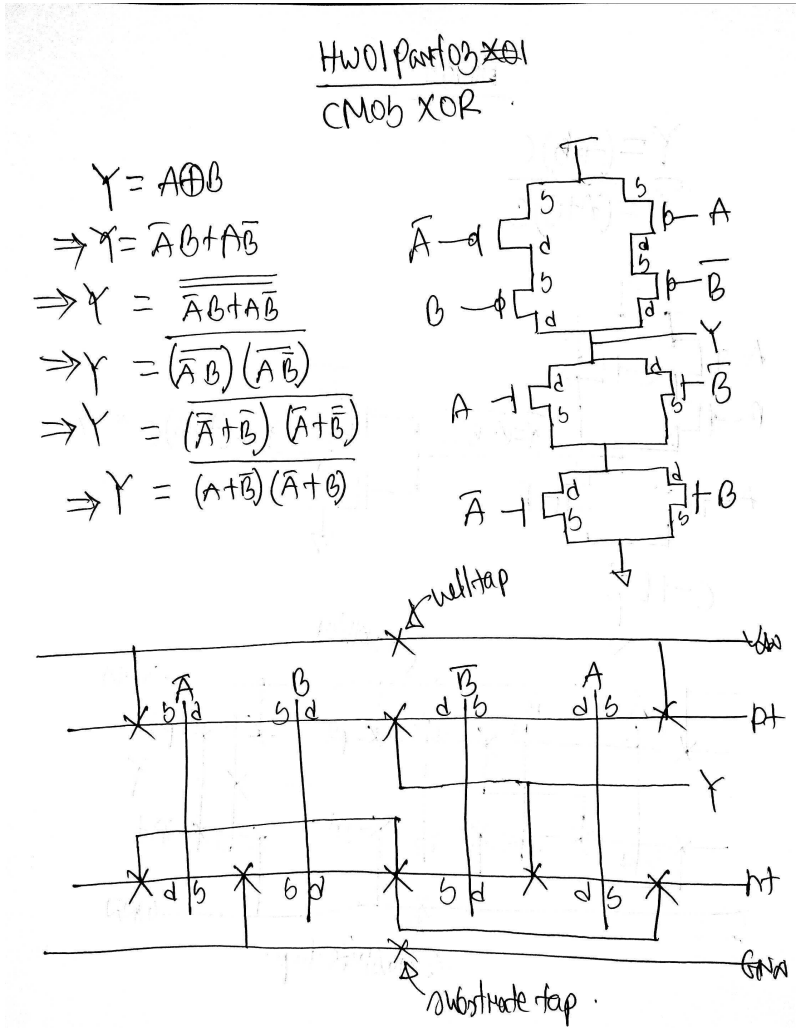
Home Work 01 Part 03 (CMOS XOR) Timing Diagram



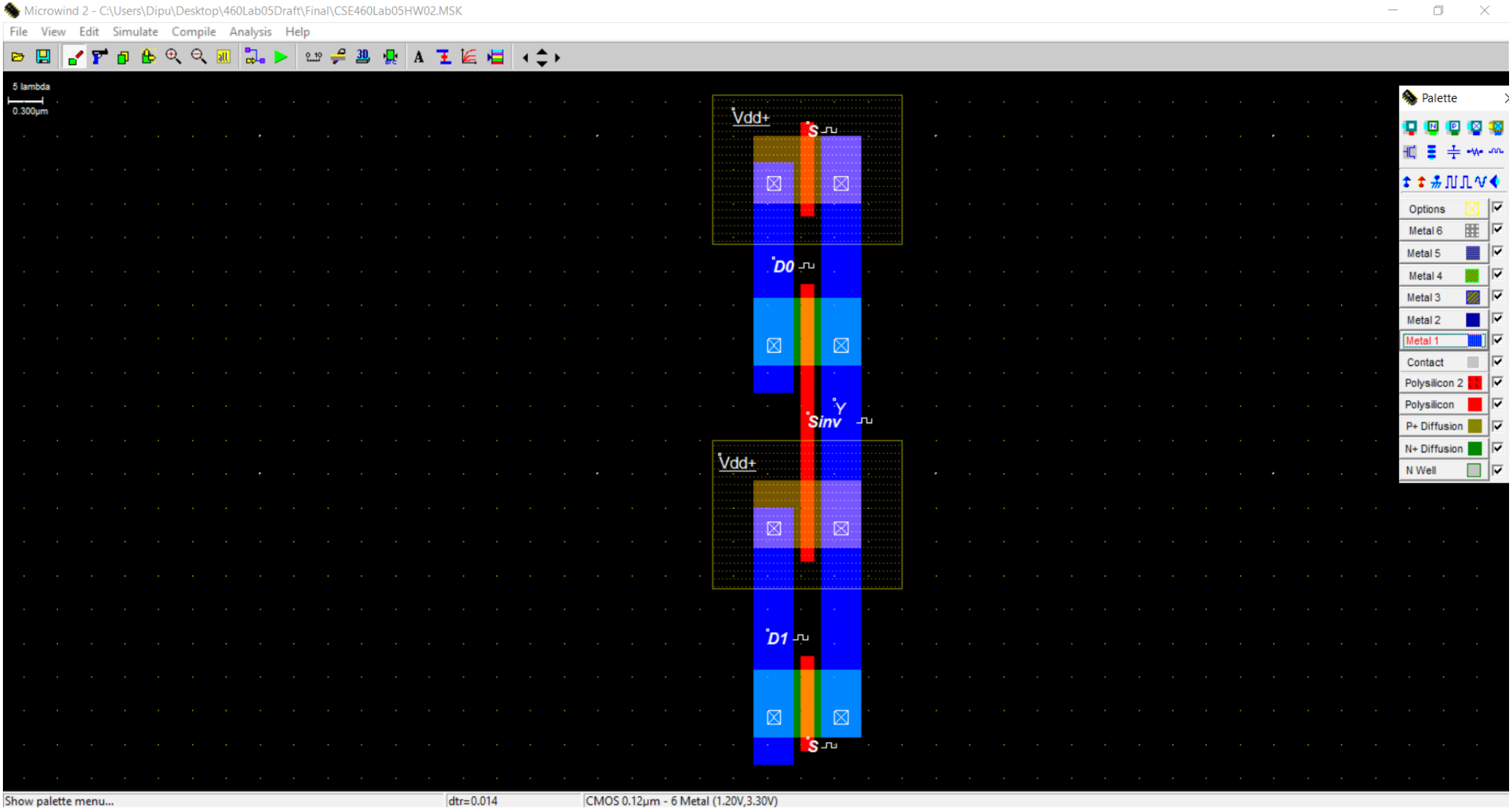
Home Work 01 Part 03 (CMOS XOR) Output Explanation

It's a 2 Input CMOS XOR gate. When both of the inputs, A & B will be at same level, either both of them at Low Level or both of them at High Level, output Y will be at Low Level. When the inputs will be at different level (A=High & B=Low or, A=Low & B=High), output Y will be at High Level.

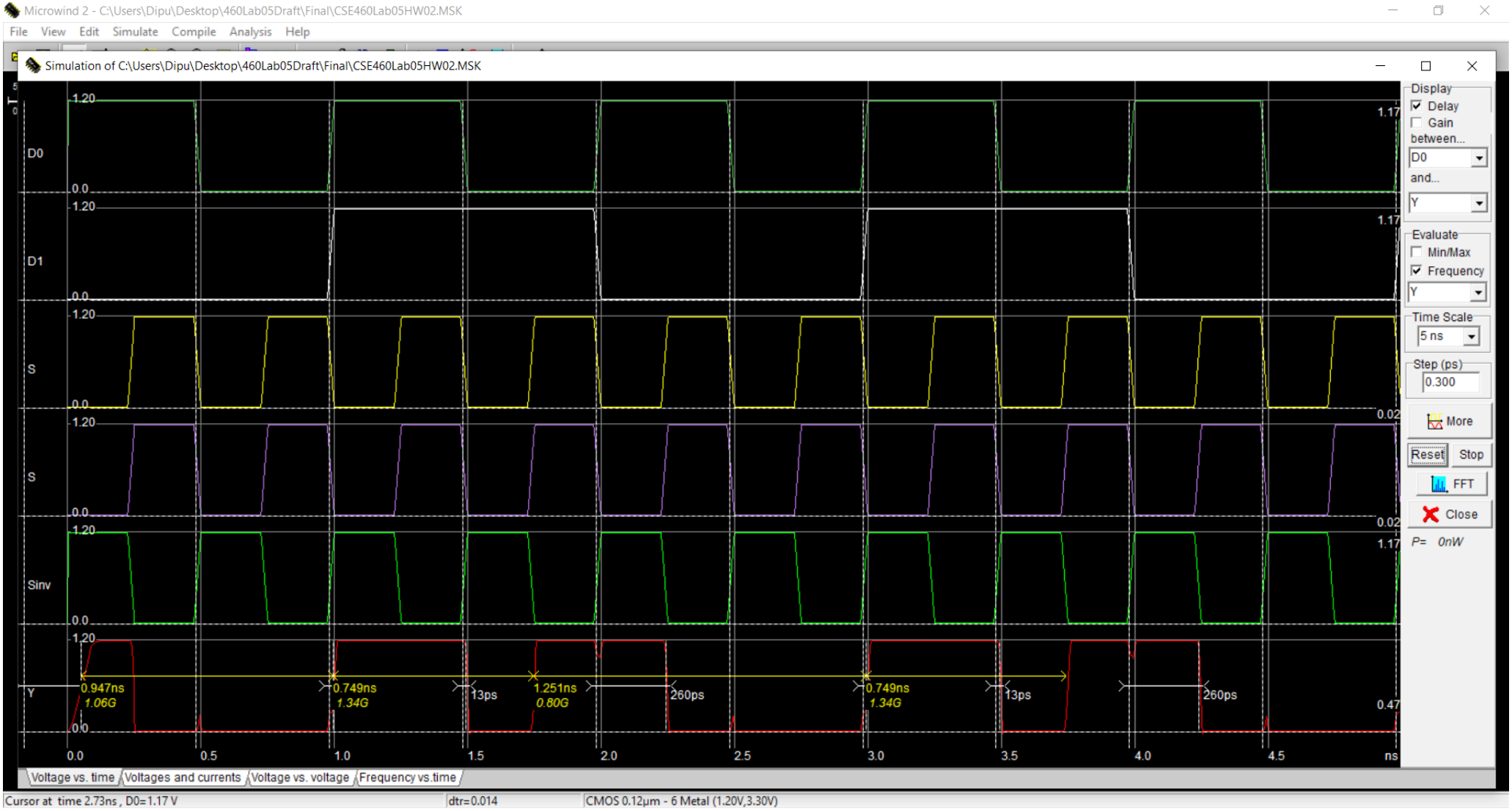
Home Work 01 Part 03 (CMOS XOR) Discussion



Home Work 02 CMOS 2 To 1 MUX Layout



Home Work 02 CMOS 2 To 1 MUX Timing Diagram



Home Work 02 CMOS 2 To 1 MUX Output Explanation

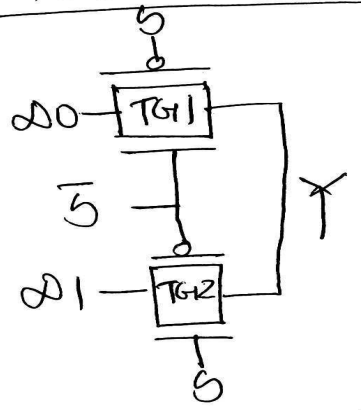
It's a 2 to 1 CMOS MUX. It has got 2 inputs : D0 & D1, got 1 selector S & output Y. It has been implemented using two CMOS Transmission Gates TG1 & TG2.

Home Work 02 CMOS 2 To 1 MUX Discussion

HW02

2 to 1 MUX using CMOS

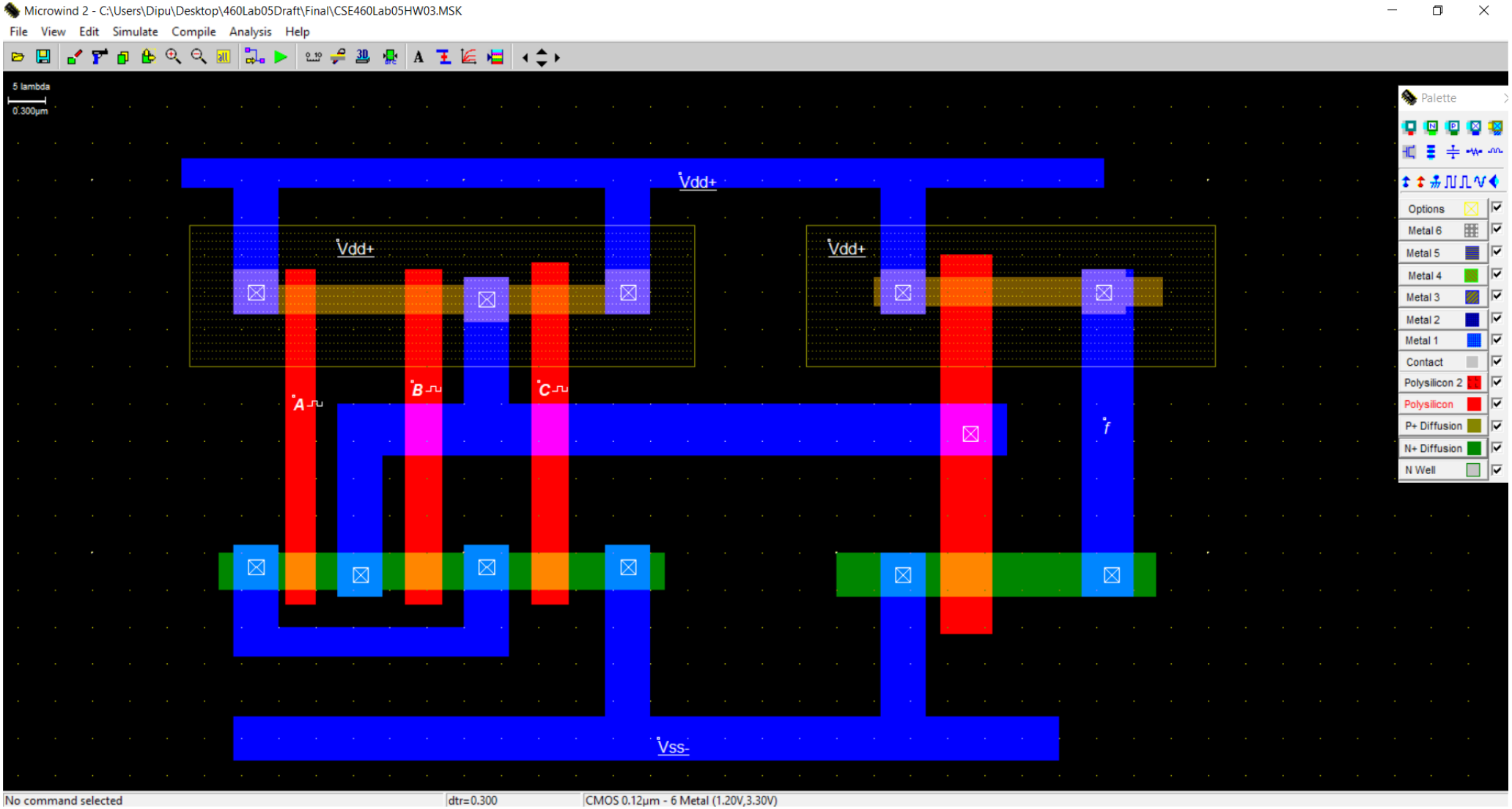
Selector, S.
input D0 & D1
Output Y.



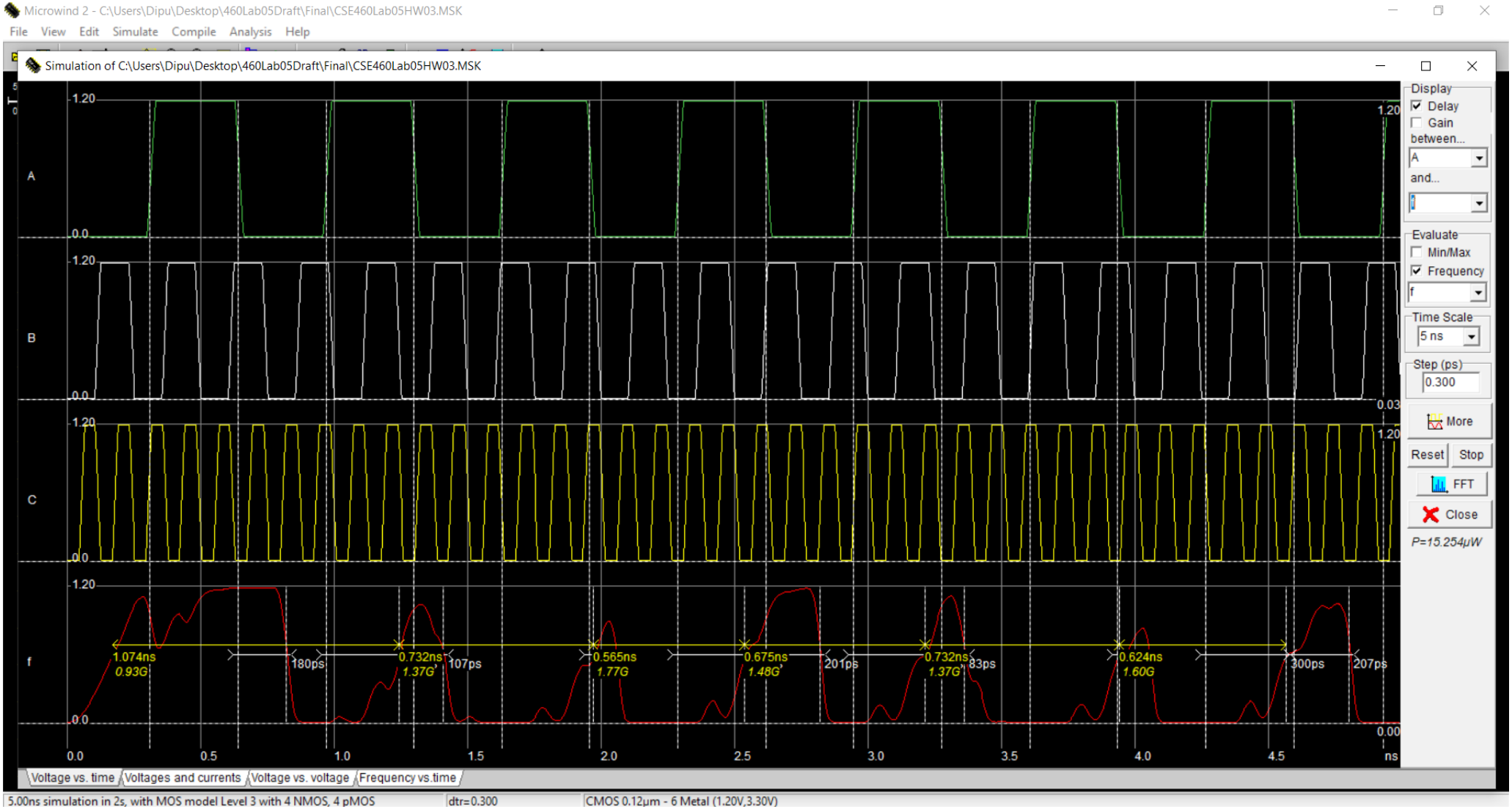
$Y = \bar{S}D0 + SD1$

S = 0		S = 1	
TG1	TG2	TG1	TG2
S=0, S̄=1 Both pMOS & nMOS will be off. D1 will not go to output.	S=0, S̄=1 S̄=1, nMOS will operate S=0, pMOS will operate D0 will appear at the output.	S=1, S̄=0 S=1, pMOS will not operate S=0, nMOS will also won't operate D0 will appear at output	S=1, S̄=0 S=1, nMOS will operate S=0, pMOS will operate D1 will appear at output.

Home Work 03 Layout



Home Work 03 Timing Diagram

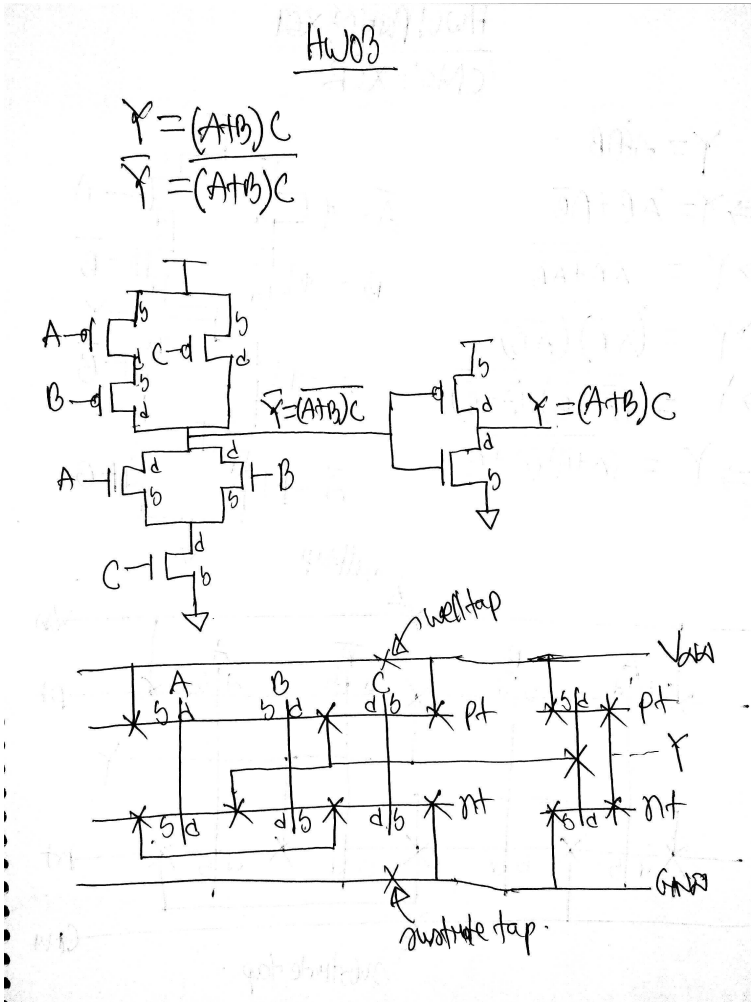


Home Work 03 Output Explanation

I have implemented this function using CMOS gates. It has got 3 different inputs A, B & C and 1 output f.

From both truth table & timing diagram we can get to know that, output will be at High Level for these 3 cases only :
I. A=Low, B=High, C=High
II. A=High, B=Low, C=High
III. A=High, B=High, C=High

Home Work 03 Discussion



Truth Tables

A	B	C	A+B	Y=(A+B)C
0	0	0	0	0
0	0	1	0	0
0	1	0	1	0
0	1	1	1	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	0
1	1	1	1	1

$Y = \bar{A}BC + A\bar{B}C + ABC$