7. a) Apply merge sort algorithm to sort the array A = [6, 5, 12, 10, 9, 1]. Show all intermediate steps at the time of sorting.

b) Derive the time complexity of the merge sort algorithm to sort a dataset of size n.

10+4=14

8. Write any **four** short notes: $3\frac{1}{2} \times 4 = 14$

a) Growth functions to measure the efficiency of an algorithm

b) Binary search versus linear search

c) Priority queue

d) Working principle of selection sorting

e) Different hash functions

f) Representation of graph

2018

COMPUTER APPLICATION

Paper : MCA-201

(Data Structure)

Full Marks : 70 Time : 3 Hours

The figures in the right-hand margin indicate marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answer wherever necessary.

Answer any **five** questions.

1. a) Suppose Q = A + (B × C – (D ÷ E ∧ F) × G) × H is an arithmetic expression written in infix notation. Find the equivalent postifix expression of Q using stack as an intermediate data structure.

   b) Compute the address of an element of an N-dimensional array. Let A[–1 : 1] [0:2] be a 2-dimensional array. The size of each element in A is a α bytes and the address of the element A[–1][0] is β. Calculate the address of the element. A[1][1]. 6+(6+2)=14

[Turn over]

2. a) Write an algorithm or a function to insert a node after a node pointed by pointer variable p into a linked list in memory.

   b) Implement the basic operations of stack using circular linked list.

   c) Two linked lists C_1 and C_2 are in memory, write an O(1) algorithm or a function to concatenate C_1 and C_2. 4+6+4=14

3. a) Design an algorithm or function to multiply two polynomials using linear linked list as an intermediate data structure.

   b) Write an algorithm or a function to insert an element into a sorted linear linked list in memory. 9+5=14

4. a) Write the merits of linked list representation of a binary tree.

   b) For any non-empty binary tree T, if n_0 is the number of terminal nodes and n_2 the number of nodes of degree 2, then prove that $n_0 = n_2+1$.

   c) Draw a tree, say T, corresponding to the infix expression Q = (2 × x + y) × (5 × a – b)^7. Now find the equivalent postifix expression and prefix expression of Q using T as an intermediate data structure.

head 1 → prev → next = head 2 → prev
head 2 → prev → next = head 1 → prev

d) Draw an almost complete binary tree which is not a strictly binary tree.

3+3+(2+4)+2=14

5. a) Write an iterative algorithm to search a particular element in a binary search tree (BST) in memory. Explain the number of comparisons required to search this element.

b) Write an algorithm that finds the elements of BST in sorted order.

c) Given a BST T and a value α, write an algorithm that reports the difference between α and its successor. If element α ∉ T, the BST will return false. (4+2)+3+5=14

6. a) Compute the minimum and maximum number of elements in a heap of height, *h*.

$2^{h+1}-1$

b) Which of the following arrays are heaps?

i) {8, 6, 4, 3, 2}

ii) {9, 4, 8, 3, 2, 5, 7}

iii) {7}

iv) {9, 4, 7, 2, 1, 6, 5, 3}

c) Write an algorithm to build a Heap.

4+4+6=14

c) Give the nomenclature justification of Trapezoidal formula for numerical integration. (4+3)+5+2=14

7. a) Find out the solution of the differential equation of the type $dy/dx = f(x, y)$ with the initial condition $y = y_1$ at $x = x_1$ by Eulers method and hence derive the condition of stability.

b) Apply Runge-Kutta second order method to compute an approximate solution of the following equation by this method: $dy/dx + xy = 0$, $y(0) = 1$ from $x = 0.0$ to 0.25 with step-value 0.05. (5+3)+6=14

8. Write short notes (any **four**): $3\frac{1}{2} \times 4 = 14$

a) Different numerical errors

b) Advantages and disadvantages of direct method to solve a system of linear equations

c) Ill conditioned equations

d) Numerical differentiation

e) Quadratic regression

f) Predictor-Corrector method

g) Runge-Kutta second order method

2(MCA) MCA-202/2nd Sem./Part-I/18

2018

COMPUTER APPLICATION

Paper : MCA-202

(Numerical and Statistical Computing)

Full Marks : 70 Time : 3 Hours

The figures in the right-hand margin indicate marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answer wherever necessary.

Answer any **five** questions.

1. a) Explain Bisection method to find a root, say α, of an equation $f(x) = 0$ and design an algorithm to find α.

   b) Use Bisection method to find a root of the equation $x^3 + 3x - 5 = 0$. The computed root must be correct up-to three significant digits.

(4+5)+5=14

2. a) Evaluating a polynomial $p(x) = a_n x^n + \ldots + a_2 x^2 + a_1 x^1 + a_0 x^0$ by a brute force technique is simple and this evaluation requires $\frac{n(n+1)}{2}$

[Turn over]

multiplications and n additions in worst case. Write an algorithm to evaluate p(x) where the number of multiplications is O(n).

b) Design the algorithm for Newton-Raphson method to find a root of an equation. Write several disadvantages of this method and explain each of them with the help of a diagram. 5+(6+3)=14

3. a) Write the working principle of Successive Approximations method to find a root of an equation.

b) Design an algorithm to solve a system of linear equations by Gauss Elimination method. 4+10=14

4. a) Use Gauss Elimination method to find the inverse of the following matrix:

$$\begin{pmatrix} 2 & 1 & 1 \\ 1 & 2 & 1 \\ 1 & 1 & 2 \end{pmatrix}.$$

b) How pivotal condensation technique is used to improve the efficiency of Gauss Elimination method? 10+4=14

5. a) Design an algorithm to compute the Lagrange interpolation polynomial of degreen n.

b) Given the following data, estimate $f(4.12)$ using interpolation:

i	0	1	2	3	4	5
x_i	0	1	2	3	4	5
$f(x_i)$	1	2	4	8	16	32

c) What are the advantages of Lagrange interpolation method over Newton-Gregory interpolation method? 6+5+3=14

6. a) Derive the linear regression formula of y on x where x and y are independent and dependent variables. Derive this linear regression formula for the following data:

x	y
2.1	50
3.6	61
3.9	62
4.0	63
4.1	65
4.5	67

b) Find the approximate value of $\int_0^6 x^2\,dx$ using any quadrature formula for numerical integration.

3(MCA) MCA-203/2nd Sem./Part-I/18

2018

COMPUTER APPLICATION

50

Paper : MCA-203

(Computer Origanization and Architecture)

Full Marks : 70 Time : 3 Hours

The figures in the right-hand margin indicate marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answer wherever necessary.

Answer **question 1** and any **four** from the rest.

1. Answer any **five** questions: 2×5=10

a) Distinguish between primary memory and secondary memory.

b) Represent the following signed 2's complement number in 8 bits: 1010.

c) How can the processor understand whether the data bus is carrying data or instruction?

d) How many bits are necessary to address a 8 MB byte addressable memory? 23

e) What is memory refreshing?

RAID Level 5

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Table 4 RAID Cor

Level	Advanta
0	I/O perfo by spreadi many cha No parity involved Very simp Easy to im
1	100% redu rebuild is r failure, jus disk Under cert 1 can susta drive failur Simplest R design

f) What is meant by locality of reference?

g) What is the major limitation of program-controlled I/O?

2. a) What is indexed addressing mode? Illustrate its use with an example assembly language program.

b) Write instructions sequences to compute $X = (P \div Q) \times (R - S) \times T)$ in one address and zero-address machines.

c) What are the steps in an instruction execution cycle? (1+5)+(3+3)+3

3. a) Assuming single-bus CPU organization, write the sequence of control steps showing the control signals to be active in each step for the following instructions:

i) ADD R1, R2 [R1 ← (R1) + (R2)]

ii) MUL R1, (R2) [(R2) ← (R1) × ((R2))]

Here R1 and R2 are two registers.

b) Explain what happens when the *End* control signal is generated.

c) Explain how a microprogrammed control unit works with the help of a flowchart.

(4+5)+2+4

Table 4 Continued

4. a) Represent the decimal values-86 and 59 as signed 8-bit binary numbers in the following number representations:

   i) signed magnitude

   ii) signed 1's complement

   iii) signed 2's complement

   b) Explain how overflow condition is checked during addition of two numbers in signed 2's complement representation.

   c) Write the flowchart of Booth's algorithm for multiplying two binary numbers in signed 2's complement representation. Also show step by step the multiplications of 24 × –18 using this algorithm. 2+2+(3+8)

5. a) Why is RAM called random access memory? Distinguish between static RAM and dynamic RAM.

   b) Draw the block diagram of a 64M×16 memory using 16K×8 memory chips.

   c) A 4-way set-associative cache consists of 64 lines. The main memory contains 4096 blocks, each consisting of 128 words.

   i) How many bits are there in the main memory address?

RAID Level 5

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Table 4 RAI...

Level	Adv...
0	I/O ... by s... man... No ... ... Ver... Eas...
1	100... rebu... fails... disk Und... I ca... drive Sim... desi...

ii) How many bits are there in each of the TAG, SET and OFFSET fields? (1+2)+6(1+5)

6. a) What is a write-through cache?

b) Consider the following block reference string: 0, 1, 2, 3, 0, 1, 4, 0, 1, 2, 3, 4. If the cache contains 4 lines organized in associative manner, how many misses will be there if the following block replacement algorithms are used?

i) FIFO

ii) LRU

c) Calculate the total time to transfer 8 words from main memory to cache memory after a cache read miss occurs. Assume that the main memory is organized as 4-module memory interleaving. Access time for main memory (1st word) = 8 cycles/word and access time for main memory (2nd to 8th word) = 4 cycles/word. Access/transfer time from main memory to cache = 1 cycle/word. Cache miss takes 2 cycles. 3+(4+4)+4

7. a) What do you mean by handshaking signals?

b) What is interrupt-driven I/O? Explain it using an example with respect to data transfer between a processor and a keyboard.

c) Write down the steps of how CPU serves an interrupt.

d) Explain how CPU initiates a DMA operation.

2+(2+4)+4+3

8. Write short notes on the following (any **three**):

5×3=15

a) Hardwired control unit

b) Nested subroutine call

c) Addressing modes

d) Determining the source of interrupt

e) Serial and parallel I/O interfaces

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b) Describe different 8-bit registers and their functions which are available in 8257 DMA controller. 6+4

7. a) Develop a software to store data to the Mem. Loc. 4200H from the accumulator whose content is 76H.

b) Use STAX to store data from Accumulator to the memory address 4500H.

c) Add two decimal numbers 25 and 78 and find the results in decimal form. 2+3+5

8. Write short notes on (any **two**): 5×2=10

a) Mode 5 of 8253

b) Cascading of 8259A

c) PUSH PSW

d) Instruction Register and Decoder in 8085up

4(MCA) MCA-204/2nd Sem./Part-I/18

2018

COMPUTER APPLICATION

Paper : MCA-204

(Microprocessor)

Full Marks : 70 Time : 3 Hours

The figures in the right-hand margin indicate marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer **Q.No. 1** and any **five** from the rest.

1. Answer any **ten** questions: 2×10=20

a) Why the size of a microprocessor is decreasing day by day?

b) What is the function of ALE pin of 8085 microprocessor?

c) The last address of a 16K byte memory space is $C23F_H$. Calculate the address of the first location.

d) Name the pins available in INTEL 8085 for serial data communication.

[Turn over]

RAID Level 5

RAID 5 is organized in a similar fashion to RAID 4. The difference is that RAID 5 dist...

e) Which type of addressing mode takes the least time? Justify your answer.

f) Write the name of interrupts of 8085 in order of priority.

g) What is the functions of AEN (address enable) signal in 8257 DMA controller?

h) What are the different flags in 8085 microprocessor? Mention their bit position in the flag register.

i) What is the role of ESMM bit in OCW_3 of Programmable Interrupt Controller?

j) Why port A of 8255 can only be used in bidirectional data transfer mode? What are the different handshaking signals used for that purpose?

k) Define: Instruction cycle.

l) What are the predefined conditions to be satisfied in case of synchronous data transfer mode?

2. a) What are the various ways of implementing stack in MPU? Discuss them with their advantages and disadvantages.

Table 4 R...

Level	
0	
1	

Table 4 Continued

b) Why limited number of GRPs can be used in MPU? 6+4

3. Explain the functions of following instructions of 8085: $2\frac{1}{2} \times 4 = 10$

i) RAR

ii) CALL addr

iii) DAD D

iv) $J_{condition}$ addr.

4. a) Why data transfer mode is necessary?

b) Draw the flowchart of DMA mode data transfer technique.

c) Mark the difference between cycle stealing DMA and block DMA data transfer mode. 2+5+3

5. a) Draw the timing diagram to execute the instruction IN <port...spit>.

b) Describe different components of non-programmable I/O port. 6+4

6. a) In how many modes a 8255A can be used? What is the purpose of its BSR mode? Describe how 8255 A can be used as input port in mode 1.