# LMO44L

- 20 Character x 4 lines
- Built-in control LSI HD44780 type (see page 23)
- +5V single power supply

## **MECHANICAL DATA (Nominal dimensions)**

Module size	$98W \times 60H \times 12D$ (max.) mm
Effective display area	76.0W x 25.2H mm
Character size ( $5 \times 7$ dots)	2.95W x 4.15H mm
Pitch	3.55 mm
Dot size	0.55W x 0.55H mm
Weight	about 65 g

max.
7.0 V
13.5 V
$V_{DD} V$
50°C
70°C

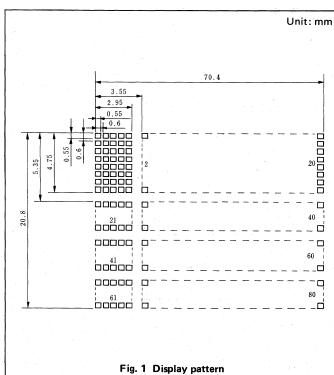
## **ELECTRICAL CHARACTERISTICS**

$Ta = 25^{\circ}C$ , $V_{DD} = 5.0 V \pm 0.25 V$
Input "high" voltage (Vi <sub>H</sub> ) 2.2 V min.
Input "low" voltage (Vi <sub>L</sub> ) 0.6 V max.
Output high voltage ( $V_{OH}$ ) ( $-I_{OH}$ = 0.2 mA) . 2.4 V min.
Output low voltage ( $V_{OL}$ ) ( $I_{OL} = 1.2 \text{ mA}$ ) 0.4 V max
Power supply current $(I_{DD})$ $(V_{DD} = 5.0 \text{ V})$ 1.0 mA typ.
3.5 mA max.
Person assembly faul CD daily (December 1) (V

Power supply for LCD drive (Recommended) (V<sub>DD</sub>-V<sub>O</sub>)
Du=1/16

at $Ta = 0$ °C	. 4.6 V typ.
at Ta = 25°C	. 4.4 V typ.
at $Ta = 50^{\circ}C$	4.2 V tvn

OPTICAL DATA ..... See page 8



## INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Fur	nction
1	V <sub>SS</sub>	_	0V	
2	V <sub>DD</sub>		+5V	Power supply
3	Vo	- ,	_	
4	RS	H/L	L: Instruction H: Data input	on code input it
5	R/W	H/L		l (LCD module→MPU) e (LCD module←MPU)
6	E	H, H→L	Enable signal	
7	DB0	H/L		
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L	Data bus line	
11	DB4	H/L	Note (1),	
12	DB5	H/L		
13	DB6	H/L	į.	*
14	DB7	H/L		

#### Note:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

- (1) When interface data is 4 bits long, data is transferred using only 4 buses of DB<sub>4</sub>~DB<sub>7</sub> and DB<sub>0</sub>~DB<sub>3</sub> are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB<sub>4</sub>~DB<sub>7</sub> when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB<sub>0</sub>~DB<sub>3</sub> when interface data is 8 bits long).
- (2) When interface data is 8 bits long, data is transferred using 8 data buses of DB<sub>0</sub>~DB<sub>7</sub>.

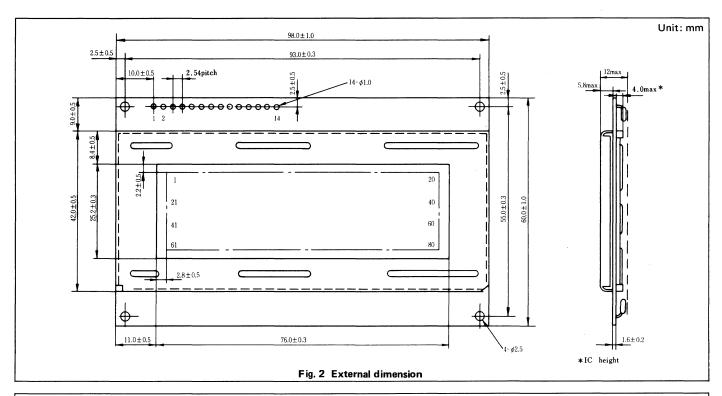
## **DISPLAY POSITION AND DD RAM ADDRESS**

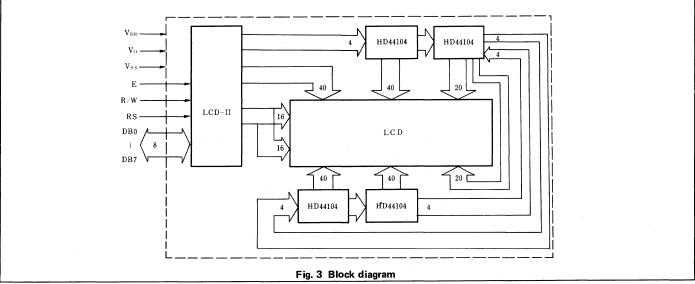
Character No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1st line	80	81	82	83	84	85	86	87	88	89	8A	88	8C	8D	8E	8F	90	91	92	93
2nd line	CO	C1	C2	СЗ	C4	C5	C6	C7	C8	С9	CA	СВ	СС	CD	CE	CF	D0	D1	D2	DS
3rd line	94	95	96	97	98	99	9A	9В	9C	9D	9E	9F	A0	A1	A2	А3	A4	A5	A6	A
4th line	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF	E0	E1	E2	E3	E4	E5	E6	E

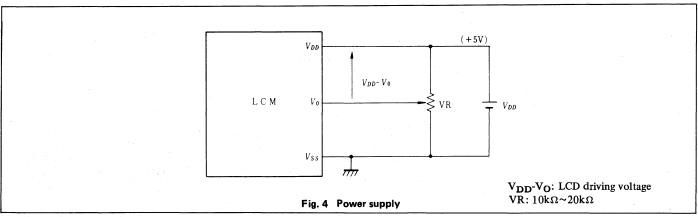
### Note:

- (1) 80 ~ E7 are described in hexidecimal for DD RAM address.
- (2) The set to HD44780 are "N = "1", F = "0" (2 lines 5 x 7 + cursol)."
- (3) DD RAM address is no series in line. Address set is necessary to change the lines.
- (4) Circuit is equal to 40 characters by 2 lines type.
- (5) In case of executing shift, first line and third line are shifted continuously, also second line and fourth line. Therefore it happens that display of third line is transfered to first line.









# TIMING CHARACTERISTICS

Item	Symbol	Test condition	min.	typ.	max.	Unit
Enable cycle time	t <sub>cyc</sub>	Fig. 5, Fig. 6	1.0		-	μs
Enable pulse width	P <sub>wEH</sub>	Fig. 5, Fig. 6	450	_	-	ns
Enable rise/fall time	t <sub>Er</sub> , t <sub>Ef</sub>	Fig. 5, Fig. 6	_	-	25	ns
RS, R/W set up time	t <sub>AS</sub>	Fig. 5, Fig. 6	140	_	-	ns
Data delay time	t <sub>DDR</sub>	Fig. 6		-	320	ns
Data set up time	t <sub>DSW</sub>	Fig. 5	195	-	_	ns
Hold time	t <sub>H</sub>	Fig. 5, Fig. 6	20	_	_	ns

