Technical Report

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# Introduction

The basic functionality of this application is a Sobel filter for edge detection in images. They are on two implementations: single core hardware design that is running a RTOS, and, five core bare metal hardware design. The design constraints considered here are as below:

For a 32x32 pixel image

* Throughput > 320 images/sec
* Throughput > 200 images/sec with total code size <= 45kB

The application is implemented on Altera Nios II FPGA hardware.

# Specification

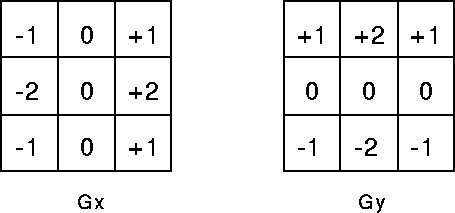
## Sobel Filter Application

Sobel filter algorithm is used in image edge detection by emphasizing it. This algorithm is a mathematical based as below:

* GrayScale – The 32x32 pixel image is first converted into a grayscale image. Each RGB value of a pixel is converted into a single gray value.
* Resize Image – The grayed image is then resized by to half 16x16 pixel image. Each pixel value is calculated by averaging the 4 pixels into one value.

In this process, the maximum and minimum value of a pixel in also identified as

* Correct Image – The values of maximum and minimum brightness show that pixel values in the image have a very small range. Correctness is applied to expand this range into [0,255].
* Sobel Filter – After correcting the image, Sobel filter is applied to the image. Convolution of the image with Gx and Gy is done. The modulo of the values obtained are added to get the final pixel value. Each pixel values obtained here are divided by 128 to get a value from [0,15] so as to fit in the ASCII value range.



* ASCII Values – The output of sobel is an image’s pixel value with values ranging from [0,15]. This is mapped onto an ASCII level array and the printed on the console. This is where the edge detected is highlighted.

The complete application is implemented using the above equations. Application flow is formally represented using Synchronous Data Flow (SDF) as shown in Fig 1.

­­­­­­­­­­A close up of a map

Description automatically generated

Fig. 1. Application SDF

SDF shows the data dependencies between actors, the expected input data and output data. The Actors also show which processes/functions can be implemented in parallel, as well as deadlocks can be identified. Hence, identifying concurrency is easy, which is needed in multiprocessor architecture.

In the case of our application, example of concurrency is graySDF in which all the multiple rows can be processed independently, and hence in parallel.

The SDF as shown in diagram1 is how the single core bare metal and single core RTOS algorithm is implemented. For single core RTOS, TODO. Actor/Pattern mapped to C code, kernel objects,

For 5 core bare metal design, TODO software

## Altera Nios II FPGA Hardware

The interconnection network here is Altera Avalon Switch Fabric. Multi Core TODO. Each processor communicates like this. Shred meme etc.

# Results and Discussion

The implementations work in two modes: Debug and Performance mode. Debug mode processes the images once and shows their corresponding edge output in ASCII. Performance mode processes the images 32 times and shows the performance metrics such as number of images executed, total execution time, execution time per image, throughput in images per sec.

The table 1 shows the comparison between single core bare metal, single core RTOS and five core bare metal design.

TABLE I.

# Result of the three different Implementations

| Implementations | Measures | | |
| --- | --- | --- | --- |
| Throughput | Code Size |
| Single Core Bare Metal |  |  |
| Single core RTOS |  |  |
| Five core Bare Metal |  |  |

Scheduling diagram for five core bare metal design is as follows:

# Appendix

For the initial project work, both Prabir and Nakita worked together on understanding the provided Sobel filter specification written in Haskell-ForSyDe. Further, they worked on developing a basic flow chart on how the Sobel filter is to be implemented. Then, an SDF graph for the algorithm was developed.

Development and implementation of the software for single core and multicore was done together by Prabir and Nakita. Prabir primarily worked on developing the hardware design for the implementations with Nakita as a secondary on it, while Nakita developed a tool to convert images into arrays directly for ease of testing. Troubleshooting and result analysis was done by both Prabir and Nakita together.

Nakita worked on creating the project report with incorporating the developments in the project on weekly basis. Prabir reviewed the report and, any modifications needed were discussed and updated.

##### References

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