Technical Report

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# Introduction

The basic functionality of this application is a Sobel filter for edge detection in images. They are on two implementations: single core hardware design that is running a RTOS, and, five core bare metal hardware design. The design constraints considered here are as below:

For a 32x32 pixel image

* Throughput > 320 images/sec
* Throughput > 200 images/sec with total code size <= 45kB

The application is implemented on Altera Nios II FPGA hardware.

# Specification

## Sobel Filter Application

Sobel filter algorithm is used in image edge detection by emphasizing it. This algorithm is a mathematical based as below:

The complete application is implemented using the above equations. Application flow is formally represented using Synchronous Data Flow (SDF) as shown in Fig 1.

­­­­­­­­­­A close up of a map

Description automatically generated

Fig. 1. Application SDF

* graySDF:
* resizeSDF, brightnessSDF, correctSDF:
* sobelSDF:
* asciiSDF:
* nsSDF:
* odSDF:

The reason for using SDF as method of formal modeling is because SDF shows the data dependencies between actors,

the expected input data and output data. The Actors also show which processes/functions can be implemented in parallel, as well as deadlocks can be identified. Hence, identifying concurrency is easy, which is needed in multiprocessor architecture.

In the case of our application, example of concurrency is graySDF in which all the pixels can be processed independently, and hence in parallel.

The SDF as shown in diagram1 is how the single core bare metal and single core RTOS algorithm is implemented. For single core RTOS, TODO. Actor/Pattern mapped to C code, kernel objects,

For 5 core bare metal design, TODO software

## Altera Nios II FPGA Hardware

The interconnection network here is Altera Avalon Switch Fabric. Multi Core TODO. Each processor communicates like this. Shred meme etc.

# Results and Discussion

The table 1 shows the comparison between single core bare metal, single core RTOS and five core bare metal design.

TABLE I.

# Result of the three different Implementations

| Implementations | Measures | | |
| --- | --- | --- | --- |
| Throughput | Code Size |
| Single Core Bare Metal |  |  |
| Single core RTOS |  |  |
| Five core Bare Metal |  |  |

Scheduling diagram for five core bare metal design is as follows:

# Appendix

For the initial project work, both Prabir and Nakita worked together on understanding the provided Sobel filter specification written in Haskell-ForSyDe. Further, they worked on developing a basic flow chart on how the Sobel filter is to be implemented. Then, an SDF graph for the algorithm was developed.

Development and implementation of the software for single core and multicore was done together by Prabir and Nakita. Prabir primarily worked on developing the hardware design for the implementations with Nakita as a secondary on it, while Nakita developed a tool to convert images into arrays directly for ease of testing. Troubleshooting and result analysis was done by both Prabir and Nakita together.

Nakita worked on creating the project report with incorporating the developments in the project on weekly basis. Prabir reviewed the report and, any modifications needed were discussed and updated.

##### References

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