

## DM7408

### Quad 2-Input AND Gates

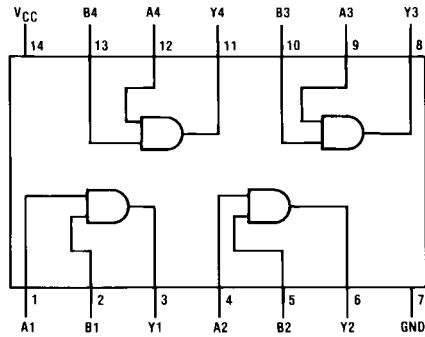
#### General Description

This device contains four independent gates each of which performs the logic AND function.

#### Ordering Code:

Order Number	Package Number	Package Description
DM7408N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

#### Connection Diagram



#### Function Table

$$Y = AB$$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Logic Level  
L = LOW Logic Level

**Absolute Maximum Ratings**(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
$V_{CC}$	Supply Voltage	4.75	5	5.25	V
$V_{IH}$	HIGH Level Input Voltage	2			V
$V_{IL}$	LOW Level Input Voltage			0.8	V
$I_{OH}$	HIGH Level Output Current			–0.8	mA
$I_{OL}$	LOW Level Output Current			16	mA
$T_A$	Free Air Operating Temperature	0		70	°C

**Electrical Characteristics**

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
$V_I$	Input Clamp Voltage	$V_{CC} = \text{Min}$ , $I_I = -12 \text{ mA}$			–1.5	V
$V_{OH}$	HIGH Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OH} = \text{Max}$ $V_{IL} = \text{Max}$	2.4	3.4		V
$V_{OL}$	LOW Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OL} = \text{Max}$ $V_{IH} = \text{Min}$		0.2	0.4	V
$I_I$	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$ , $V_I = 5.5 \text{ V}$			1	mA
$I_{IH}$	HIGH Level Input Current	$V_{CC} = \text{Max}$ , $V_I = 2.4 \text{ V}$			40	μA
$I_{IL}$	LOW Level Input Current	$V_{CC} = \text{Max}$ , $V_I = 0.4 \text{ V}$			–1.6	mA
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 3)	–18		–55	mA
$I_{CCH}$	Supply Current with Outputs HIGH	$V_{CC} = \text{Max}$		11	21	mA
$I_{CCL}$	Supply Current with Outputs LOW	$V_{CC} = \text{Max}$		20	33	mA

**Note 2:** All typicals are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

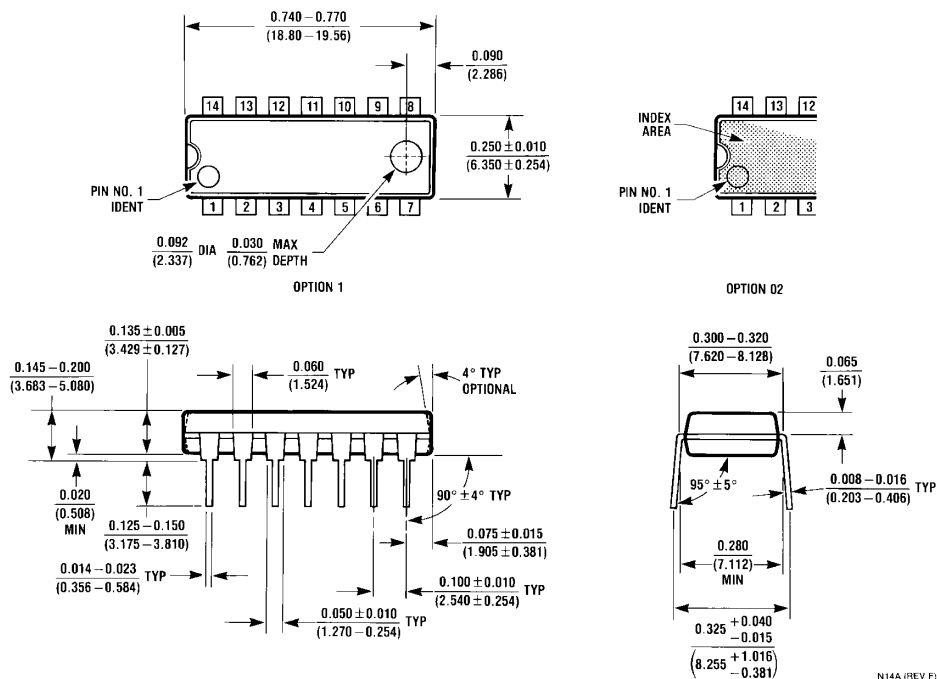
**Note 3:** Not more than one output should be shorted at a time.

**Switching Characteristics**

at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$

Symbol	Parameter	Conditions	Min	Max	Units
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	$C_L = 15 \text{ pF}$ $R_L = 400\Omega$		27	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output			19	ns

# Physical Dimensions inches (millimeters) unless otherwise noted



**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N14A**

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## DM7404

### Hex Inverting Gates

#### General Description

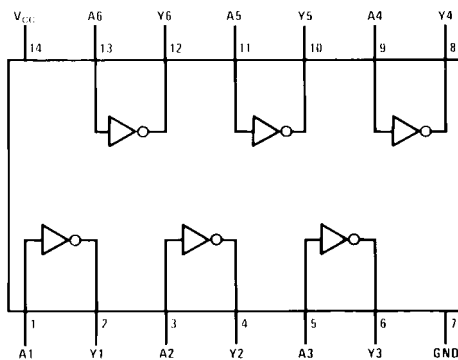
This device contains six independent gates each of which performs the logic INVERT function.

#### Ordering Code:

Order Number	Package Number	Package Description
DM7404M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM7404N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Connection Diagram



#### Function Table

$$Y = \overline{A}$$

Inputs	Output
A	Y
L	H
H	L

H = HIGH Logic Level  
L = LOW Logic Level

**Absolute Maximum Ratings**(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
V <sub>CC</sub>	Supply Voltage	4.75	5	5.25	V
V <sub>IH</sub>	HIGH Level Input Voltage	2			V
V <sub>IL</sub>	LOW Level Input Voltage			0.8	V
I <sub>OH</sub>	HIGH Level Output Current			–0.4	mA
I <sub>OL</sub>	LOW Level Output Current			16	mA
T <sub>A</sub>	Free Air Operating Temperature	0		70	°C

**Electrical Characteristics**

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = –12 mA			–1.5	V
V <sub>OH</sub>	HIGH Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max V <sub>IL</sub> = Max	2.4	3.4		V
V <sub>OL</sub>	LOW Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max V <sub>IH</sub> = Min		0.2	0.4	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V			1	mA
I <sub>IH</sub>	HIGH Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.4V			40	μA
I <sub>IL</sub>	LOW Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V			–1.6	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 3)	–18		–55	mA
I <sub>CCH</sub>	Supply Current with Outputs HIGH	V <sub>CC</sub> = Max		6	12	mA
I <sub>CCL</sub>	Supply Current with Outputs LOW	V <sub>CC</sub> = Max		18	33	mA

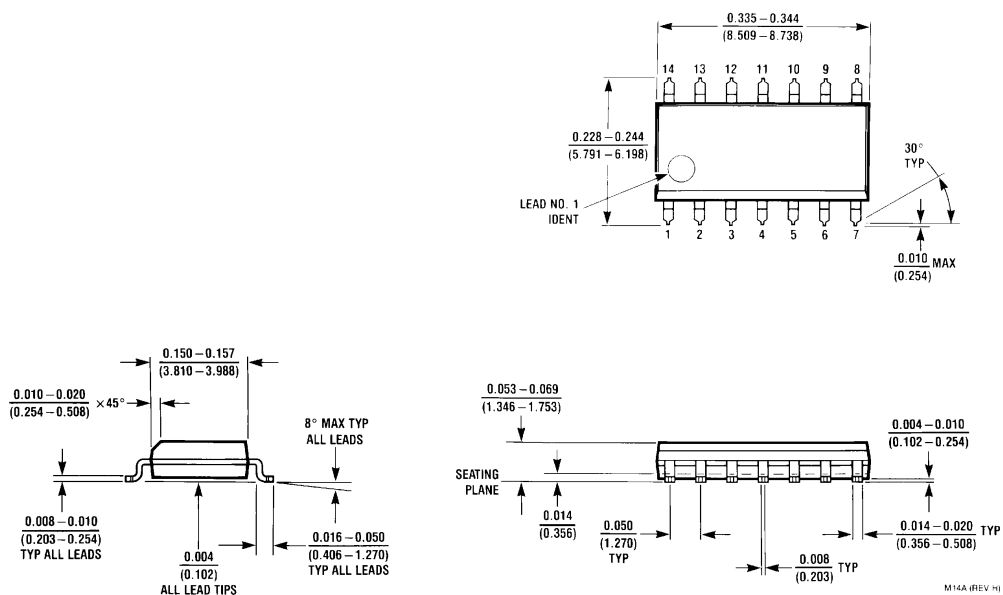
**Note 2:** All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

**Note 3:** Not more than one output should be shorted at a time.

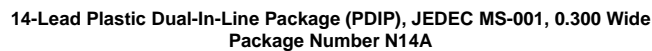
**Switching Characteristics**

at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C

Symbol	Parameter	Conditions	Min	Max	Units
t <sub>PLH</sub>	Propagation Delay Time LOW-to-HIGH Level Output	C <sub>L</sub> = 15 pF R <sub>L</sub> = 400Ω		22	ns
t <sub>PHL</sub>	Propagation Delay Time HIGH-to-LOW Level Output			15	ns



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow  
Package Number M14A**



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## DM7402

### Quad 2-Input NOR Gates

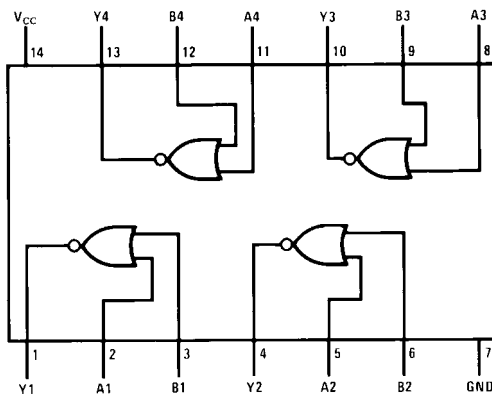
#### General Description

This device contains four independent gates each of which performs the logic NOR function.

#### Ordering Code:

Order Number	Package Number	Package Description
DM7402N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

#### Connection Diagram



#### Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH Logic Level  
L = LOW Logic Level



**Absolute Maximum Ratings**(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
V <sub>CC</sub>	Supply Voltage	4.75	5	5.25	V
V <sub>IH</sub>	HIGH Level Input Voltage	2			V
V <sub>IL</sub>	LOW Level Input Voltage			0.8	V
I <sub>OH</sub>	HIGH Level Output Current			-0.4	mA
I <sub>OL</sub>	LOW Level Output Current			16	mA
T <sub>A</sub>	Free Air Operating Temperature	0		70	°C

**Electrical Characteristics**

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = -12 mA			-1.5	V
V <sub>OH</sub>	HIGH Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max V <sub>IL</sub> = Max	2.4	3.4		V
V <sub>OL</sub>	LOW Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max V <sub>IH</sub> = Min		0.2	0.4	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V			1	mA
I <sub>IH</sub>	HIGH Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.4V			40	μA
I <sub>IL</sub>	LOW Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V			-1.6	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 3)	-18		-55	mA
I <sub>CCH</sub>	Supply Current with Outputs HIGH	V <sub>CC</sub> = Max		8	16	mA
I <sub>CCL</sub>	Supply Current with Outputs Low	V <sub>CC</sub> = Max		14	27	mA

**Note 2:** All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

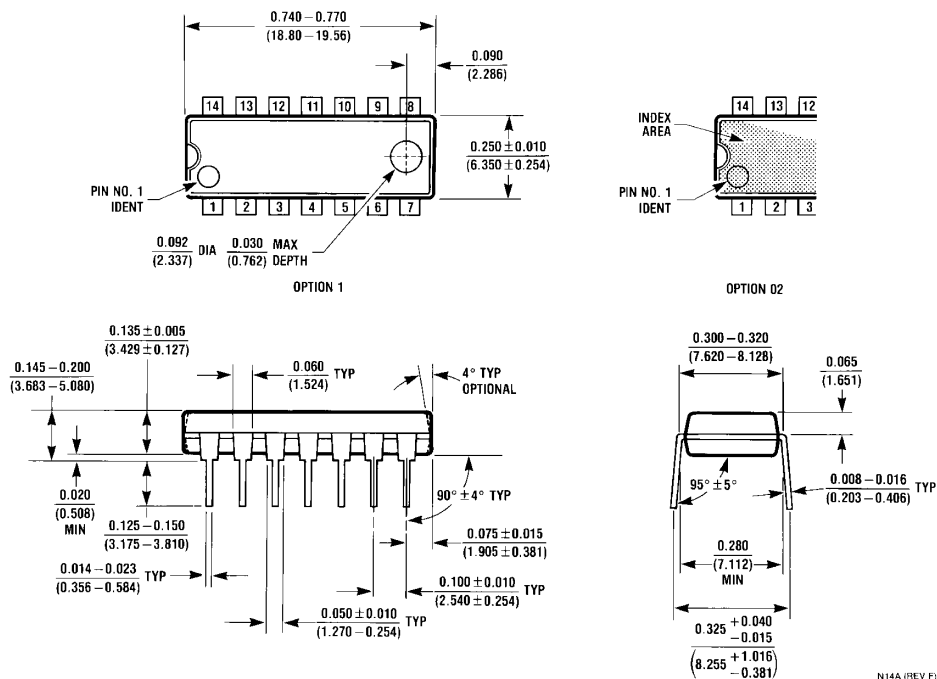
**Note 3:** Not more than one output should be shorted at a time.

**Switching Characteristics**

at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C

Symbol	Parameter	Conditions	Min	Max	Units
t <sub>PLH</sub>	Propagation Delay Time LOW-to-HIGH Level Output	C <sub>L</sub> = 15 pF R <sub>L</sub> = 400Ω		22	ns
t <sub>PHL</sub>	Propagation Delay Time HIGH-to-LOW Level Output			15	ns

# Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide  
Package Number N14A

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## DM7476

# Dual Master-Slave J-K Flip-Flops with Clear, Preset, and Complementary Outputs

### General Description

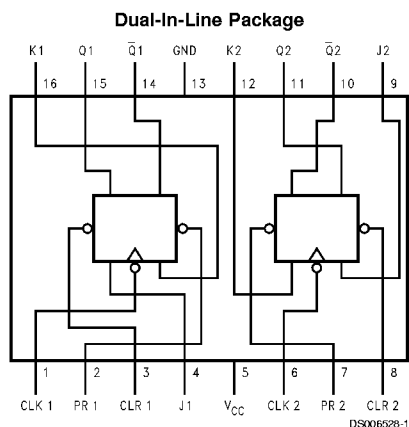
This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flop after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high the J and K inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic state of J and K inputs must not be al-

lowed to change while the clock is high. The data is transferred to the outputs on the falling edge of the clock pulse. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

### Features

- Alternate Military/Aerospace device (5476) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

### Connection Diagram



Order Number 5476DMQB, 5476FMQB,  
DM5476J, DM5476W or DM7476N  
See Package Number J16A, N16E or W16A

### Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	$\neg$	L	L	$Q_0$	$\bar{Q}_0$
H	H	$\neg$	H	L	H	L
H	H	$\neg$	L	H	L	H
H	H	$\neg$	H	H	Toggle	

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

$\neg$  = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.

$Q_0$  = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each complete active high level clock pulse.

**Note 1:** This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.

**Absolute Maximum Ratings** (Note 2)

Supply Voltage

7V

Input Voltage

5.5V

Operating Free Air Temperature Range

DM54 and 54

DM74

Storage Temperature Range

–55°C to +125°C

0°C to +70°C

–65°C to +150°C

**Recommended Operating Conditions**

Symbol	Parameter		DM5476			DM7476			Units
			Min	Nom	Max	Min	Nom	Max	
$V_{CC}$	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High Level Input Voltage		2			2			V
$V_{IL}$	Low Level Input Voltage				0.8			0.8	V
$I_{OH}$	High Level Output Current				–0.4			–0.4	mA
$I_{OL}$	Low Level Output Current				16			16	mA
$f_{CLK}$	Clock Frequency (Note 8)		0		15	0		15	MHz
$t_w$	Pulse Width (Note 8)	Clock High	20			20			ns
		Clock Low	47			47			
		Preset Low	25			25			
		Clear Low	25			25			
$t_{SU}$	Input Setup Time (Notes 3, 8)		0↑			0↑			ns
$t_H$	Input Hold Time (Notes 3, 8)		0↓			0↓			ns
$T_A$	Free Air Operating Temperature		–55		125	0		70	°C

**Note 2:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Electrical Characteristics**

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
$V_I$	Input Clamp Voltage	$V_{CC} = \text{Min}$ , $I_I = -12 \text{ mA}$			–1.5	V
$V_{OH}$	High Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OH} = \text{Max}$ $V_{IL} = \text{Max}$ , $V_{IH} = \text{Min}$	2.4	3.4		V
$V_{OL}$	Low Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OL} = \text{Max}$ $V_{IH} = \text{Min}$ , $V_{IL} = \text{Max}$		0.2	0.4	V
$I_I$	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$ , $V_I = 5.5 \text{ V}$			1	mA
$I_{IH}$	High Level Input Current	$V_{CC} = \text{Max}$ $V_I = 2.4 \text{ V}$	J, K		40	$\mu\text{A}$
			Clock		80	
			Clear		80	
			Preset		80	
$I_{IL}$	Low Level Input Current	$V_{CC} = \text{Max}$ $V_I = 0.4 \text{ V}$ (Note 7)	J, K		–1.6	mA
			Clock		–3.2	
			Clear		–3.2	
			Preset		–3.2	
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 5)	DM54	–20	–55	mA
			DM74	–18	–55	
$I_{CC}$	Supply Current	$V_{CC} = \text{Max}$ (Note 6)		18	34	mA

**Note 3:** The symbol (↑, ↓) indicates the edge of the clock pulse is used for reference (↑) for rising edge, (↓) for falling edge.

**Note 4:** All typicals are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

**Note 5:** Not more than one output should be shorted at a time.

**Note 6:** With all outputs open,  $I_{CC}$  is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement the clock input is grounded.

**Note 7:** Clear is measured with preset high and preset is measured with clear high.

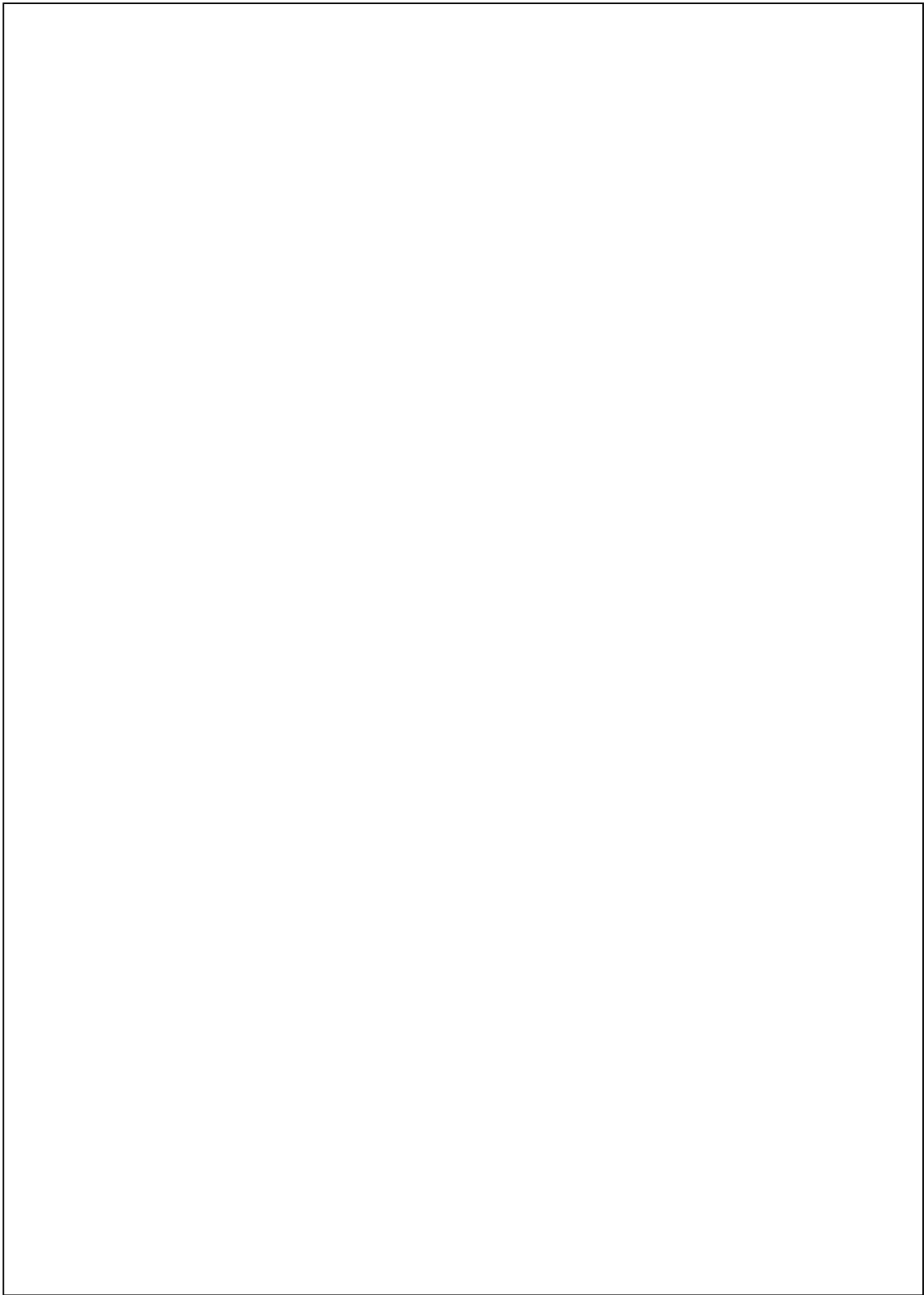
## Electrical Characteristics (Continued)

**Note 8:**  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .

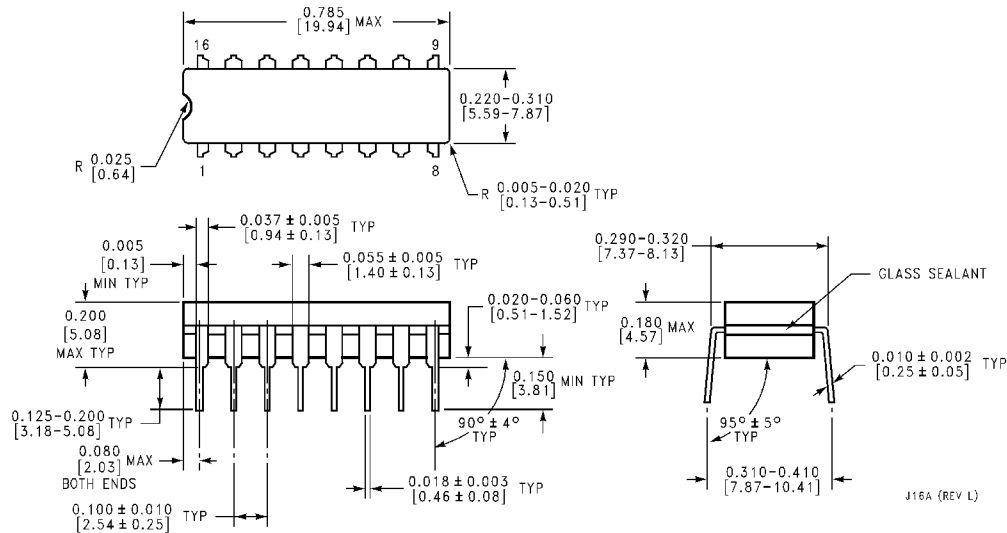
## Switching Characteristics

at  $V_{CC} = 5\text{V}$  and  $T_A = 25^\circ\text{C}$

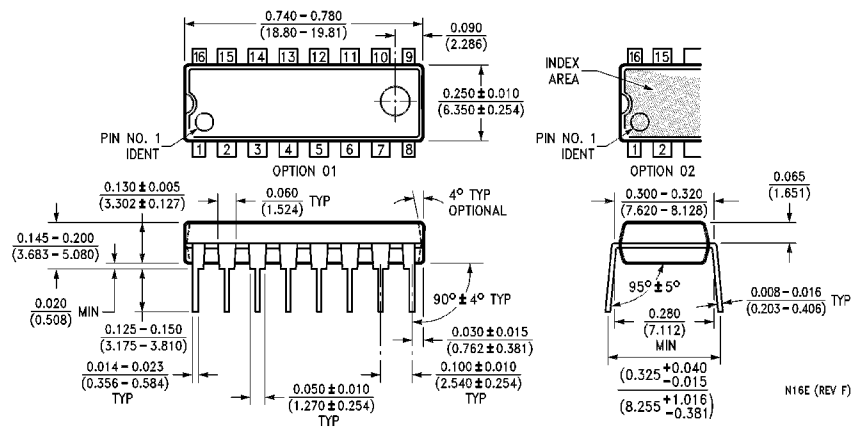
Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$ $C_L = 15\text{ pF}$		Units
			Min	Max	
$f_{MAX}$	Maximum Clock Frequency		15		MHz
$t_{PHL}$	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		40	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	Preset to Q		25	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	Clear to Q		40	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		40	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		25	ns



## Physical Dimensions inches (millimeters) unless otherwise noted

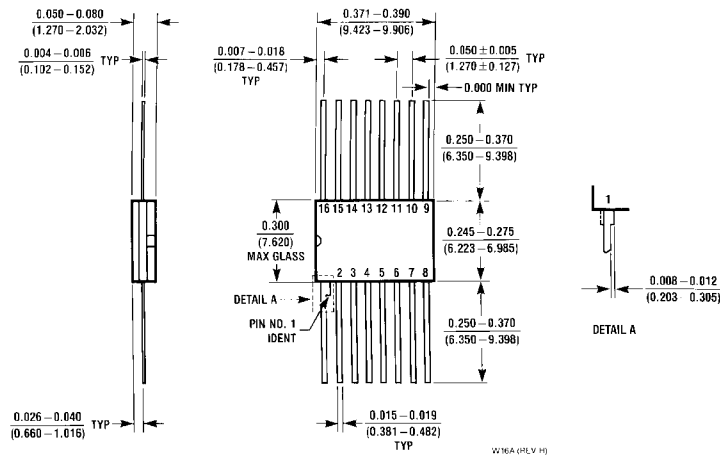


**16-Lead Ceramic Dual-In-Line Package (J)**  
**Order Number 5476DMQB or DM5476J**  
**Package Number J16A**



**16-Lead Molded Dual-In-Line Package (N)**  
**Order Number DM7476N**  
**Package Number N16E**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Ceramic Flat Package (W)**  
**Order Number 5476FMBQ or DM7476W**  
**Package Number W16A**

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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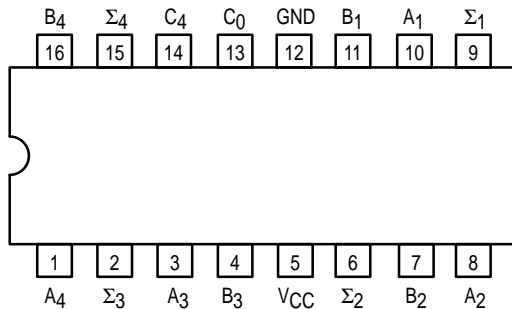
Datasheets for electronic components.



## 4-BIT BINARY FULL ADDER WITH FAST CARRY

The SN54/74LS83A is a high-speed 4-Bit binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words ( $A_1$ – $A_4$ ,  $B_1$ – $B_4$ ) and a Carry Input ( $C_0$ ). It generates the binary Sum outputs  $\Sigma_1$ – $\Sigma_4$  and the Carry Output ( $C_4$ ) from the most significant bit. The LS83A operates with either active HIGH or active LOW operands (positive or negative logic). The SN54/74LS283 is recommended for new designs since it is identical in function with this device and features standard corner power pins.

### CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

$A_1$ – $A_4$  Operand A Inputs  
 $B_1$ – $B_4$  Operand B Inputs  
 $C_0$  Carry Input  
 $\Sigma_1$ – $\Sigma_4$  Sum Outputs (Note b)  
 $C_4$  Carry Output (Note b)

### LOADING (Note a)

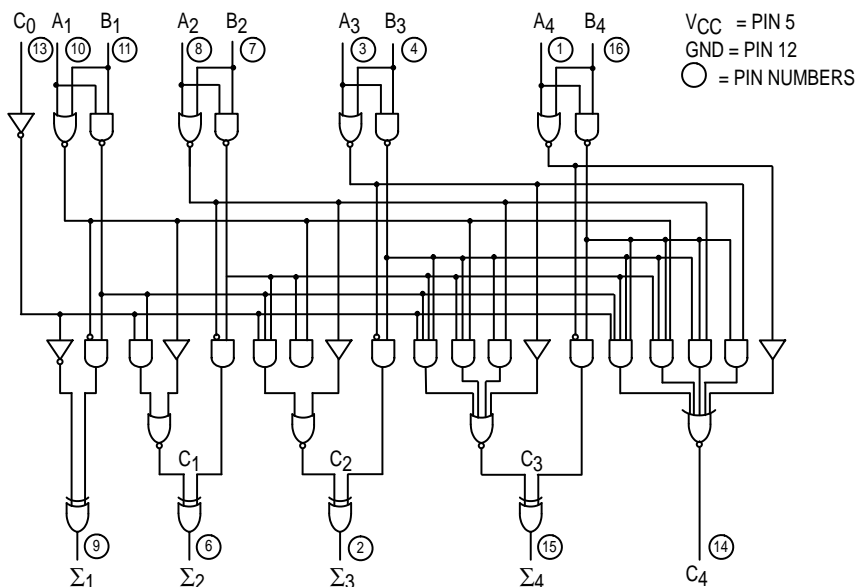
HIGH	LOW
1.0 U.L.	0.5 U.L.
1.0 U.L.	0.5 U.L.
0.5 U.L.	0.25 U.L.
10 U.L.	5 (2.5) U.L.
10 U.L.	5 (2.5) U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

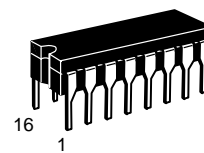
### LOGIC DIAGRAM



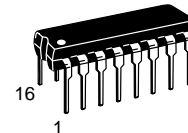
## SN54/74LS83A

### 4-BIT BINARY FULL ADDER WITH FAST CARRY

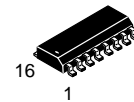
#### LOW POWER SCHOTTKY



**J SUFFIX**  
CERAMIC  
CASE 620-09



**N SUFFIX**  
PLASTIC  
CASE 648-08

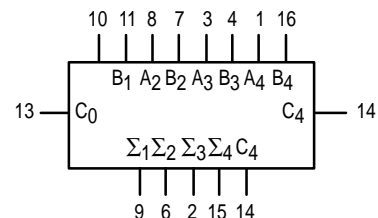


**D SUFFIX**  
SOIC  
CASE 751B-03

### ORDERING INFORMATION

SN54LSXXJ Ceramic  
SN74LSXXN Plastic  
SN74LSXXD SOIC

### LOGIC SYMBOL



# SN54/74LS83A

## FUNCTIONAL DESCRIPTION

The LS83A adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs ( $\Sigma_1 - \Sigma_4$ ) and outgoing carry ( $C_4$ ) outputs.

$$C_0 + (A_1+B_1)+2(A_2+B_2)+4(A_3+B_3)+8(A_4+B_4) = \Sigma_1+2\Sigma_2+4\Sigma_3+8\Sigma_4+16C_4$$

Where: (+) = plus

Due to the symmetry of the binary add function the LS83A can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH Inputs, Carry Input can not be left open, but must be held LOW when no carry in is intended.

Example:

	C <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	A <sub>4</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>	B <sub>4</sub>	Σ <sub>1</sub>	Σ <sub>2</sub>	Σ <sub>3</sub>	Σ <sub>4</sub>	C <sub>4</sub>	
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10+9 = 19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry+5+6 = 12)

Interchanging inputs of equal weight does not affect the operation, thus C<sub>0</sub>, A<sub>1</sub>, B<sub>1</sub>, can be arbitrarily assigned to pins 10, 11, 13, etc.

## FUNCTIONAL TRUTH TABLE

C (n-1)	A <sub>n</sub>	B <sub>n</sub>	Σ <sub>n</sub>	C <sub>n</sub>
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

C<sub>1</sub> — C<sub>3</sub> are generated internally  
C<sub>0</sub> — is an external input  
C<sub>4</sub> — is an output generated internally

## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I <sub>OH</sub>	Output Current — High	54, 74			-0.4	mA
I <sub>OL</sub>	Output Current — Low	54 74			4.0 8.0	mA

# SN54/74LS83A

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
$V_{IK}$	Input Clamp Diode Voltage			-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ per Truth Table
		74	2.7	3.5		V	
$V_{OL}$	Output LOW Voltage	54, 74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$ , $V_{IN} = V_{IL}$ or $V_{IH}$ per Truth Table
		74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
$I_{IH}$	Input HIGH Current $C_0$ A or B				20 40	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
	$C_0$ A or B				0.1 0.2	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current $C_0$ A or B				-0.4 -0.8	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{OS}$	Output Short Circuit Current (Note 1)		-20		-100	mA	$V_{CC} = \text{MAX}$
$I_{CC}$	Power Supply Current All Inputs Grounded All Inputs at 4.5 V, Except B All Inputs at 4.5 V				39 34 34	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay, $C_0$ Input to any $\Sigma$ Output			16 15	24 24	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$ Figures 1 and 2
$t_{PLH}$ $t_{PHL}$	Propagation Delay, Any A or B Input to $\Sigma$ Outputs			15 15	24 24	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay, $C_0$ Input to $C_4$ Output			11 15	17 22	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay, Any A or B Input to $C_4$ Output			11 12	17 17	ns	

## AC WAVEFORMS

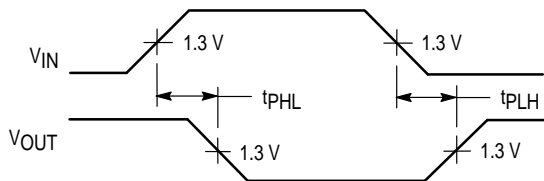


Figure 1

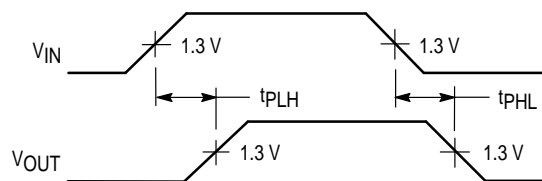


Figure 2

## DM74LS11

### Triple 3-Input AND Gate

#### General Description

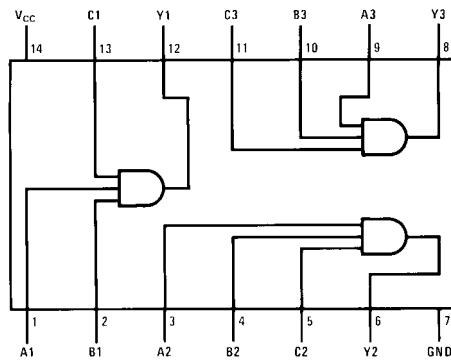
This device contains three independent gates each of which performs the logic AND function.

#### Ordering Code:

Order Number	Package Number	Package Description
DM74LS11M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS11N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Connection Diagram



#### Function Table

$$Y = ABC$$

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = HIGH Logic Level  
L = LOW Logic Level  
X = Either LOW or HIGH Logic Level

**Absolute Maximum Ratings**(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
V <sub>CC</sub>	Supply Voltage	4.75	5	5.25	V
V <sub>IH</sub>	HIGH Level Input Voltage	2			V
V <sub>IL</sub>	LOW Level Input Voltage			0.8	V
I <sub>OH</sub>	HIGH Level Output Current			–0.4	mA
I <sub>OL</sub>	LOW Level Output Current			8	mA
T <sub>A</sub>	Free Air Operating Temperature	0		70	°C

**Electrical Characteristics**

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = –18 mA			–1.5	V
V <sub>OH</sub>	HIGH Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max V <sub>IH</sub> = Min	2.7	3.4		V
V <sub>OL</sub>	LOW Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max V <sub>IL</sub> = Max I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min		0.35 0.25	0.5 0.4	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 7V			0.1	mA
I <sub>IH</sub>	HIGH Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V			20	μA
I <sub>IL</sub>	LOW Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V			–0.36	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 3)	–20		–100	mA
I <sub>CCH</sub>	Supply Current with Outputs HIGH	V <sub>CC</sub> = Max		1.8	3.6	mA
I <sub>CCL</sub>	Supply Current with Outputs LOW	V <sub>CC</sub> = Max		3.3	6.6	mA

**Note 2:** All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

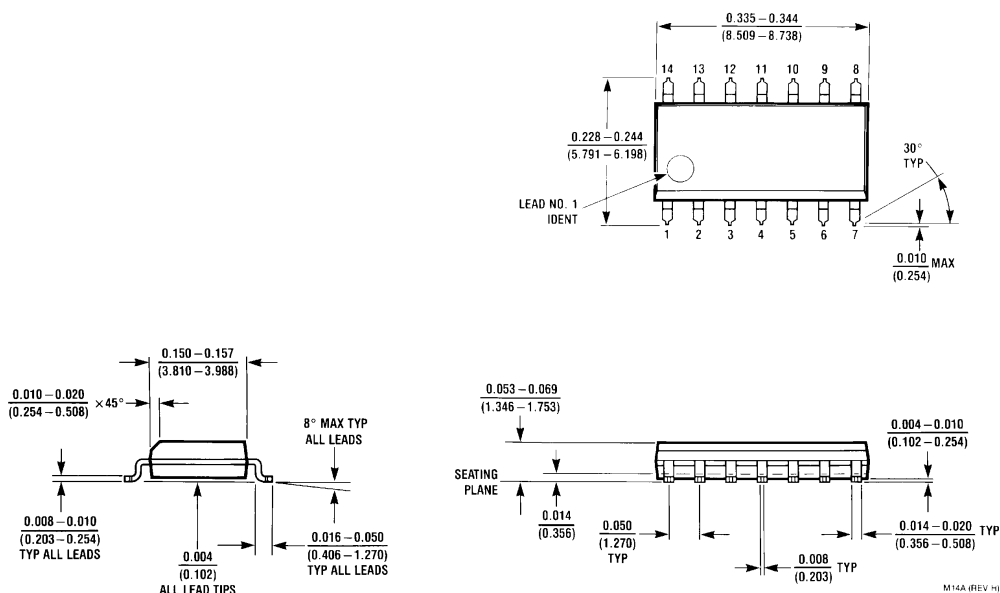
**Note 3:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

**Switching Characteristics**

at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C

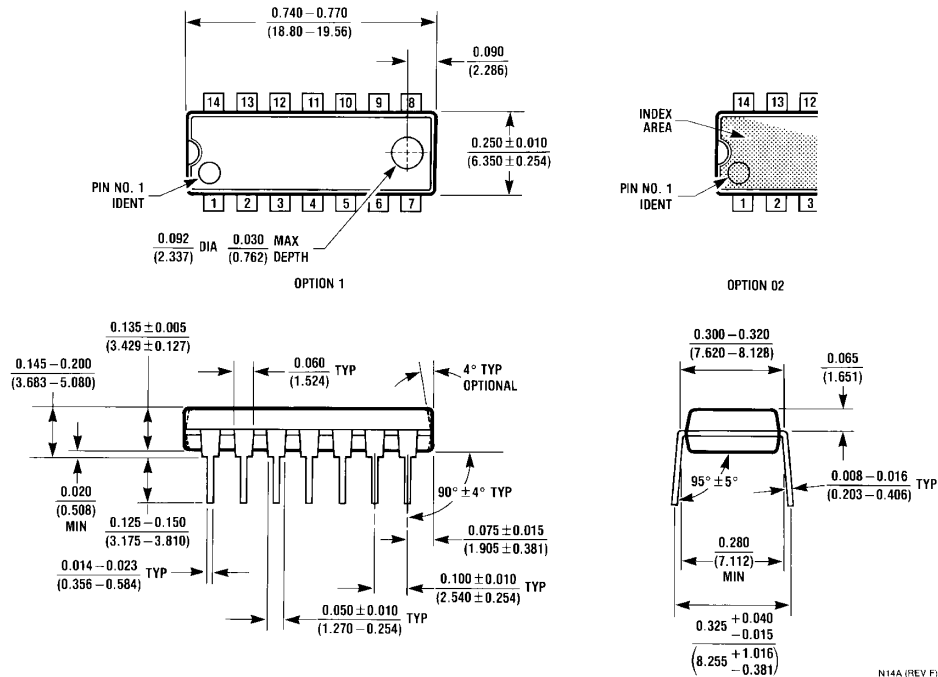
Symbol	Parameter	R <sub>L</sub> = 2 kΩ				Units
		C <sub>L</sub> = 15 pF		C <sub>L</sub> = 50 pF		
		Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay Time LOW-to-HIGH Level Output	4	13	6	18	ns
t <sub>PHL</sub>	Propagation Delay Time HIGH-to-LOW Level Output	3	11	5	18	ns

**Physical Dimensions** inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow Package Number M14A**

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide  
Package Number N14A

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## 54LS85/DM54LS85/DM74LS85 4-Bit Magnitude Comparators

### General Description

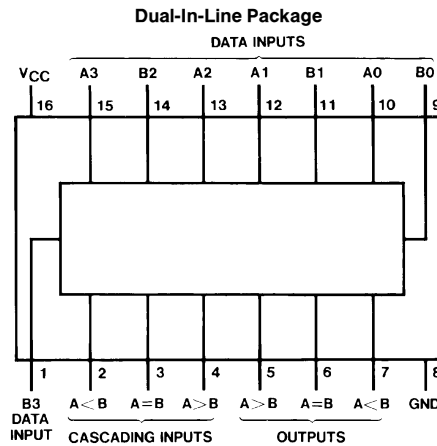
These 4-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two, 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The  $A > B$ ,  $A < B$ , and  $A = B$  outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must

have a high-level voltage applied to the  $A = B$  input. The cascading path is implemented with only a two-gate-level delay to reduce overall comparison times for long words.

### Features

- Typical power dissipation 52 mW
- Typical delay (4-bit words) 24 ns
- Alternate Military/Aerospace device (54LS85) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

### Connection Diagram



TL/F/6379-1

### Function Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

H = High Level, L = Low Level, X = Don't Care

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameter	DM54LS85			DM74LS85			Units
		Min	Nom	Max	Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2			2			V
V <sub>IL</sub>	Low Level Input Voltage			0.7			0.8	V
I <sub>OH</sub>	High Level Output Current			−0.4			−0.4	mA
I <sub>OL</sub>	Low Level Output Current			4			8	mA
T <sub>A</sub>	Free Air Operating Temperature	−55		125	0		70	°C

## Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = −18 mA			−1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	DM54 2.5 DM74 2.7	3.4		V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	DM54 DM74	0.25 0.35	0.4 0.5	V
		I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min	DM74	0.25	0.4	
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max V <sub>I</sub> = 7V	A < B A > B Others		0.1 0.1 0.3	mA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max V <sub>I</sub> = 2.7V	A < B A > B Others		20 20 60	μA
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max V <sub>I</sub> = 0.4V	A < B A > B Others		−0.4 −0.4 −1.2	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 2)	DM54 DM74	−20 −20	−100 −100	mA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max (Note 3)		10	20	mA

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

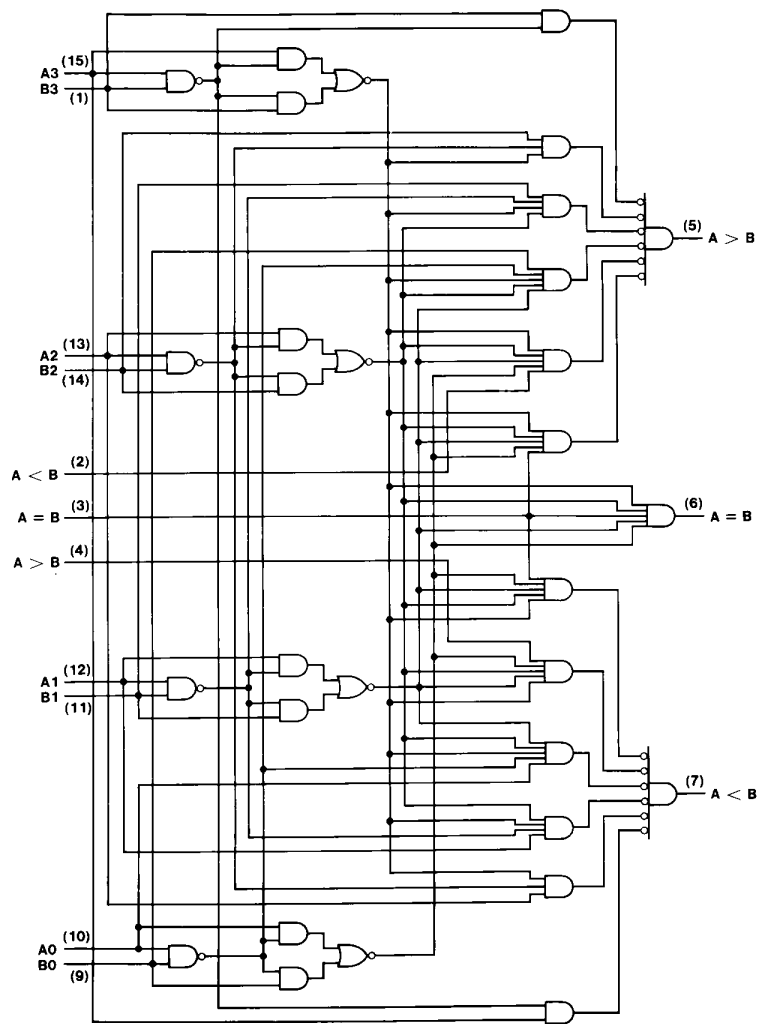
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I<sub>CC</sub> is measured with all outputs open, A = B grounded and all other inputs at 4.5V.

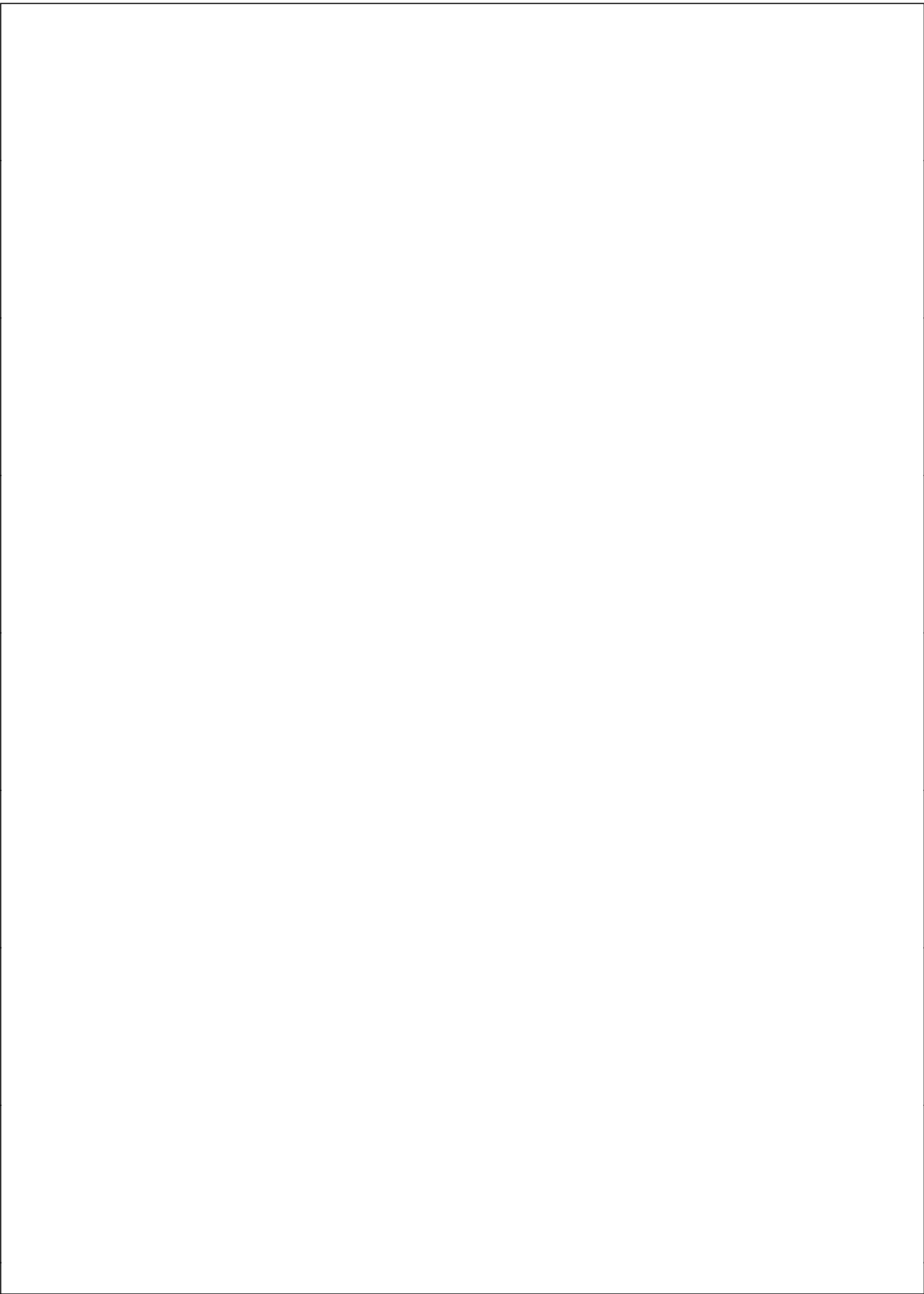
**Switching Characteristics** at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$  (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From Input	To Output	Number of Gate Levels	R <sub>L</sub> = 2 kΩ				Units
					C <sub>L</sub> = 15 pF		C <sub>L</sub> = 50 pF		
					Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay Time Low-to-High Level Output	Any A or B Data Input	A < B, A > B	3		36		42	ns
			A = B	4		40		40	
t <sub>PHL</sub>	Propagation Delay Time High-to-Low Level Output	Any A or B Data Input	A < B, A > B	3		30		40	ns
			A = B	4		30		40	
t <sub>PLH</sub>	Propagation Delay Time Low-to-High Level Output	A < B or A = B	A > B	1		22		26	ns
t <sub>PHL</sub>	Propagation Delay Time High-to-Low Level Output	A < B or A = B	A > B	1		17		26	ns
t <sub>PLH</sub>	Propagation Delay Time Low-to-High Level Output	A = B	A = B	2		20		25	ns
t <sub>PHL</sub>	Propagation Delay Time High-to-Low Level Output	A = B	A = B	2		17		26	ns
t <sub>PLH</sub>	Propagation Delay Time Low-to-High Level Output	A > B or A = B	A < B	1		22		26	ns
t <sub>PHL</sub>	Propagation Delay Time High-to-Low Level Output	A > B or A = B	A < B	1		17		26	ns

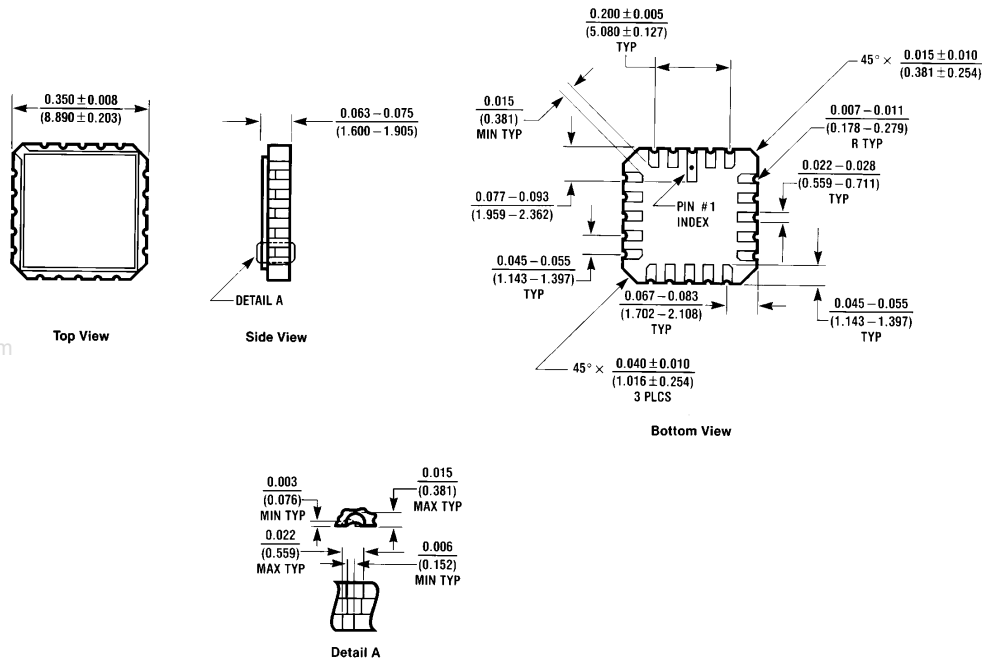
# Logic Diagram



TL/F/6379-2

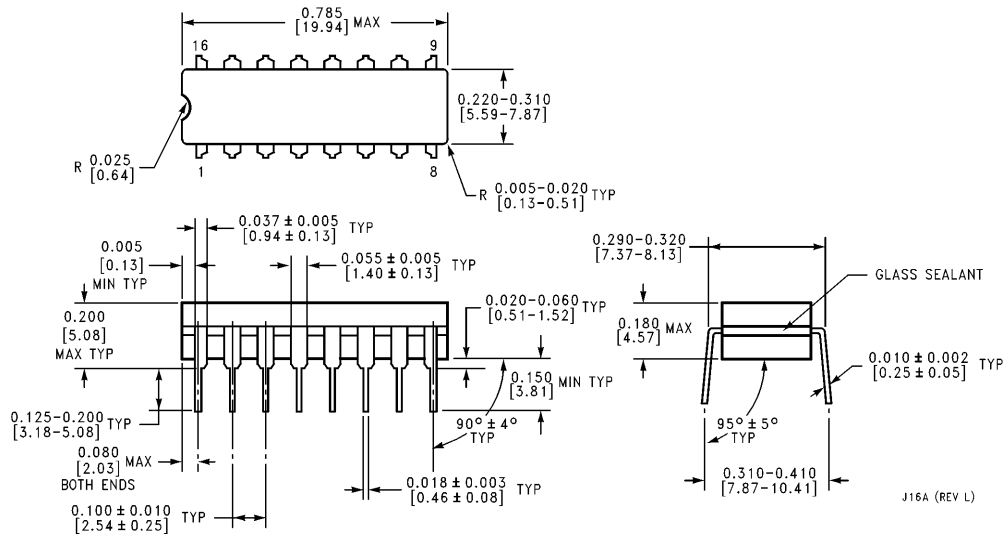


## Physical Dimensions inches (millimeters)



**Chip Carrier Package (E)**  
**Order Number 54LS85LMQB**  
**NS Package Number E20A**

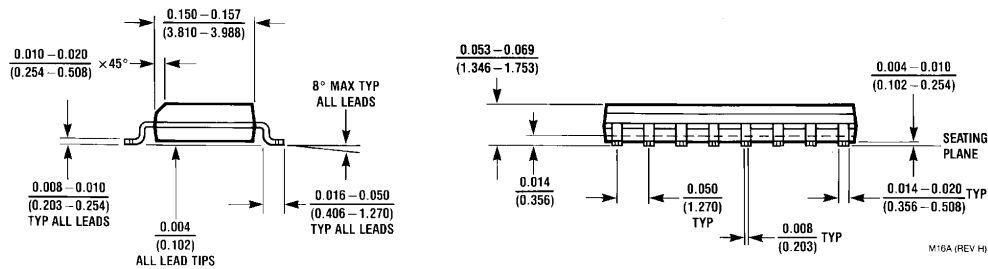
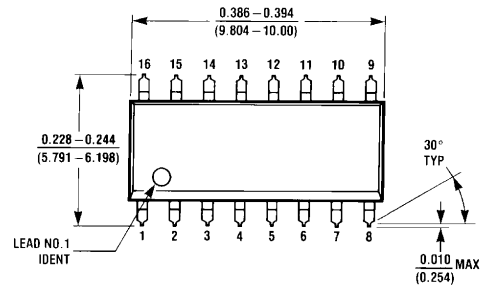
E20A (REV D)



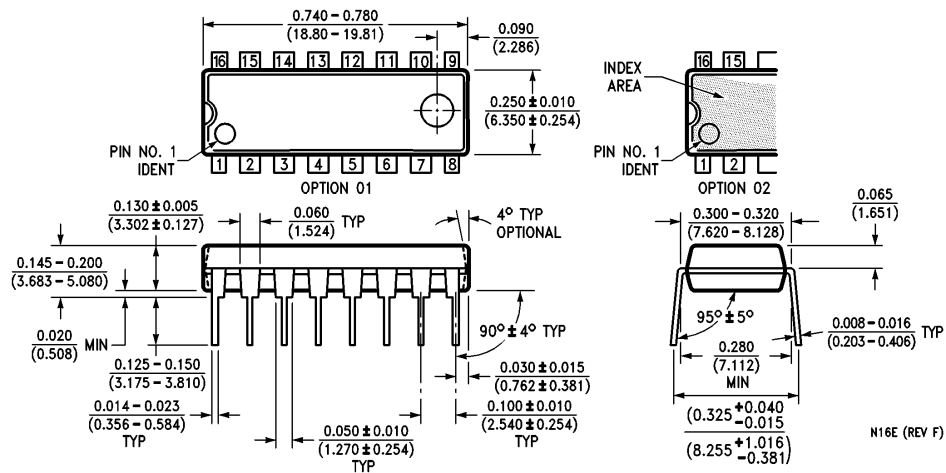
**16-Lead Ceramic Dual-In-Line Package (J)**  
**Order Number 54LS85DMQB or DM54LS85J**  
**NS Package Number J16A**

J16A (REV L)

# Physical Dimensions inches (millimeters) (Continued)

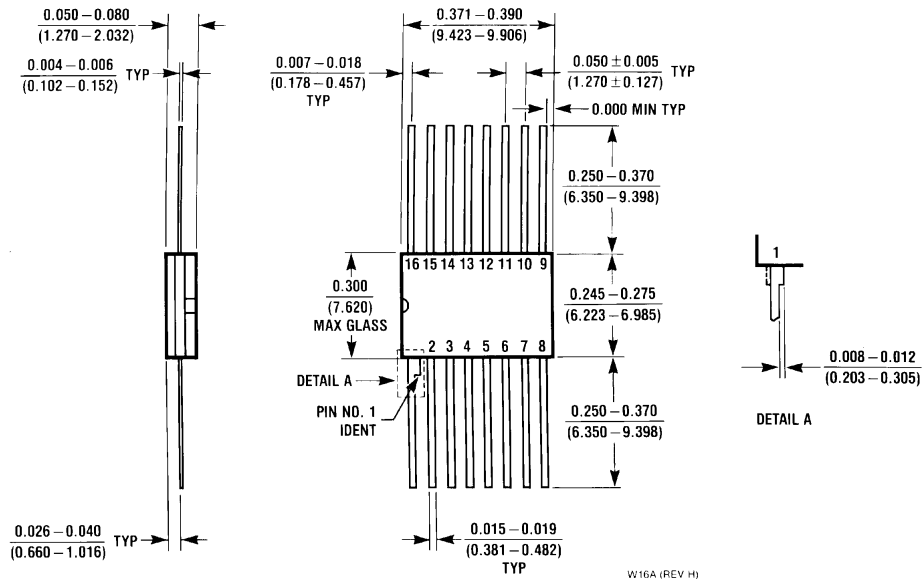


**16-Lead Small Outline Molded Package (M)**  
**Order Number DM74LS85M**  
**NS Package Number M16A**



**16-Lead Molded Dual-In-Line Package (N)**  
**Order Number DM74LS85N**  
**NS Package Number N16E**



**Physical Dimensions** inches (millimeters) (Continued)

**16-Lead Ceramic Flat Package (W)**  
**Order Number 54LS85FMQB or DM54LS85W**  
**NS Package Number W16A**

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## DM7486

### Quad 2-Input Exclusive-OR Gate

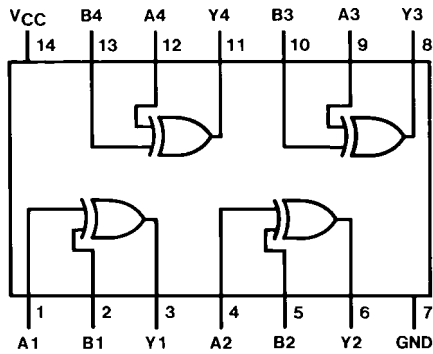
#### General Description

This device contains four independent gates each of which performs the logic exclusive-OR function.

#### Ordering Code:

Order Number	Package Number	Package Description
DM7486N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

#### Connection Diagram



#### Function Table

$$Y = A \oplus B$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level  
L = LOW Logic Level

**Absolute Maximum Ratings**(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
$V_{CC}$	Supply Voltage	4.75	5	5.25	V
$V_{IH}$	HIGH Level Input Voltage	2			V
$V_{IL}$	LOW Level Input Voltage			0.8	V
$I_{OH}$	HIGH Level Output Current			–0.8	mA
$I_{OL}$	LOW Level Output Current			16	mA
$T_A$	Free Air Operating Temperature	0		70	°C

**Electrical Characteristics**

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
$V_I$	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -12 \text{ mA}$			–1.5	V
$V_{OH}$	HIGH Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$	2.4	3.4		V
$V_{OL}$	LOW Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IH} = \text{Min}, V_{IL} = \text{Max}$		0.2	0.4	V
$I_I$	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 5.5 \text{ V}$			1	mA
$I_{IH}$	HIGH Level Input Current	$V_{CC} = \text{Max}, V_I = 2.4 \text{ V}$			40	μA
$I_{IL}$	LOW Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4 \text{ V}$			–1.6	mA
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 3)	–18		–55	mA
$I_{CCH}$	Supply Current with Outputs HIGH	$V_{CC} = \text{Max}$ (Note 4)		30	50	mA
$I_{CCL}$	Supply Current with Outputs LOW	$V_{CC} = \text{Max}$ (Note 3)(Note 5)		36	57	mA

**Note 2:** All typicals are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

**Note 3:** Not more than one output should be shorted at a time.

**Note 4:**  $I_{CCH}$  is measured with all outputs open, one input of each gate at 4.5V, and the other inputs grounded.

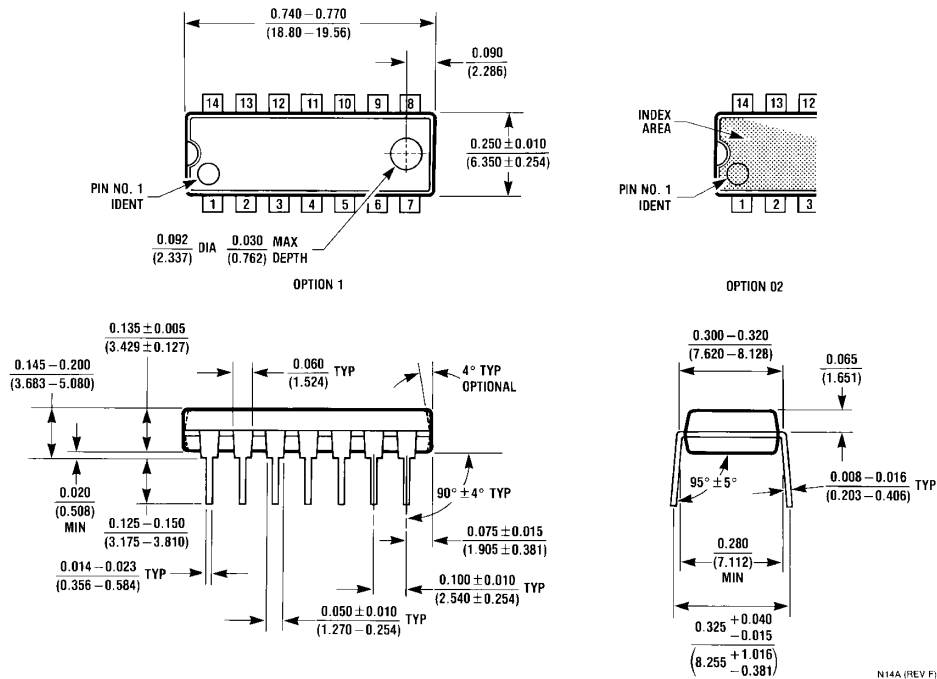
**Note 5:**  $I_{CCL}$  is measured with all outputs open, and all inputs at ground.

**Switching Characteristics**

at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$

Symbol	Parameter	Conditions	$C_L = 15 \text{ pF}, R_L = 400\Omega$		Units
			Min	Max	
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Other Input LOW		23	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output			17	ns
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Other Input HIGH		30	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output			22	ns

# Physical Dimensions inches (millimeters) unless otherwise noted



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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Datasheets for electronics components.

## 74LS194

### 4-Bit Bidirectional Universal Shift Register

#### General Description

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register; they feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

- Parallel (broadside) load
- Shift right (in the direction  $Q_A$  toward  $Q_D$ )
- Shift left (in the direction  $Q_D$  toward  $Q_A$ )
- Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs,  $S_0$  and  $S_1$ , HIGH. The data is loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when  $S_0$  is HIGH and  $S_1$  is LOW. Serial data for this mode is entered at the shift-right data input. When  $S_0$  is LOW and  $S_1$  is HIGH, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are LOW.

#### Features

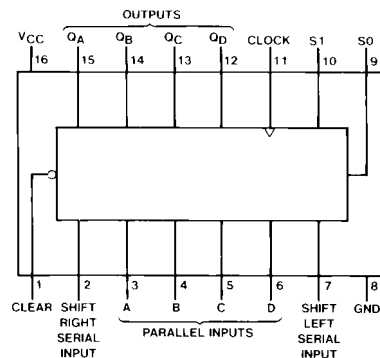
- Parallel inputs and outputs
- Four operating modes:
  - Synchronous parallel load
  - Right shift
  - Left shift
  - Do nothing
- Positive edge-triggered clocking
- Direct overriding clear

#### Ordering Code:

Order Number	Package Number	Package Description
DM74LS194AM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS194AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Connection Diagram



DM74LS194A

## Function Table

Inputs									Outputs				
Clear	Mode		Clock	Serial		Parallel				Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>
	S1	S0		Left	Right	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>
H	L	H	↑	X	L	X	X	X	X	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>
H	H	L	↑	H	X	X	X	X	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	H
H	H	L	↑	L	X	X	X	X	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	L
H	L	L	X	X	X	X	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>

H = HIGH Level (steady state)

L = LOW Level (steady state)

X = Don't Care (any input, including transitions)

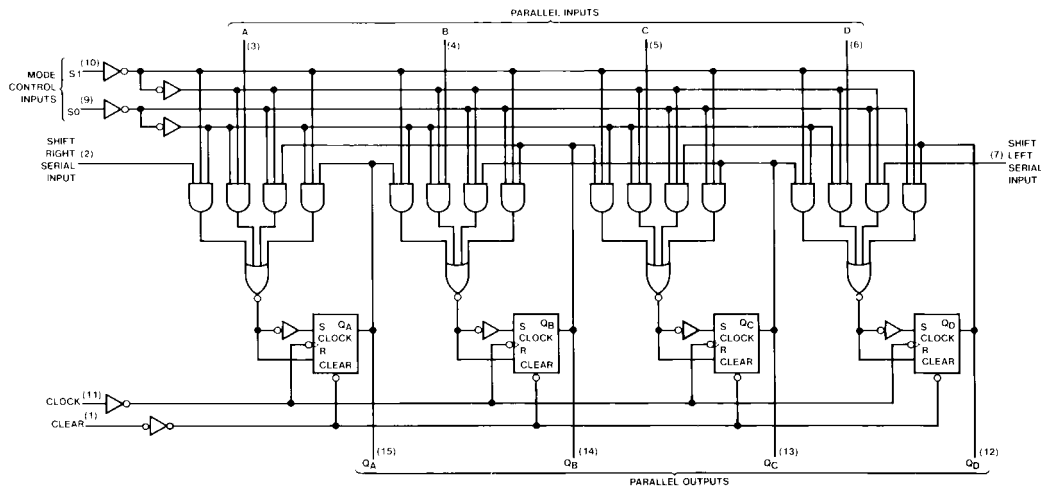
↑ = Transition from LOW-to-HIGH level

a, b, c, d = The level of steady state input at inputs A, B, C or D, respectively.

Q<sub>A0</sub>, Q<sub>B0</sub>, Q<sub>C0</sub>, Q<sub>D0</sub> = The level of Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, or Q<sub>D</sub>, respectively, before the indicated steady state input conditions were established.

Q<sub>An</sub>, Q<sub>Bn</sub>, Q<sub>Cn</sub>, Q<sub>Dn</sub> = The level of Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>C</sub>, respectively, before the most-recent ↑ transition of the clock.

## Logic Diagram



## Absolute Maximum Ratings<sup>(Note 1)</sup>

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V <sub>CC</sub>	Supply Voltage	4.75	5	5.25	V
V <sub>IH</sub>	HIGH Level Input Voltage	2			V
V <sub>IL</sub>	LOW Level Input Voltage			0.8	V
I <sub>OH</sub>	HIGH Level Output Current			−0.4	mA
I <sub>OL</sub>	LOW Level Output Current			8	mA
f <sub>CLK</sub>	Clock Frequency (Note 2)	0		25	MHz
	Clock Frequency (Note 3)	0		20	
t <sub>W</sub>	Pulse Width (Note 4)	Clock	20		ns
		Clear	20		
t <sub>SU</sub>	Setup Time (Note 4)	Mode	30		ns
		Data	20		
t <sub>H</sub>	Hold Time (Note 4)	0			ns
t <sub>REL</sub>	Clear Release Time (Note 4)	25			ns
T <sub>A</sub>	Free Air Operating Temperature	0		70	°C

**Note 2:** C<sub>L</sub> = 15 pF, T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

**Note 3:** C<sub>L</sub> = 50 pF, R<sub>L</sub> = 2 kΩ, T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

**Note 4:** T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

## Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = −18 mA			−1.5	V
V <sub>OH</sub>	HIGH Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	2.7	3.4		V
V <sub>OL</sub>	LOW Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max V <sub>IL</sub> = Max, V <sub>IH</sub> = Min		0.35	0.5	V
		I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min			0.4	
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 7V			0.1	mA
I <sub>IH</sub>	HIGH Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V			20	μA
I <sub>IL</sub>	LOW Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V			−0.4	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 6)	−20		−100	mA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max (Note 7)		15	23	mA

**Note 5:** All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

**Note 6:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

**Note 7:** With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the serial inputs, I<sub>CC</sub> is tested with momentary ground, then 4.5V applied to CLOCK.



## Switching Characteristics

at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$

Symbol	Parameter	From (Input) To (Output)	$C_L = 50 \text{ pF}, R_L = 2 \text{ k}\Omega$		Units
			Min	Max	
$f_{MAX}$	Maximum Clock Frequency		20		MHz
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Any Q		26	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Any Q		35	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Output	Clear to Any Q		38	ns

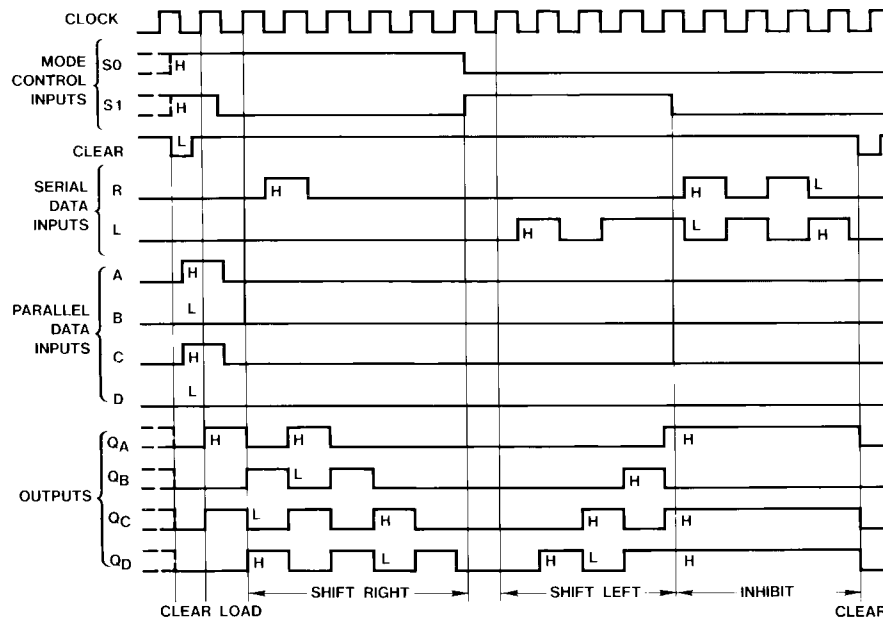
**Note 8:** All typicals are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .

**Note 9:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

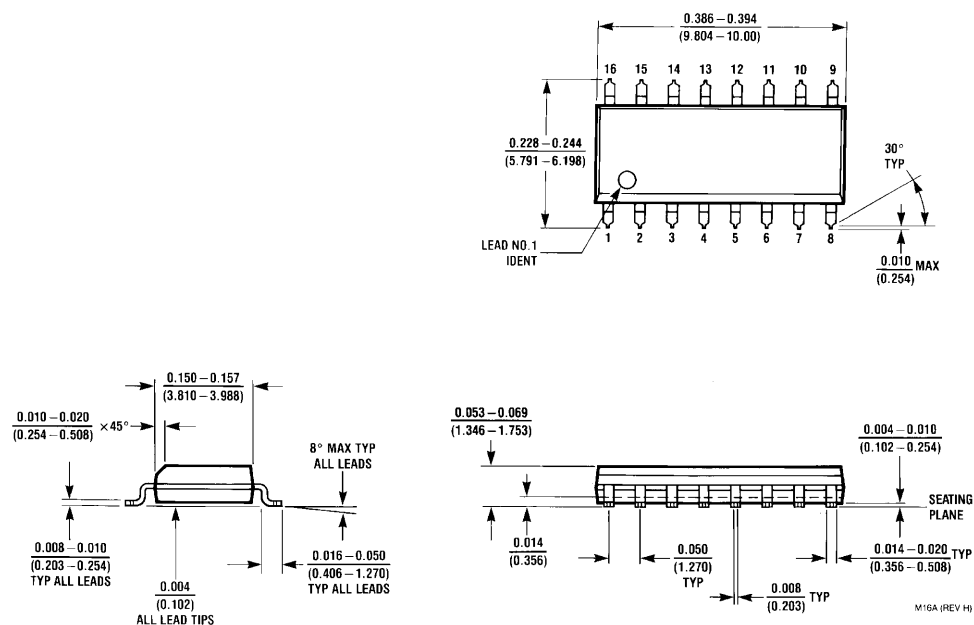
**Note 10:** With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the serial inputs,  $I_{CC}$  is tested with momentary ground, then 4.5V applied to CLOCK.

## Timing Diagram

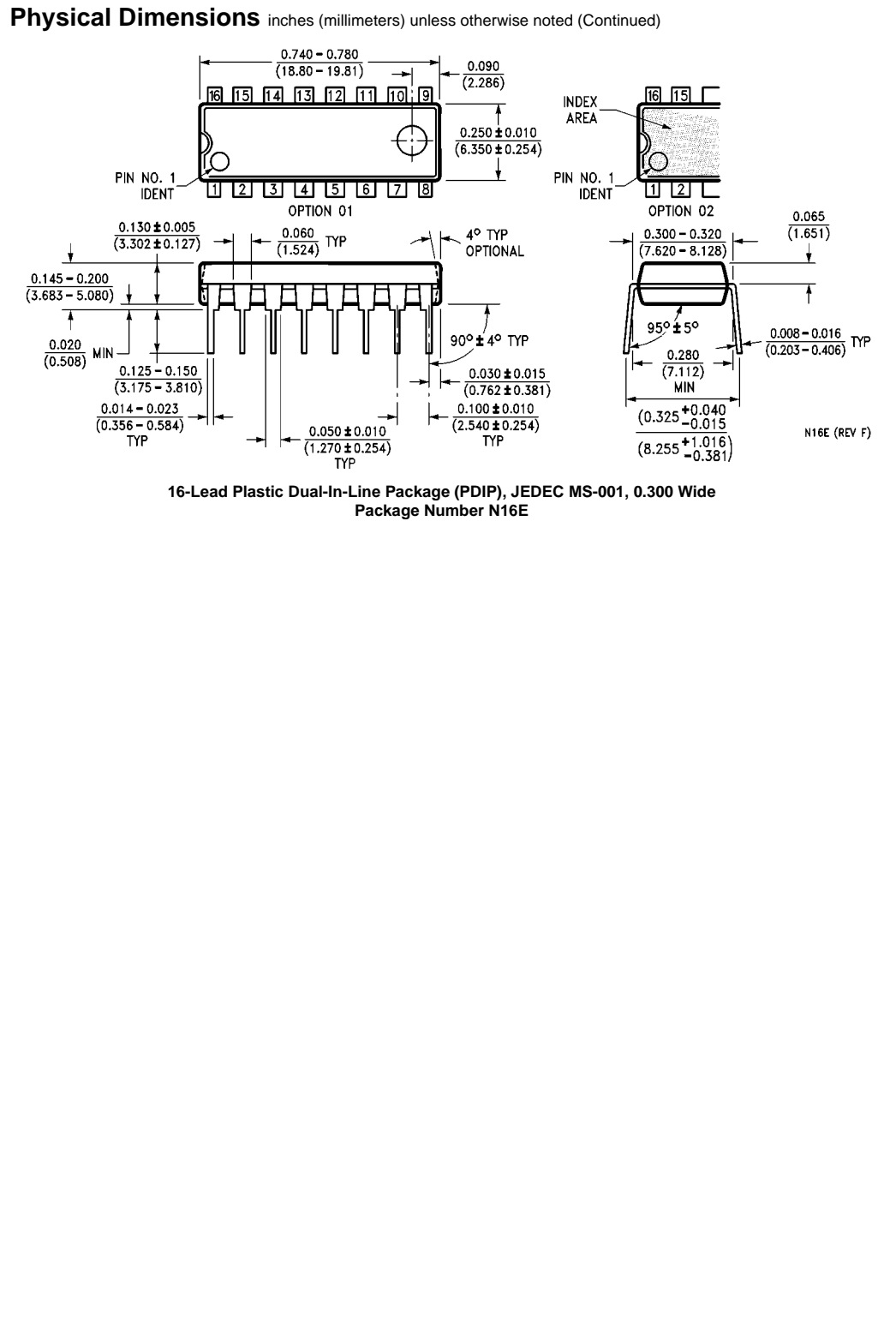
Typical Clear, Load, Right-Shift, Left-Shift, Inhibit, and Clear Sequences



**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A**



## DM74LS266

### Quad 2-Input Exclusive-NOR Gate with Open-Collector Outputs

#### General Description

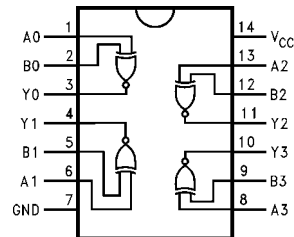
This device contains four independent gates each of which performs the logic exclusive-NOR function. Outputs are open collector.

#### Ordering Code:

Order Number	Package Number	Package Description
DM74LS266M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS266N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Connection Diagram



#### Truth Table

Inputs		Outputs
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

H = HIGH Voltage Level  
L = LOW Voltage Level

DM74LS266 Quad 2-Input Exclusive-NOR Gate

**Absolute Maximum Ratings**(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
$V_{CC}$	Supply Voltage	4.75	5	5.25	V
$V_{IH}$	HIGH Level Input Voltage	2			V
$V_{IL}$	LOW Level Input Voltage			0.8	V
$V_{OH}$	HIGH Level Output Voltage			5.5	V
$I_{OL}$	LOW Level Output Current			8	mA
$T_A$	Free Air Operating Temperature	0		70	°C

**Electrical Characteristics**

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
$V_I$	Input Clamp Voltage	$V_{CC} = \text{Min}$ , $I_I = -18 \text{ mA}$			–1.5	V
$I_{CEX}$	HIGH Level Output Current	$V_{CC} = \text{Min}$ , $V_O = 5.5 \text{ V}$ , $V_{IL} = \text{Max}$			100	μA
$V_{OL}$	LOW Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OL} = \text{Max}$ , $V_{IH} = \text{Min}$			0.5	V
		$I_{OL} = 4 \text{ mA}$ , $V_{CC} = \text{Min}$			0.4	
$I_I$	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$ , $V_I = 7 \text{ V}$			0.2	mA
$I_{IH}$	HIGH Level Input Current	$V_{CC} = \text{Max}$ , $V_I = 2.7 \text{ V}$			40	μA
$I_{IL}$	LOW Level Input Current	$V_{CC} = \text{Max}$ , $V_I = 0.4 \text{ V}$			–0.8	mA
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 3)	–20		–100	mA
$I_{CC}$	Supply Current	$V_{CC} = \text{Max}$			13	mA

**Note 2:** All typicals are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

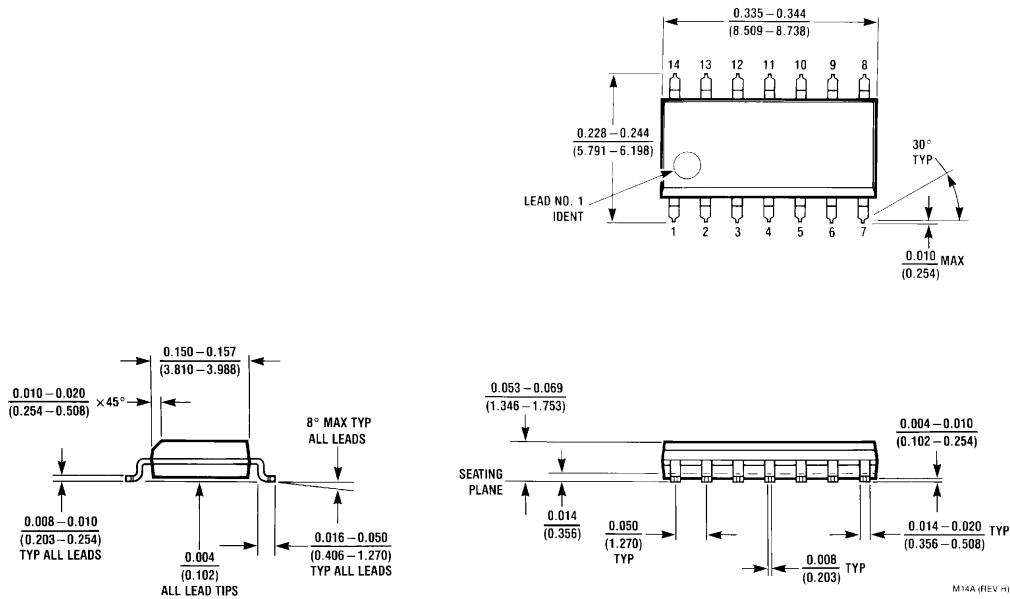
**Note 3:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

**Switching Characteristics**

$V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

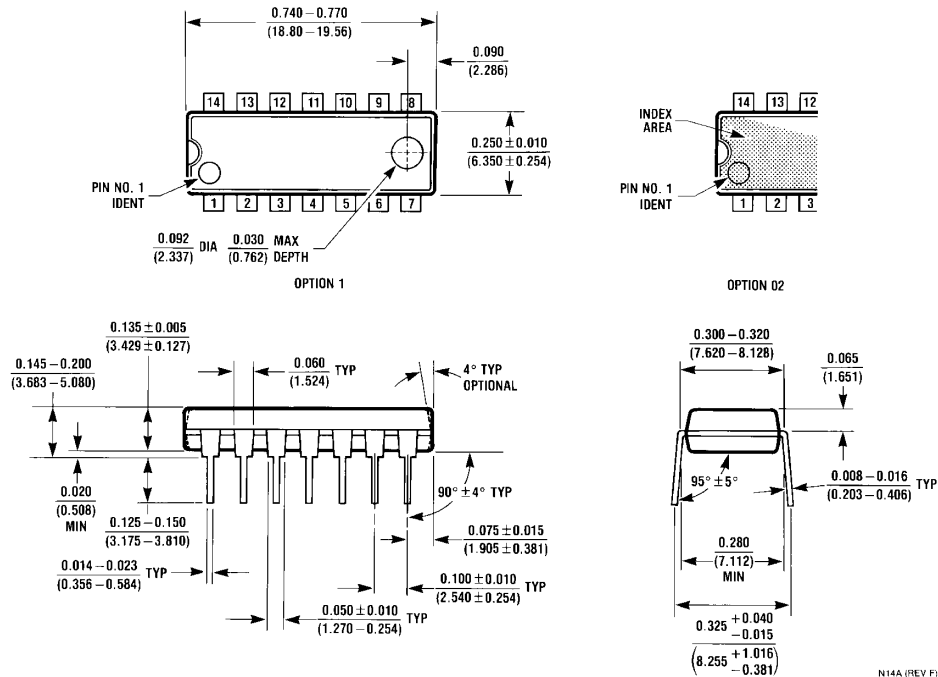
Symbol	Parameter	$R_L = 2 \text{ k}\Omega$ $C_L = 15 \text{ pF}$		Units
		Min	Max	
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output		23	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output		23	ns

**Physical Dimensions** inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow  
Package Number M14A**

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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# SN54147, SN54148, SN54LS147, SN54LS148, SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148 10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS

SDLS053 OCTOBER 1978 - REVISED MARCH 1988

## '147, 'LS147

- Encodes 10-Line Decimal to 4-Line BCD

- Applications Include:

Keyboard Encoding

Range Selection: '148, 'LS148

- Encodes 8 Data Lines to 3-Line Binary (Octal)

- Applications Include:

N-Bit Encoding

Code Converters and Generators

TYPE	TYPICAL DATA DELAY	TYPICAL POWER DISSIPATION
'147	10 ns	225 mW
'148	10 ns	190 mW
'LS147	15 ns	60 mW
'LS148	15 ns	60 mW

## description

These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The '147 and 'LS147 encode nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. The '148 and 'LS148 encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level. All inputs are buffered to represent one normalized Series 54/74 or 54LS/74LS load, respectively.

## '147, 'LS147

FUNCTION TABLE

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	L	H	H	H	H	H	L	L	H
X	X	X	L	H	H	H	H	H	H	L	H	L
X	X	L	H	H	H	H	H	H	H	L	H	H
X	L	H	H	H	H	H	H	H	H	H	L	L
L	H	H	H	H	H	H	H	H	H	H	H	L

H = high logic level, L = low logic level, X = irrelevant

## SN54147, SN54LS147,

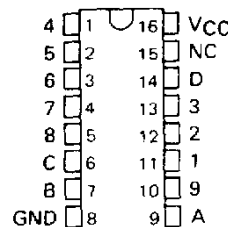
SN54148, SN54LS148 . . . J OR W PACKAGE

SN74147, SN74148 . . . N PACKAGE

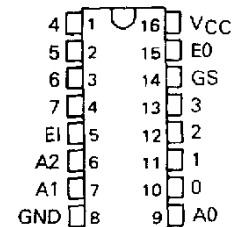
SN74LS147, SN74LS148 . . . D OR N PACKAGE

(TOP VIEW)

## '147, 'LS147



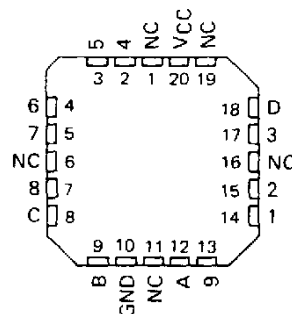
## '148, 'LS148



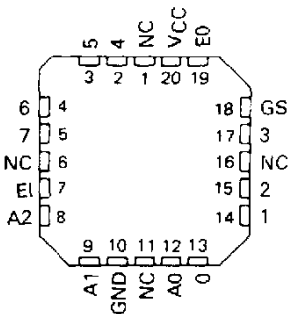
## SN54LS147, SN54LS148 . . . FK PACKAGE

(TOP VIEW)

## 'LS147



## 'LS148



NC - No internal connection

## '148, 'LS148

FUNCTION TABLE

INPUTS								OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS EO
H	X	X	X	X	X	X	X	X	H	H	H	H H
L	H	H	H	H	H	H	H	H	H	H	H	H L
L	X	X	X	X	X	X	X	L	L	L	L	L H
L	X	X	X	X	X	X	L	H	L	L	H	L H
L	X	X	X	X	X	L	H	H	L	H	L	L H
L	X	X	X	X	L	H	H	H	L	H	H	L H
L	X	X	X	L	H	H	H	H	L	H	L	L H
L	X	X	L	H	H	H	H	H	H	L	H	L H
L	X	L	H	H	H	H	H	H	H	H	L	L H
L	L	H	H	H	H	H	H	H	H	H	H	L H

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TEXAS  
INSTRUMENTS

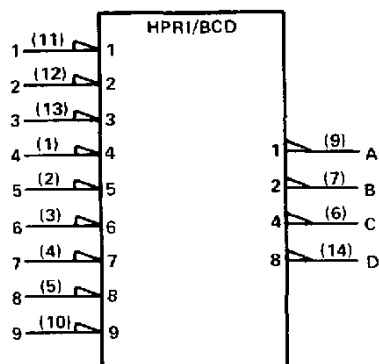
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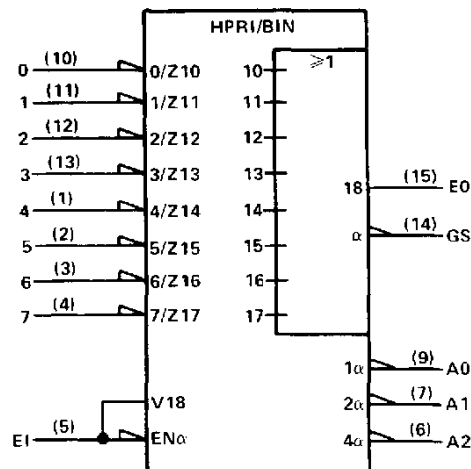
**SN54147, SN54148, SN54LS147, SN54LS148,  
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148**  
**10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

**logic symbols†**

**'147, 'LS147**



**'148, 'LS148**

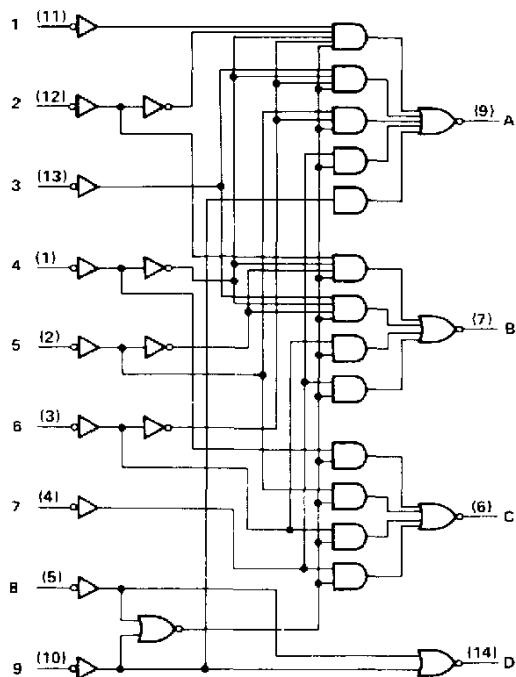


†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

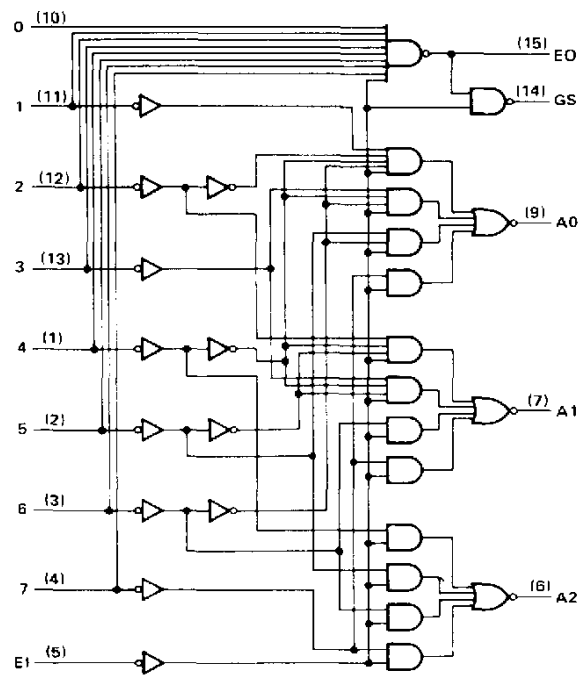
Pin numbers shown are for D, J, N, and W packages.

**logic diagrams**

**'147, 'LS147**



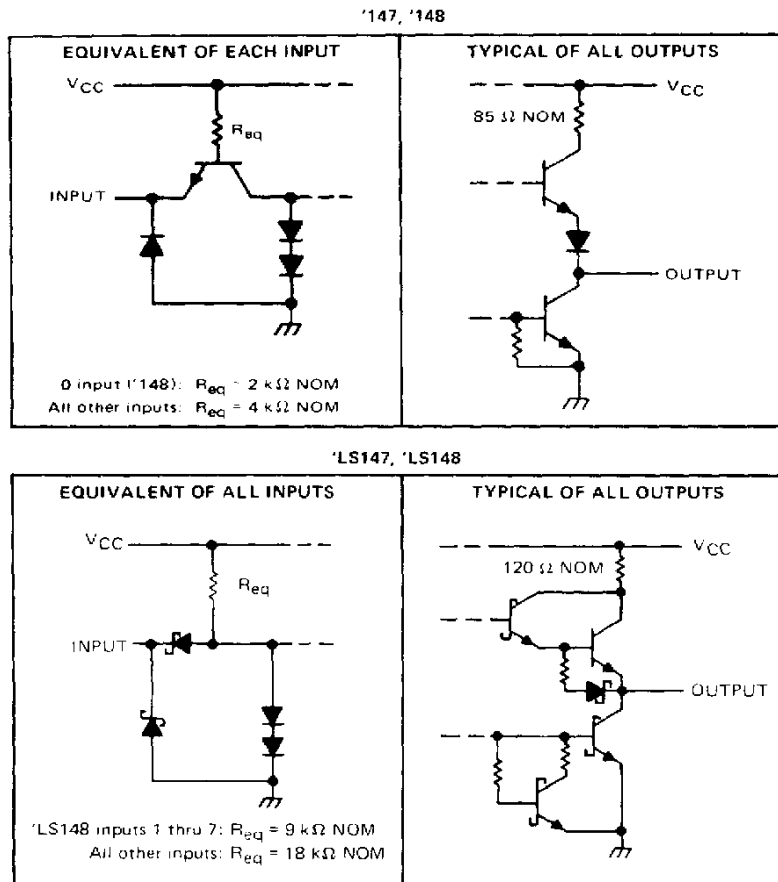
**'148, 'LS148**



Pin numbers shown are for D, J, N, and W packages.

**SN54147, SN54148, SN54LS147, SN54LS148,  
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148  
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

**schematics of inputs and outputs**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage: '147, '148	5.5 V
'LS147, 'LS148	7 V
Interemitter voltage: '148 only (see Note 2)	5.5 V
Operating free-air temperature range: SN54', SN54LS Circuits	-55°C to 125°C
SN74', SN74LS Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.  
2. This is the voltage between two emitters of a multiple-emitter transistor. For '148 circuits, this rating applies between any two of the eight data lines, 0 through 7.

**recommended operating conditions**

	SN54'			SN74'			SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-800			-800			-400			-400	$\mu$ A
Low-level output current, $I_{OL}$			16			16			4			8	mA
Operating free-air temperature, $T_A$	-55		125	0		70	-55		125	0		70	°C

**TEXAS  
INSTRUMENTS**

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**SN54147, SN54148, SN74147, SN74148 (TIM9907)**  
**10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	'147			'148			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage				0.8			0.8	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA			-1.5			-1.5	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -800 µA	2.4	3.3		2.4	3.3		V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 16 mA	0.2	0.4		0.2	0.4		V
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V		1			1		mA
I <sub>IH</sub>	High-level input current	0 input						40	µA
		Any input except 0		40				80	
I <sub>IL</sub>	Low-level input current	0 input						-1.6	mA
		Any input except 0		-1.6				-3.2	
I <sub>OS</sub>	Short-circuit output current <sup>§</sup>	V <sub>CC</sub> = MAX	-35	-85		-35	-85		mA
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX, Condition 1		50	70		40	60	mA
		See Note 3, Condition 2		42	62		35	55	

NOTE 3: For '147, I<sub>CC</sub> (condition 1) is measured with input 7 grounded, other inputs and outputs open; I<sub>CC</sub> (condition 2) is measured with all inputs and outputs open. For '148, I<sub>CC</sub> (condition 1) is measured with inputs 7 and E1 grounded, other inputs and outputs open; I<sub>CC</sub> (condition 2) is measured with all inputs and outputs open.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time.

**SN54147, SN74147 switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

PARAMETER <sup>¶</sup>	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Any	Any	In-phase output	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 400 Ω, See Note 4		9	14	ns
t <sub>PHL</sub>						7	11	
t <sub>PLH</sub>	Any	Any	Out-of-phase output			13	19	ns
t <sub>PHL</sub>						12	19	

**SN54148, SN74148 switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**

PARAMETER <sup>¶</sup>	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<sup>1</sup> PLH	1 thru 7	A0, A1, or A2	In-phase output	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 400 Ω, See Note 4	10	15	ns	
<sup>1</sup> PHL					9	14		
<sup>1</sup> PLH	1 thru 7	A0, A1, or A2	Out-of-phase output		13	19	ns	
<sup>1</sup> PHL					12	19		
<sup>1</sup> PLH	0 thru 7	EO	Out-of-phase output		6	10	ns	
<sup>1</sup> PHL					14	25		
<sup>1</sup> PLH	0 thru 7	GS	In-phase output		18	30	ns	
<sup>1</sup> PHL					14	25		
<sup>1</sup> PLH	E1	A0, A1, or A2	In-phase output		10	15	ns	
<sup>1</sup> PHL					10	15		
<sup>1</sup> PLH	E1	GS	In-phase output		8	12	ns	
<sup>1</sup> PHL					10	15		
<sup>1</sup> PLH	E1	EO	In-phase output		10	15	ns	
<sup>1</sup> PHL					17	30		

¶ t<sub>PLH</sub> = propagation delay time, low-to-high-level output

t<sub>PHL</sub> = propagation delay time, high-to-low-level output

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

# **SN54LS147, SN54LS148, SN74LS147, SN74LS148** **10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54LS*		SN74LS*		UNIT			
				MIN	TYP‡	MAX	MIN		TYP‡	MAX	
V <sub>IH</sub>	High-level input voltage				2		2	V			
V <sub>IL</sub>	Low-level input voltage					0.7		0.8	V		
V <sub>IK</sub>	Input clamp voltage		V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5		-1.5	V		
V <sub>OH</sub>	High-level output voltage		V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -400 µA		2.5	3.4		2.7	3.4	V	
V <sub>OL</sub>	Low-level output voltage		V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>ILmax</sub>	I <sub>OL</sub> = 4 mA		0.25	0.4		0.25	0.4	V
				I <sub>OL</sub> = 8 mA					0.35	0.5	
I <sub>I</sub>	Input current at maximum input voltage	'LS148 inputs 1 thru 7	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V			0.2		0.2	mA		
		All other inputs				0.1		0.1			
I <sub>IH</sub>	High-level input current	'LS148 inputs 1 thru 7	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			40		40	µA		
		All other inputs				20		20			
I <sub>IL</sub>	Low-level input current	'LS148 inputs 1 thru 7	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.8		-0.8	mA		
		All other inputs				-0.4		-0.4			
I <sub>OS</sub>	Short-circuit output current§		V <sub>CC</sub> = MAX		-20	-100	-20	-100	mA		
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX, See Note 5	Condition 1		12	20		12	20	mA	
			Condition 2		10	17		10	17	mA	

NOTE 5: For LS147, I<sub>CC</sub> (condition 1) is measured with input 7 grounded, other inputs and outputs open. I<sub>CC</sub> (condition 2) is measured with all inputs and outputs open. For LS148, I<sub>CC</sub> (condition 1) is measured with inputs 7 and E1 grounded, other inputs and outputs open. I<sub>CC</sub> (condition 2) is measured with all inputs and outputs open.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25° C.

§ Not more than one output should be shorted at a time.

## **SN54LS147, SN74LS147 switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25° C**

PARAMETER <sup>1</sup>	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Any	Any	In-phase output	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ, See Note 4	12	18	ns	
t <sub>PHL</sub>					12	18		
t <sub>PLH</sub>	Any	Any	Out-of-phase output		21	33	ns	
t <sub>PHL</sub>					15	23		

## **SN54LS148, SN74LS148 switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25° C**

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	1 thru 7	A0, A1, or A2	In-phase output	$C_L = 15\text{ pF}$ , $R_L = 2\text{ k}\Omega$ , See Note 4	14	18	ns	
$t_{PHL}$					15	25		
$t_{PLH}$	1 thru 7	A0, A1, or A2	Out-of-phase output		20	36	ns	
$t_{PHL}$					16	29		
$t_{PLH}$	0 thru 7	EO	Out-of-phase output		7	18	ns	
$t_{PHL}$					25	40		
$t_{PLH}$	0 thru 7	GS	In-phase output		35	55	ns	
$t_{PHL}$					9	21		
$t_{PLH}$	EI	A0, A1, or A2	In-phase output		16	25	ns	
$t_{PHL}$					12	25		
$t_{PLH}$	EI	GS	In-phase output		12	17	ns	
$t_{PHL}$					14	36		
$t_{PLH}$	EI	EO	In-phase output		12	21	ns	
$t_{PHL}$					23	35		

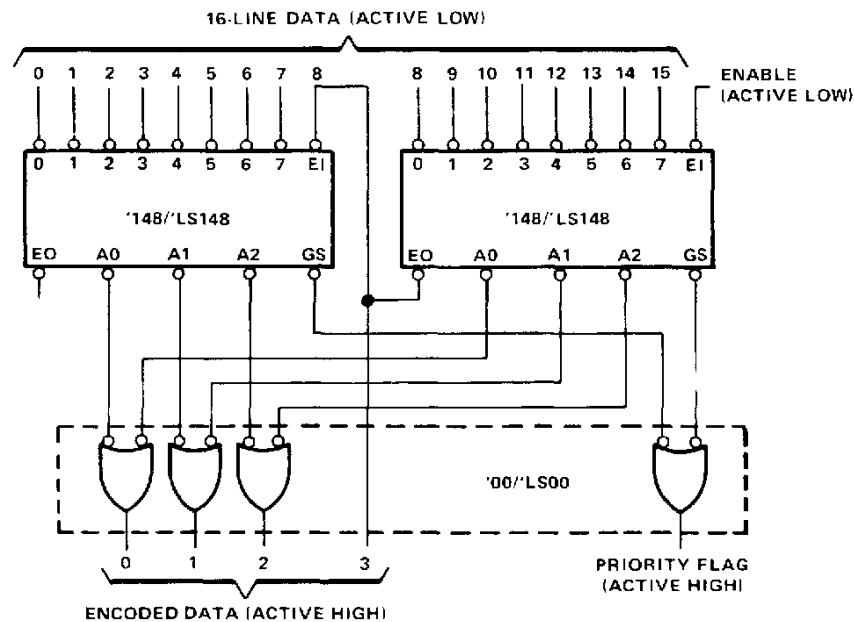
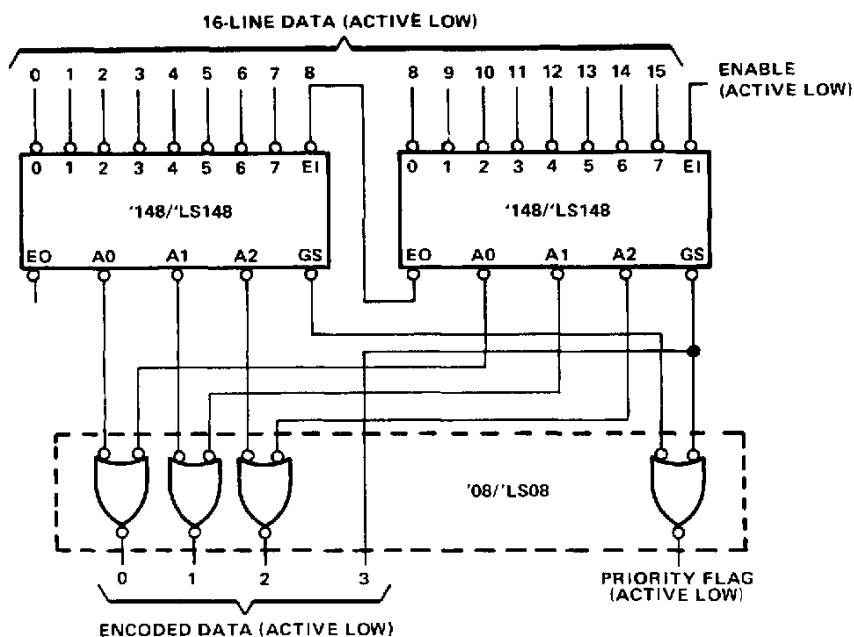
\* t<sub>PLH</sub> = propagation delay time, low to high level output

t<sub>PHL</sub> = propagation delay time, high to low level output

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

**SN54147, SN54148 (TIM9907), SN54LS147, SN54LS148,  
SN74147, SN74148, SN74LS147, SN74LS148  
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

**TYPICAL APPLICATION DATA**



Since the '147/'LS147 and '148/'LS148 are combinational logic circuits, wrong addresses can appear during input transients. Moreover, for the '148/'LS148 a change from high to low at input EI can cause a transient low on the GS output when all inputs are high. This must be considered when strobing the outputs.

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SN54148J - <http://www.ti.com/product/sn54148j?HQS=TI-null-null-dscatalog-df-pf-null-ww>  
74LS148 - <http://www.ti.com/product/74ls148?HQS=TI-null-null-dscatalog-df-pf-null-ww>  
SN54148W - <http://www.ti.com/product/sn54148w?HQS=TI-null-null-dscatalog-df-pf-null-ww>  
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SN74148 - <http://www.ti.com/product/sn74148?HQS=TI-null-null-dscatalog-df-pf-null-ww>  
SN74148N - <http://www.ti.com/product/sn74148n?HQS=TI-null-null-dscatalog-df-pf-null-ww>  
SNJ54148J - <http://www.ti.com/product/sn54148j?HQS=TI-null-null-dscatalog-df-pf-null-ww>  
SN74147 - <http://www.ti.com/product/sn74147?HQS=TI-null-null-dscatalog-df-pf-null-ww>  
SN54LS147W - <http://www.ti.com/product/sn54ls147w?HQS=TI-null-null-dscatalog-df-pf-null-ww>  
SN74LS147 - <http://www.ti.com/product/sn74ls147?HQS=TI-null-null-dscatalog-df-pf-null-ww>  
SN74LS147D - <http://www.ti.com/product/sn74ls147d?HQS=TI-null-null-dscatalog-df-pf-null-ww>  
SN74LS147N - <http://www.ti.com/product/sn74ls147n?HQS=TI-null-null-dscatalog-df-pf-null-ww>



## DM74157

### Quad 2-Line to 1-Line Data Selectors/Multiplexer

#### General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs.

#### Applications

- Expand any data input point
- Multiplex dual data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

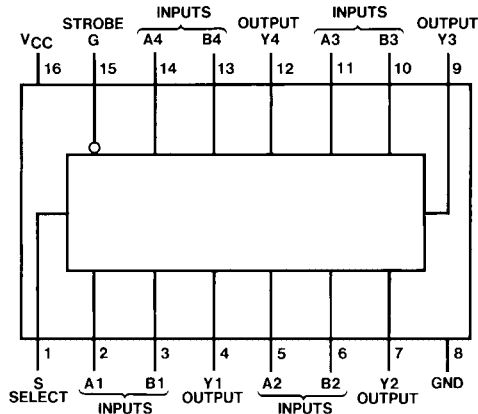
#### Features

- Buffered inputs and outputs
- Typical propagation time 9 ns
- Typical power dissipation 150 mW

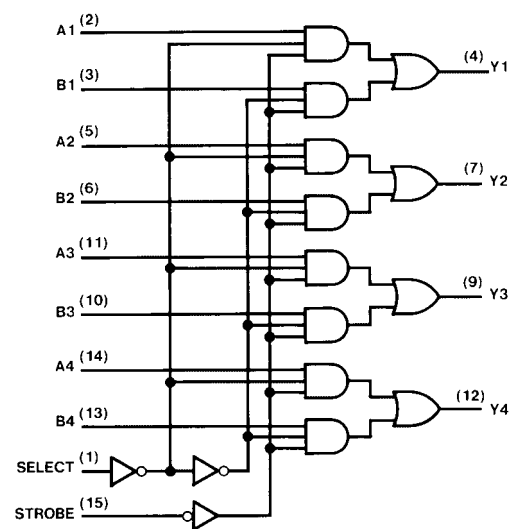
#### Ordering Code:

Order Number	Package Number	Package Description
DM74157N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

#### Connection Diagram



#### Logic Diagram



#### Function Table

Inputs				Output Y
Strobe	Select	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = HIGH Level, L = LOW Level, X = Don't Care

**Absolute Maximum Ratings**(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
$V_{CC}$	Supply Voltage	4.75	5	5.25	V
$V_{IH}$	HIGH Level Input Voltage	2			V
$V_{IL}$	LOW Level Input Voltage			0.8	V
$I_{OH}$	HIGH Level Output Current			–0.8	mA
$I_{OL}$	LOW Level Output Current			16	mA
$T_A$	Free Air Operating Temperature	0		70	°C

**Electrical Characteristics**

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
$V_I$	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -12 \text{ mA}$			–1.5	V
$V_{OH}$	HIGH Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$	2.4	3.4		V
$V_{OL}$	LOW Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IH} = \text{Min}, V_{IL} = \text{Max}$			0.4	V
$I_I$	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 5.5 \text{ V}$			1	mA
$I_{IH}$	HIGH Level Input Current	$V_{CC} = \text{Max}, V_I = 2.4 \text{ V}$			40	μA
$I_{IL}$	LOW Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4 \text{ V}$			–1.6	mA
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 3)	–18		–55	mA
$I_{CC}$	Supply Current	$V_{CC} = \text{Max}$ (Note 4)		30	48	mA

**Note 2:** All typicals are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ \text{C}$ .

**Note 3:** Not more than one output should be shorted at a time.

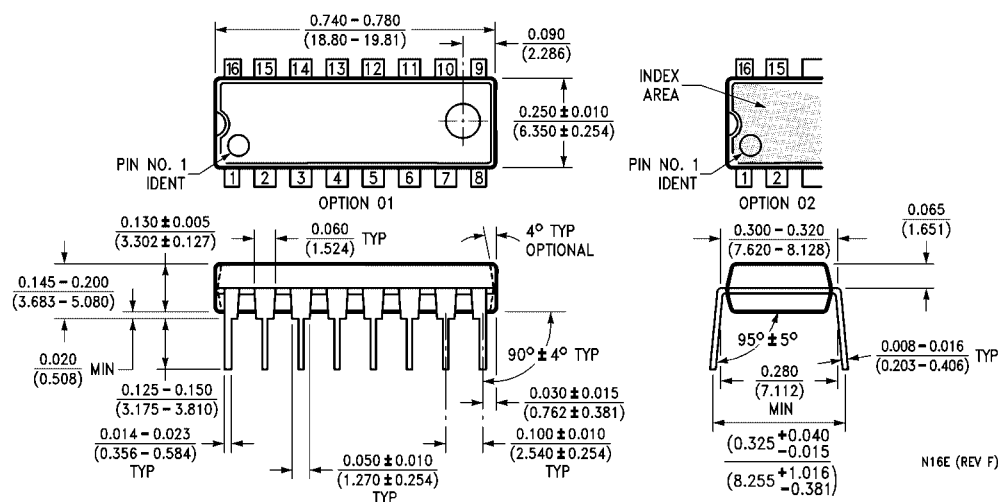
**Note 4:**  $I_{CC}$  is measured with 4.5V applied to all inputs and all outputs OPEN.

**Switching Characteristics**

at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ \text{C}$

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega, C_L = 15 \text{ pF}$		Units
			Min	Max	
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Data to Y		14	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Data to Y		14	ns
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Strobe to Y		20	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Strobe to Y		21	ns
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Select to Y		23	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Select to Y		27	ns

# Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E**

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