TOPIC:
Shift Registers

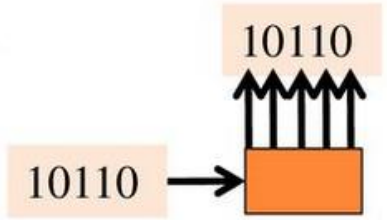
Shift Register

The Shift Register is another type of sequential logic circuit that can be used for the storage or the transfer of binary data

- An *n*-bit register has a group of *n* flip-flops and some logic gates and is capable of storing *n* bits of information.
- The flip-flops store the information while the gates control when and how new information is transferred into the register.
- Some functions of register:
  - retrieve data from register
  - store/load new data into register (serial or parallel)
  - shift the data within register (left or right)

Shift Register

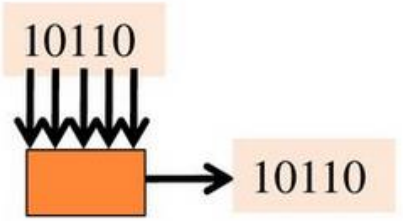
- Serial-in to Parallel-out (SIPO) - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.



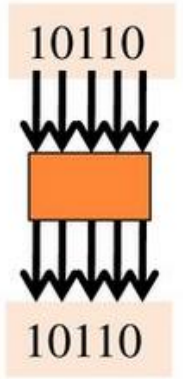
- Serial-in to Serial-out (SISO) - the data is shifted serially “IN” and “OUT” of the register, one bit at a time in either a left or right direction under clock control.

Shift Register

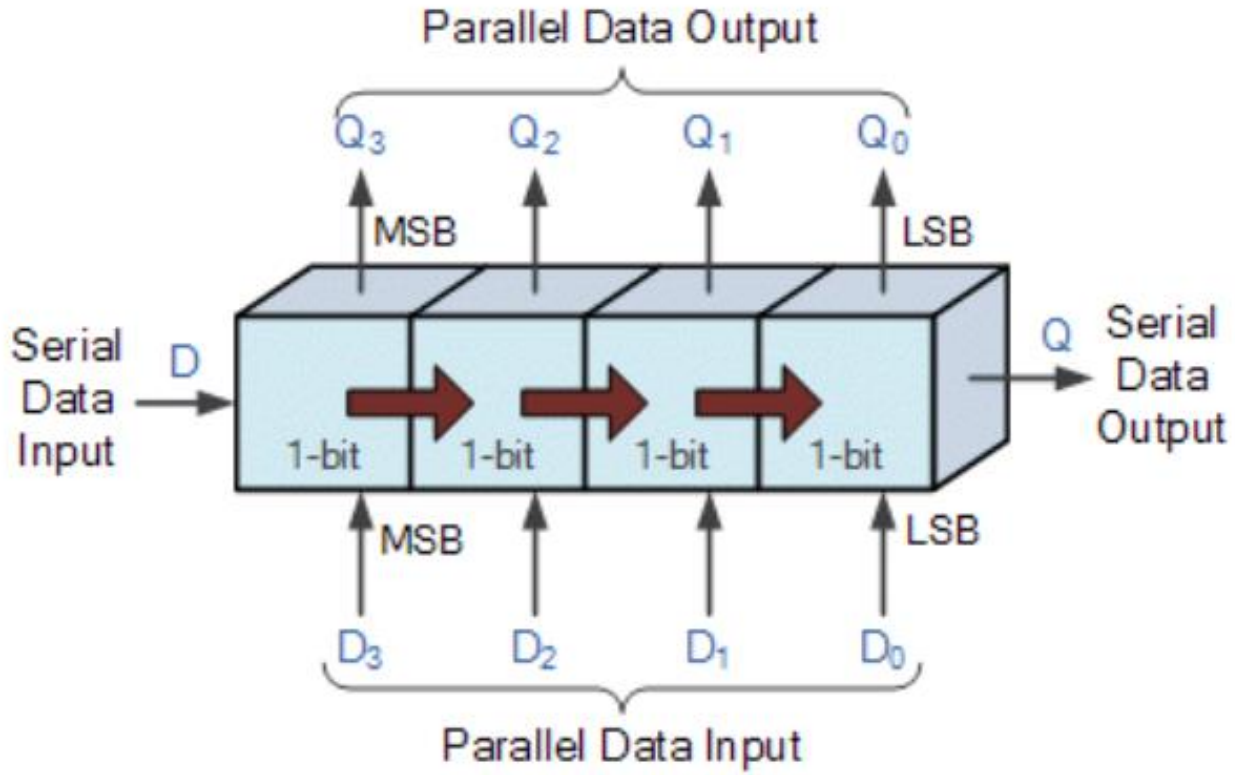
- Parallel-in to Serial-out (PISO) - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.



- Parallel-in to Parallel-out (PIPO) - the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.



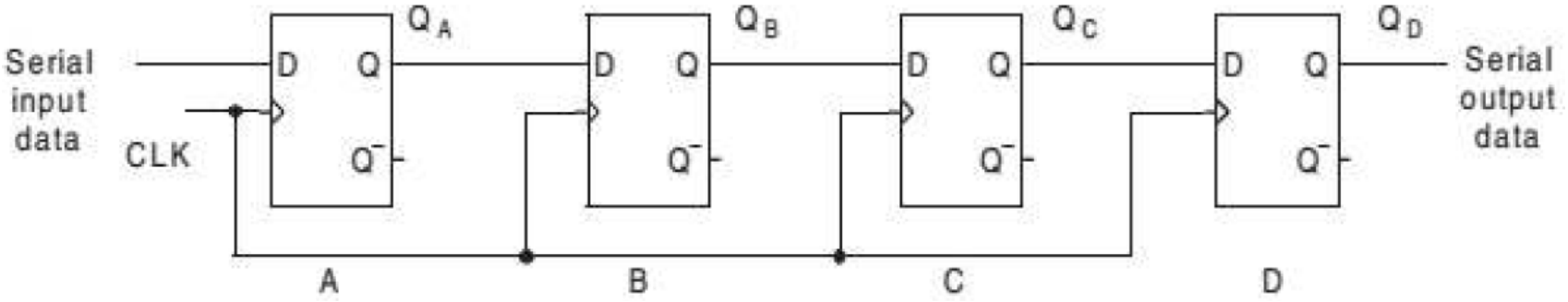
Shift Register



Shift Register

Serial-in to Serial-out (SISO) Shift Register

In the shift register using D flip flop, D input of the left most flip flop is used as a serial input line. To input 1, one should apply 1 at the D input.

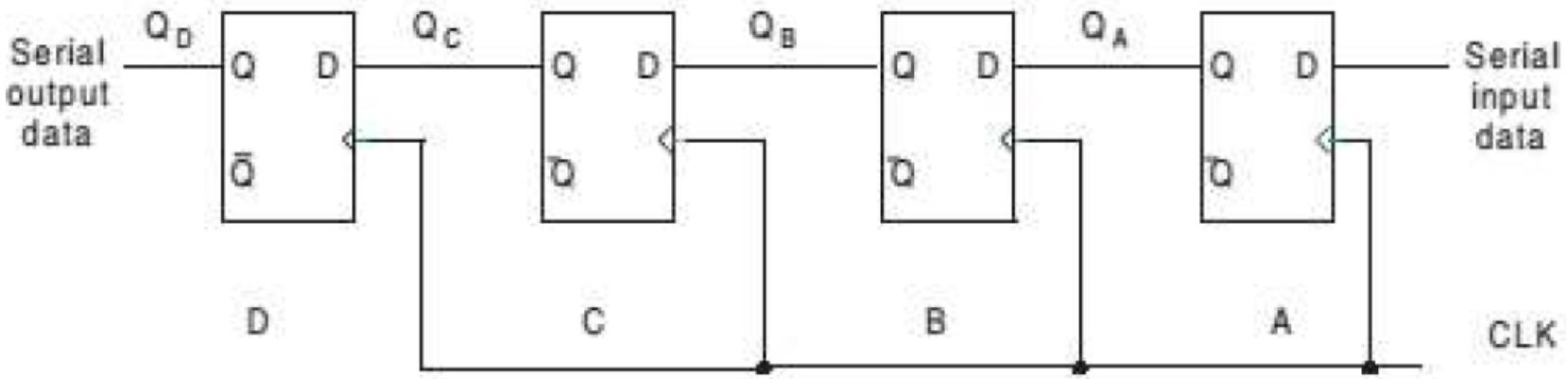


Timing pulse	Q_A	Q_B	Q_C	Q_D	*Serial output at* Q_D
Initial value	0	0	0	0	0
After 1st clock pulse	1	0	0	0	0
After 2nd clock pulse	1	1	0	0	0
After 3rd clock pulse	0	1	1	0	0
After 4th clock pulse	1	0	1	1	1

For example, consider that all the stages are reset and a logical input 1011 is applied at the serial input line connected to stage A. The data after four clock pulses is shown in above Table.

Shift Register

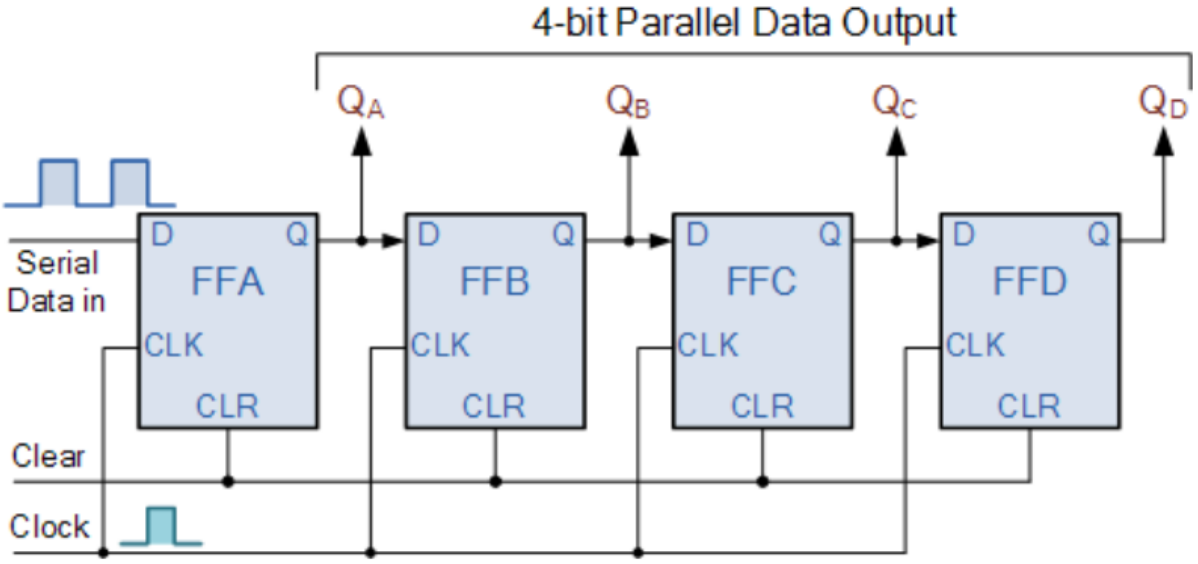
Serial-in to Serial-out (SISO) Shift Register



4-bit Serial-in to Serial-out Shift-Left Register

Serial-in to Parallel-out (SIPO) Shift Register

- In this type of register, the data is shifted in serially, but shifted out in parallel. To obtain the output data in parallel, it is required that all the output bits are available at the same time.
- Once the data is stored in the flip-flop the bits are available simultaneously. The basic configuration of a serial-in–parallel-out shift register is shown in below.



4-bit Serial-in to Parallel-out Shift Register

Shift Register

Serial-in to Parallel-out (SIPO) Shift Register

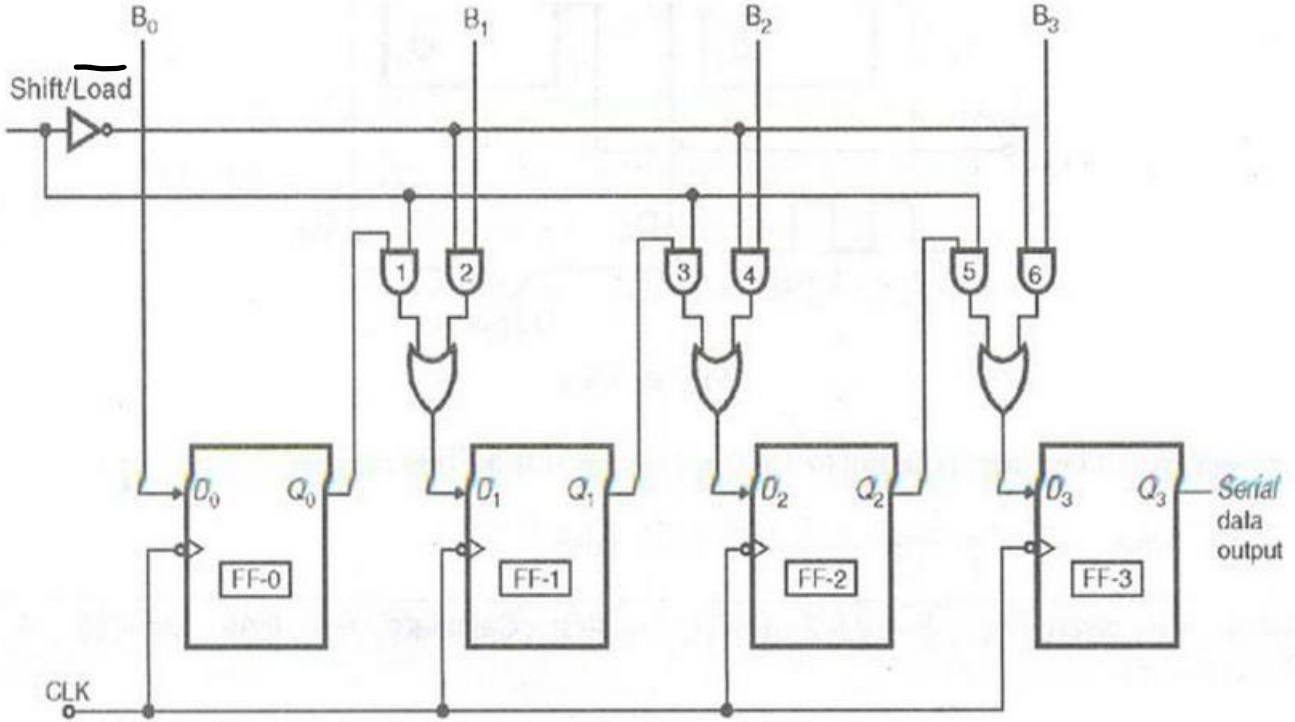
CLK Pulse	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	0	1	0
4	1	1	0	1

SIPO Shift Register Truth Table

Basic Data Movement Through A Shift Register

Parallel-in to Serial-out (PISO) Shift Register

In the preceding two cases the data was shifted into the registers in a serial manner. Here we develop an idea for the parallel entry of data into the register. Here the data bits are entered into the flip-flops simultaneously, rather than a bit-by-bit basis.



4-bit Parallel-in to Serial-out Shift Register

Shift Register

Parallel-in to Serial-out (PISO) Shift Register

Load Mode

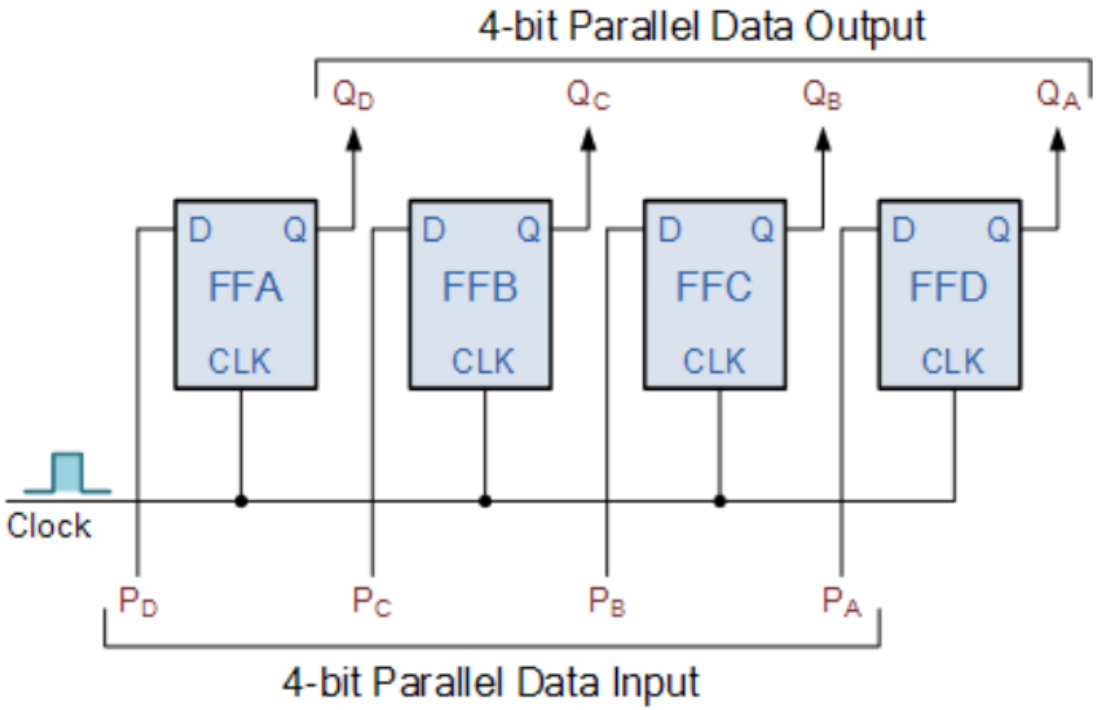
- Load mode s active low device, they gives s/g to AND gate 2,4,6 & they become active. They pass B0,B1,B2,B3 bits to the corresponding flipflops.
- On the low going edge of clock the binary inputs B0,B1,B2,B3 will get loaded into the corresponding flipflops. Thus parallel loading is take place.

- Shift mode is active high device, they gives s/g to AND gate 1,3,5 & they become active at that time AND gate 2,4,6 become inactive. Hence parallel loading is not possible therefore data shifting of data from left to right, bit by bit.

Shift Mode

Shift Register

Parallel-in to Parallel-out (PIPO) Shift Register



4-bit Parallel-in to Parallel-out Shift Register

Shift Register

Parallel-in to Parallel-out (PIPO) Shift Register

- The 4 bit binary input B0,B1,B2,B3 is applied to the data input D0,D1,D2,D3 respectively.
- A negative clock pulse is applied the binary input will be loaded into flip flop simultaneously and loaded bit will appear at o/p side.
- Only one clock pulse is essential to load all the bits.

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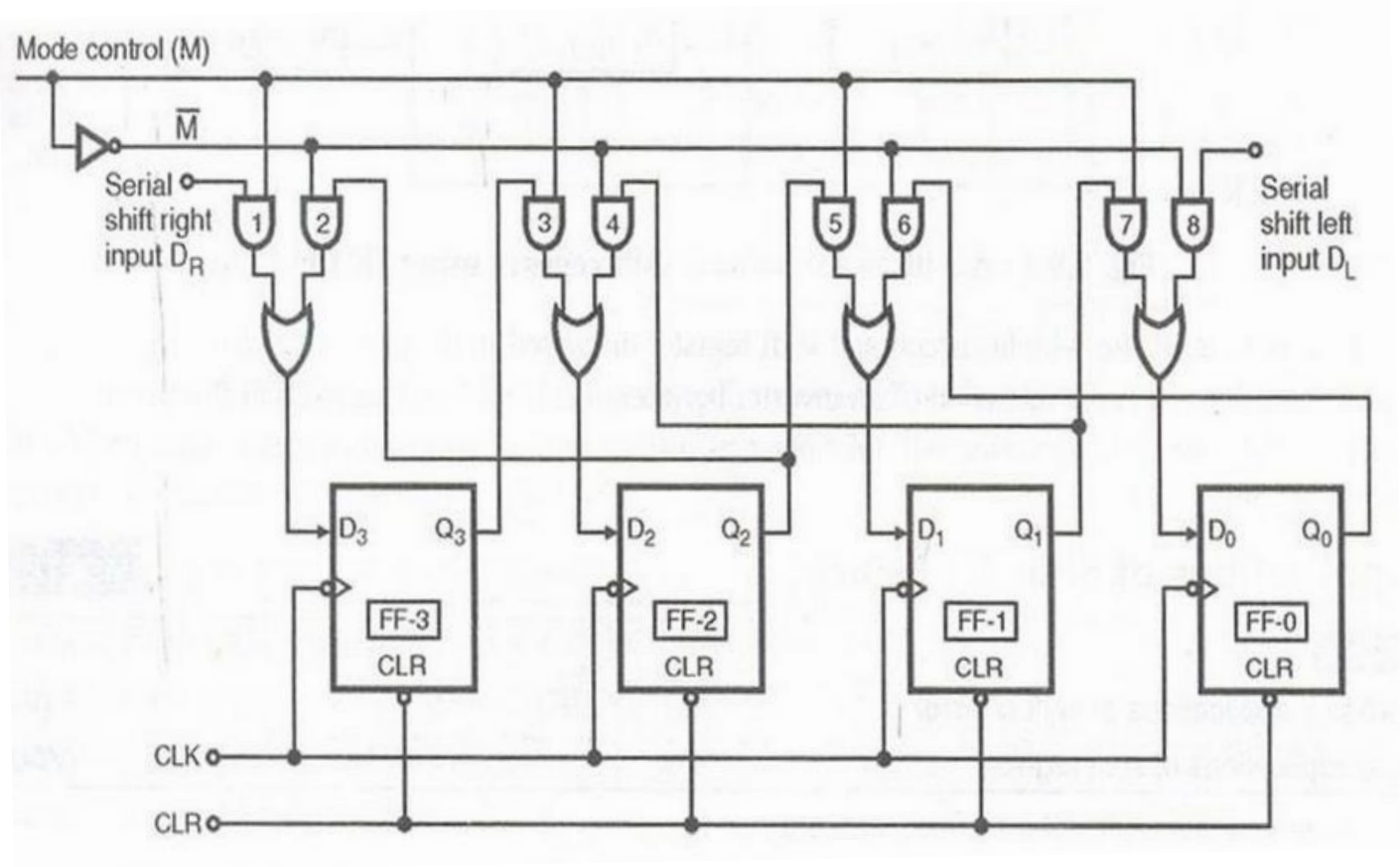
Shift Register

Bidirectional Shift Register



Shift Register

Bidirectional Shift Register

- M=1= Shift right operation
- M=1 then AND gate 1,3,5,7 are enabled whereas the remaining AND gate 2,4,6,8 will be disable.
- Data D_R shifted bit by bit from FF3 to FF0, on the application of clock pulse.

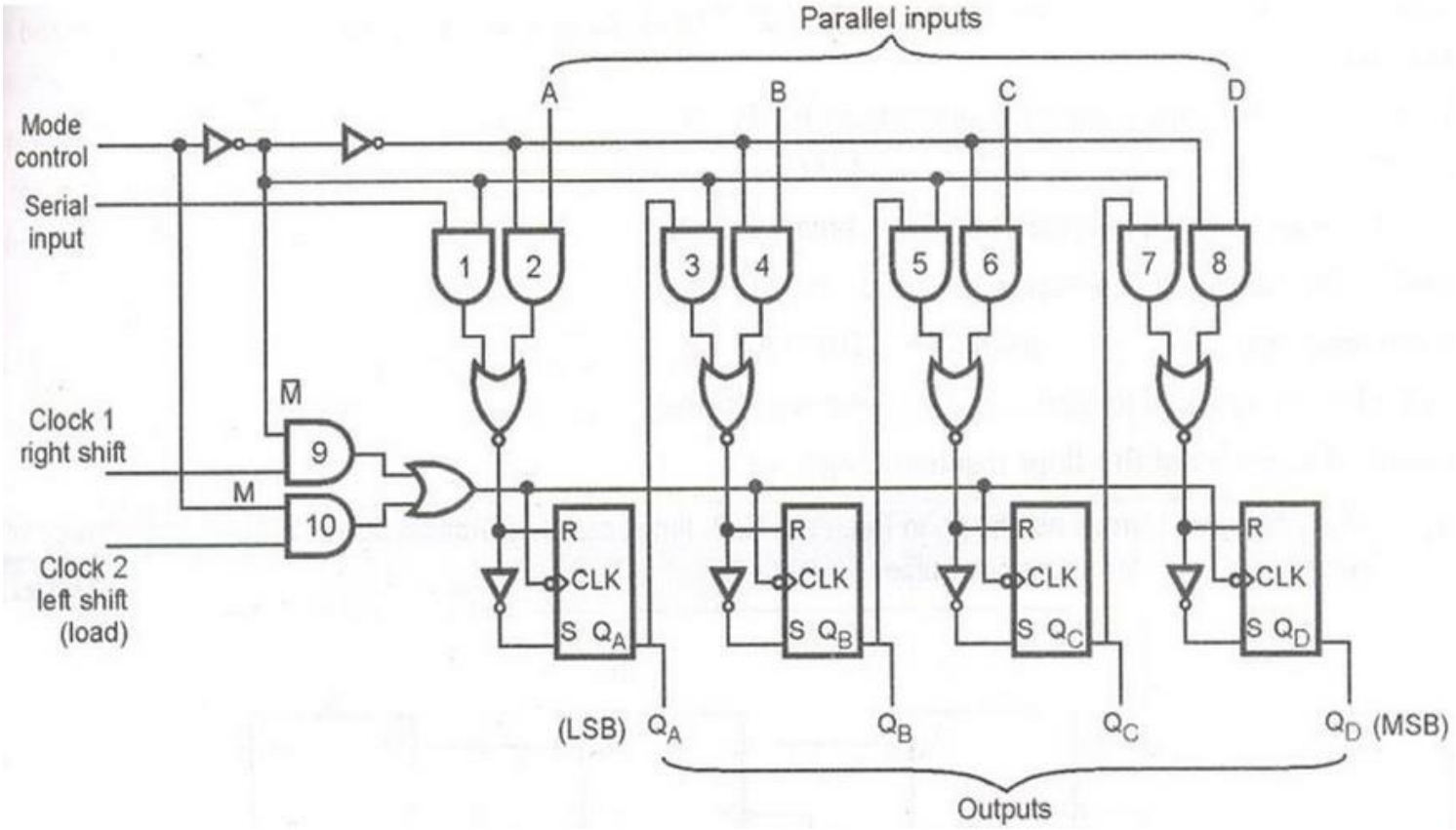
Shift Right Operation

Shift Left Operation

- M=0=Shift left operation
- M=0 then AND gate 2,4,6,8 are enabled whereas the remaining AND gate 1,3,5,7 will be disable.
- Data D_L shifted bit by bit from FF0 to FF3, on the application of clock pulse.
- M changed only when clock =0 otherwise data stored in the register may be altered.

Shift Register

Universal Shift Register



Universal Shift Register

The universal shift register can be defined as “The register which can be used to shift the data in both the directions like left, right and can load parallel data as well”.

This register can perform three types of operations, stated below.

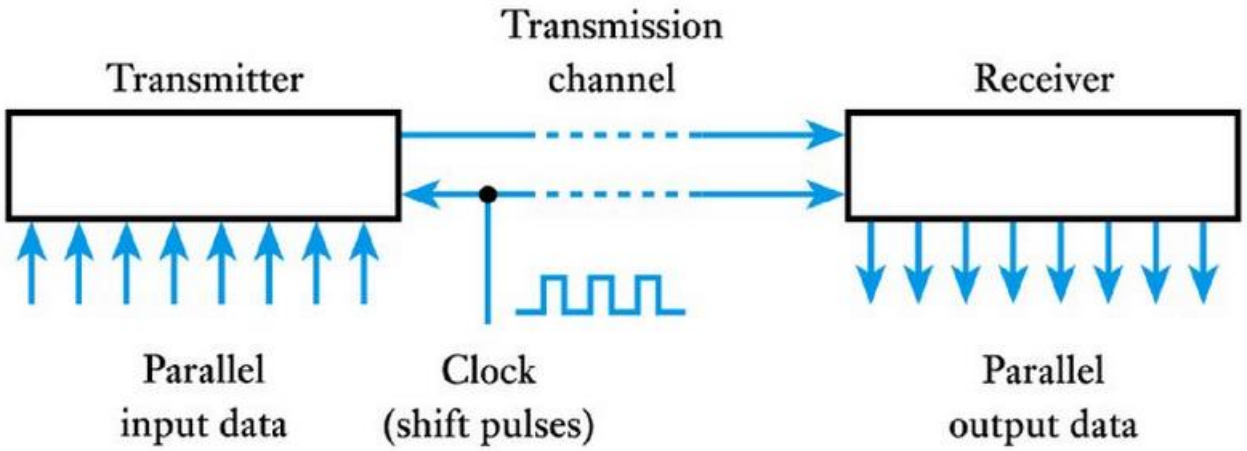
- Parallel loading
- Shifting left
- Shifting right

Applications of Shift Registers

1. Registers are used in digital electronic devices like computers as
   - Temporary data storage
   - Data transfer
   - Data manipulation
   - As counters
2. Shift registers are used in computers as memory elements.
3. Shift registers are used for counter designing.

Applications of Shift Registers

An application of Shift register in serial/parallel and parallel/serial conversion used in serial communication



Applications of Shift Registers

- *Serial in – serial out* register are used for time delays.
- *Serial in – parallel out* registers are used for converting the data from serial form to parallel form. So these are also called “Serial to parallel converters”.
- *Parallel in – serial out* registers are used for converting the data from parallel form to serial form. So these are also called “Parallel to serial converters”.