Course Plan

CHITKARA
UNIVERSITY

A. Course Handout (Version 1.1) | Last updated on 2nd Jan, 2023

Institute/School Name	Chitkara University Institute of Engineering & Technology		
Department Name	Department of Interdisciplinary Courses in Engineering		
Programme Name	Bachelor of Engineering, Computer Science & Engineering		
Course Name	Computer Organisation and Architecture	Session	2022-2023
Course Code	CS157	Semester/Batch	4th/2021
L-T-P (Per Week)	3-0-0	Course Credit	03
Course Coordinator	Dr Jyoti		

1. Objective of the Course

The course provides a wide scope of learning & understanding of the subject. The main objectives of the course are:

- To familiarize the students with the basic understanding of computer system architecture and digital circuits.
- Implementation of the machine instructions for the operation of the computer system.
- To Interpret the concept of micro-programmed control, parallel processing and pipelining.
- To Illustrate concepts regarding input-output interfacing and Direct Memory Access.
- To familiarize concepts of Analog to Digital and Digital to Analog convertors.

2. Course Learning Outcome:

Students will be able to:

CLO01: To understand and identify the fundamental organization of the computer system architecture.
CLO02: To apply the concept of Arithmetic Operations in various applications.
CLO03: To conceptualize the micro-programmed control, parallel processing and pipelining.
CLO04: To understand I/O organization and Direct Memory Access.
CLO05: To understand the concepts of Analog to Digital and Digital to Analog convertors.

CLO-PO mapping grid |Program outcomes (POs) are available as a part of Academic Program Guide (APG) at

Course Learning Outcomes	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CLO01	H	M								L		L
CLO02	H			L	M							
CLO03			M			H	H					L
CLO04				M			H					
CLO05	H		M		M							

3. Recommended Books (Reference Books/Text Books):

B01: 'Computer System Architecture' by M. Morris Mano, Pearson Education, 2008
B02: John P Hayes, "Computer Architecture and Organization", Prentice Hall
B03: Malvino Leech, Digital Electronics Fundamentals
B04: David A Patterson, Computer Architecture A Quantitative Approach, Pearson Education
B05: J.P. Hayes, Computer System Architecture, Pearson Education Asia

B06: William Stallings, Computer Organization and Architecture: Designing for Performance, Prentice-Hall India

4. Other readings & relevant websites:

S. No.	Link of Journals, Magazines, websites and Research Papers
1	https://nptel.ac.in/courses/106106134
2	https://nptel.ac.in/courses/106104073

5. Recommended Tools and Platforms

- NPTEL
- SWAYAM

6. Course Plan:

Lecture Number.	Topic(s)	Books
1-2	Introduction to Course Handout Introduction to Computer Organization & Architecture, Overview of Digital System	B02, B03, B05, B06
3-5	Introduction to Flip-Flops and its types	B03
6-8	Shift Registers: SIPO, SISO, PISO and PIPO	B03
9-11	Design of Synchronous and Asynchronous counters.	B03
12-14	Basic Computer Organization: Instruction Codes, Computer Registers, Computer Instructions.	B01, B03
15	Timing and Control, Instruction Cycle	B01, B02, B06
16-17	Memory Reference Instructions, Input-Output and Interrupts	B01, B02, B06
18	Micro-programmed Control: Control Memory, Address Sequencing	B01, B02, B06
19-20	Micro-program Examples and Design of Control Unit	B01, B02
21	Central Processing Unit: Introduction, General Register Organization	B01, B02, B06
22	Stack Organization and Instruction Format	B01, B02, B06
23-25	Addressing Modes, Data Transfer and Manipulation	B01, B06
26-28	Program Control: Status bits, Conditional Branch Instructions, Program Interrupts & Types	B01, B02, B06
29-30	RISC and CISC Characteristics	B01, B04
31-33	Introduction to Parallel Processing, Pipelining	B01, B02, B06
34-35	Input-Output Organization: I/O Interface	B01, B02, B06
36	Asynchronous Data Transfer	B01, B02, B06
37	Modes of Transfer	B01, B02, B06

38-39	Direct Memory Access (DMA), DMA Transfer, Input-Output Processor (IOP), CPU-IOP Communication.	B01, B03
40-42	D/A Converter and A/D converters: Introduction, Digital to Analog Conversion, R2RDAC, Weighted Resistor DAC	B03
43-45	A/D Converter: Analog to Digital Conversion using Successive Approximation Method, Dual Slope Method	B03

7. Delivery/Instructional Resources

Lecture Number	Topic(s)	PPT (Link of ppts on the central server)	Industry Expert Session (If yes: link of ppts on the central server)	Web References	Audio-Video
1-5	Introduction to Computer Organization & Architecture, Overview of Digital System, Introduction to Flip-Flops and its types.			https://nitsri.ac.in/Department/Electronics%20&%20Communication%20Engineering/Chapter 1-Introduction.pdf https://www.cuemath.com/numbers/number-systems/	https://www.youtube.com/watch?v=q6oiRtKTpX4 https://www.youtube.com/watch?v=jmOPGDSSBkl https://www.youtube.com/watch?v=i-tnQMDdbfc
6-11	Shift Registers: SIPO, SISO, PISO and PIPO, Design of Synchronous and Asynchronous counters.			https://www.tutorialspoint.com/what-are-computer-registers-in-computer-architecture	https://www.youtube.com/watch?v=Aft2vPt9tkc https://www.youtube.com/watch?v=Vt3IFnBwgpo https://www.youtube.com/watch?v=lecj9xmlfXM
12-14	Basic Computer Organization: Instruction Codes, Computer Registers, Computer Instructions.			https://www.tutorialspoint.com/what-are-computer-registers-in-computer-architecture	https://www.youtube.com/watch?v=Aft2vPt9tkc https://www.youtube.com/watch?v=Vt3IFnBwgpo https://www.youtube.com/

					/watch?v=iec j9xmIfXM
15	Timing and Control, Instruction Cycle			https://www.Ja vatpoint.com/In struction-cycle	https://www. youtube.com /watch?v=Bs h_WYIILXs
16-17	Memory Reference Instructions, Input-Output and Interrupt			https://nptel.ac .In/courses/106 /103/10610306 8/	https://www. youtube.com /watch?v=0X ybwAbup- w&list=PL59E 5B57A04EAE 09C&index=3 3 https://www. youtube.com /watch?v=LT VCbvIZbKU
18	Micro-programmed Control: Control Memory, Address Sequencing			https://nptel.ac .in/courses/106 /103/10610306 8/	https://www. youtube.com /watch?v=iG HzG5xR_nA
19-20	Micro-program Examples and Design of Control unit			https://nptel.ac .in/courses/106 /103/10610306 8/	https://www. youtube.com /watch?v=X6 GbaLQUuz8
21	Central Processing Unit: Introduction, General Register Organization			https://nptel.ac .in/courses/106 /103/10610306 8/	https://www. youtube.com /watch?v=vjq nWn5PdD0
22	Stack Organization and Instruction Format			http://nptel.ac.i n/courses/1061 04073/	https://www. youtube.com /watch?v=u- sp4gBAJKI
23-25	Addressing Modes, Data Transfer and Manipulation			http://nptel.ac.i n/courses/1061 04073/	https://www. youtube.com /watch?v=p9 wxylx-j-c
26-28	Program Control: Status bits, Conditional Branch Instructions, Program Interrupts & Types			http://nptel.ac.i n/courses/1061 06092/	https://www. youtube.com /watch?v=oT mpeck2M6M
29-30	RISC and CISC Characteristics			https://nptel.ac .in/courses/106 /103/10610306 8/	https://www. youtube.com /watch?v=pt- OOSSGezc
31-33	Introduction to Parallel processing, Pipelining			https://nptel.ac .in/courses/106 /103/10610306 8/	https://www.y outube.com/w atch?v=_7Mhz h-bQDU
34-35	Input-Output Organization: I/O Interface			https://nptel.ac .in/courses/106 /103/10610306 8/	https://www.y outube.com/w atch?v=Y17TLZ CSe4M

36	Asynchronous Data Transfer			https://nptel.ac .in/courses/106 /103/10610306 8/	https://www.y outube.com/w atch?v=- gRryttl3lg
37	Modes of Transfer			https://nptel.ac .in/courses/106 /103/10610306 8/	https://www. youtube.com /watch?v=- gRryttl3lg
38-39	Direct Memory Access (DMA), DMA Transfer, Input-Output Processor (IOP), CPU-IOP Communication.			https://nptel.ac .in/courses/106 /103/10610306 8/	https://www. youtube.com /watch?v=3R fqkVyvnnc
40-42	D/A Converter and A/D converters: Introduction, Digital to Analog Conversion, R2RDAC, Weighted Resistor DAC			https://nptel.ac .in/courses/106 /103/10610306 8/	https://www.y outube.com/w atch?v=kMGa p-0XwGs https://www.y outube.com/w atch?v=LUMh ObAm1Qs
43-45	A/D Converter: Analog to Digital Conversion using Successive Approximation Method, Dual Slope Method			https://nptel.ac .in/courses/106 /103/10610306 8/	https://www. youtube.com /watch?v=Ea yOCWaiRkw

8. Action plan for different types of learners

Slow Learners	Average Learners	Fast Learners
Remedial Classes on Saturdays	Doubt-sessions	More Practical Assignments

9. Evaluation Scheme & Components:

Evaluation Component	Type of Component	No. of Assessments	Weightage of Component	Mode of Assessment
Component 1	Formative Assessments (FAs)	02*	10%	Online
Component 2	Subjective Test/Sessional Tests (STs)	02**	30%	Offline
Component 3	End Term Examinations	01	60%	Offline
Total			100%	

*Out of 02FAs, the ERP system automatically picks the best 01 FAs marks for evaluation of the FAs as final marks.
**Out of 02 STs, the ERP system automatically picks the best 01 ST marks for evaluation of the STs as final marks.

10. Details of Evaluation Components:

Evaluation Component	Description	Syllabus Covered (%)	Timeline of Examination	Weightage (%)
Component 1	FA1	Upto 40%	Week 8	10%
	FA2	41% - 80%	Week 14	
Component 2	ST 01	45%	Week 10	30%
	ST 02	46% - 80%	Week 15	
Component 3	End Term Examination*	100%	At the end of the semester	60%
Total				100%
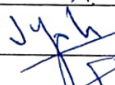
*As per Academic Guidelines minimum 90% attendance is required to become eligible for appearing in the End Semester Examination.

11. Syllabus of the Course:

S. No.	Topic (s)	No. of Lectures	Weightage %
1	Introduction to Computer Organization & Architecture, Overview of Digital System.	2	4
2	Introduction to Flip-Flops and its types	3	7
3	Shift Registers: SIPO, SISO, PISO and PIPO	3	7
4	Design of Synchronous and Asynchronous counters.	3	7
5	Basic Computer Organization: Instruction Codes, Computer Registers, Computer Instructions, Timing and Control, Memory Reference Instructions, Input-Output and Interrupts.	6	14
6	Micro-programmed Control: Control Memory, Address Sequencing, Micro program Example, General Register Organization, Stack Organization. Instruction Format.	5	11
7	Addressing Modes, Data Transfer and Manipulation.	3	7
8	Program Control: Status bits, Conditional Branch Instructions, Program Interrupts & Types,	3	7
9	RISC/CISC Characteristics.	2	4
10	Introduction to Parallel Processing, Pipelining	3	7

11	Input-Output Organization: I/O Interface, Asynchronous Data Transfer, Modes of Transfer, Direct Memory Access (DMA), DMA Transfer, DMA Controller Input-Output Processor (IOP), CPU-IOP Communication.	6	14
12	D/A Converter and A/D converters: Introduction, Digital to Analog Conversion, R2RDAC, Weighted Resistor DAC, A/D Converter: Analog to Digital Conversion using Successive Approximation Method, Dual Slope Method.	6	11

This Document is approved by:

Designation	Name	Signature
Course Coordinator	Dr Jyoti	
Program In charge	Dr Tajinder Kaur	
Dean	Dr Rajneesh Talwar	
Dean (Academic Affairs)	Dr Rajnish Sharma	
Date (DD/MM/YYYY)	02.01.2023	