

# Lab 7

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## htax\_tx\_monitor\_c.sv Code

```
htax_tx_monitor_c.sv htax_rx_monitor_c.sv
21
22
23 // TO DO : Coverpoint for htax packet field : vc (include vc=0 in illegal bin)
24 //VC :
25 VC : coverpoint tx_mon_packet.vc {
26     illegal_bins vc = {0};
27 }
28
29 // TO DO : Coverpoint for htax packet field : length (Divide range [3:63] into 16 bins)
30 //LENGTH :
31 LENGTH : coverpoint tx_mon_packet.length {
32     bins length[16] = {[3:63]};
33 }
34
35
36 // Coverpoints for Crosses
37 // TO DO : DEST_PORT cross VC
38 DEST_VC : cross DEST_PORT, VC;
39
40 // TO DO : DEST_PORT cross LENGTH
41 DEST_LENGTH : cross DEST_PORT, LENGTH;
42
43 // TO DO : VC cross LENGTH
44 VC_LENGTH : cross VC, LENGTH;
45
46
47 endgroup
48
49 covergroup cover_htax_tx_intf;
50 option.per_instance = 1;
51 option.name = "cover_htax_tx_intf";
52
53
54 // TO DO : Coverpoint for tx_outport_req: covered all the values 0001,0010,0100,1000
55 tx_outport_req : coverpoint htax_tx_intf.tx_outport_req {
56     bins outport_rq[] = {4'b0001, 4'b0010, 4'b0100, 4'b1000};
57 }
58
59 // TO DO : Coverpoint for tx_vc_req: All the VCs are requested atleast once. Ignore what is not allowed, or put it as illegal
60 tx_vc_req : coverpoint htax_tx_intf.tx_vc_req {
61     bins vc_req[] = {[1:7]}; // Legal VCs
62     illegal_bins illegal_request = {0};
63 }
64
65 // TO DO : Coverpoint for tx_vc_gnt: All the virtual channels are granted atleast once.
66 tx_vc_gnt : coverpoint htax_tx_intf.tx_vc_gnt {
67     bins vc_gnt[] = {[1:7]};
68 }
```

## htax\_rx\_monitor\_c.sv Code

```
1 ///////////////////////////////////////////////////////////////////
2 // Texas A&M University
3 // CSCE 616 Hardware Design Verification
4 // Created by : Prof. Quinn and Saumil Gogri
5 ///////////////////////////////////////////////////////////////////
6
7 class htax_rx_monitor_c extends uvm_monitor;
8
9     `uvm_component_utils(htax_rx_monitor_c)
10
11     //Analysis port to communicate with Scoreboard
12     uvm_analysis_port #(htax_rx_mon_packet_c) rx_collect_port;
13
14     virtual interface htax_rx_interface htax_rx_intf;
15     htax_rx_mon_packet_c rx_mon_packet;
16     int pkt_len;
17
18     // TO DO : Create covergroup for htax_rx_intf and add at least one coverpoint
19     covergroup cover_htax_rx_intf;
20         option.per_instance = 1;
21         option.name = "cover_htax_rx_intf";
22
23         // Coverpoint for rx_sot: Captures start of transmission signals
24         RX_SOT : coverpoint htax_rx_intf.rx_sot {
25             bins sot_active[] = {1'b1};
26         }
27
28         // Coverpoint for rx_data: Tracks data values received
29         RX_DATA : coverpoint htax_rx_intf.rx_data {
30             bins data_values[] = {[0:255]};
31         }
32         // Coverpoint for rx_eot: Captures end of transmission signals
33         RX_EOT : coverpoint htax_rx_intf.rx_eot {
34             bins eot_active[] = {1'b1}; // Capture active end signals
35         }
36     endgroup
37
38 endclass
```

## Simulation Output

terminal Sessions View X server Tools Games Settings Macros Help

Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect... 4 olympus.eco.tamu.edu

t 3

UVM INFO ../tb/htax\_scoreboard\_c.sv(146) @ 470990000: uvm\_test\_top.tb.htax\_sb [SCOREBOARD] Dropping pkt from queue 3

UVM INFO /opt/coe/cadence/XCELIUM/tools/methodology/UVM/CDMS-1.1d/sv/src/base/uvm\_objection.svh(1268) @ 520970000: reporter [TE

ST\_DONE] 'run' phase is ready to proceed to the 'extract' phase

UVM INFO ../tb/htax\_scoreboard\_c.sv(150) @ 520970000: uvm\_test\_top.tb.htax\_sb [SCOREBOARD] End of Simulation Checking

UVM INFO ../tb/htax\_scoreboard\_c.sv(152) @ 520970000: uvm\_test\_top.tb.htax\_sb [SCOREBOARD] Port 0 Queue is empty

UVM INFO ../tb/htax\_scoreboard\_c.sv(156) @ 520970000: uvm\_test\_top.tb.htax\_sb [SCOREBOARD] Port 1 Queue is empty

UVM INFO ../tb/htax\_scoreboard\_c.sv(160) @ 520970000: uvm\_test\_top.tb.htax\_sb [SCOREBOARD] Port 2 Queue is empty

UVM INFO ../tb/htax\_scoreboard\_c.sv(164) @ 520970000: uvm\_test\_top.tb.htax\_sb [SCOREBOARD] Port 3 Queue is empty

--- UVM Report catcher Summary ---

Number of demoted UVM\_FATAL reports : 0

Number of demoted UVM\_ERROR reports : 0

Number of demoted UVM\_WARNING reports : 0

Number of caught UVM\_FATAL reports : 0

Number of caught UVM\_ERROR reports : 0

Number of caught UVM\_WARNING reports : 0

--- UVM Report Summary ---

\*\* Report counts by severity

UVM\_INFO : 3017

UVM\_WARNING : 0

UVM\_ERROR : 0

UVM\_FATAL : 0

\*\* Report counts by id

[RINTST] 1

[SCOREBOARD] 2005

[TEST\_DONE] 1

[TOP] 5

[UVMTOP] 1

[htax\_tx\_driver\_c] 1000

[simple\_random\_seq] 3

[simple\_random\_test] 1

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## htax\_packet covergroup

The screenshot displays the Cadence IMC (Integrated Model Checker) interface. The top toolbar includes various analysis and refinement tools. The main window shows the 'Cover Groups' tab with a tree view of the design hierarchy. The 'htax\_packet' covergroup is selected, and its details are shown in the 'Details' pane. The 'Attributes' pane lists various attributes and their values.

Ex	UIN	Name	Overall Average Grade	Overall Covered	Enclosing Entity
		(no filter)	(no filter)	(no filter)	
		cover_htax_packet	100%	147 / 14...	uvm_pkg.uvm_test_top
		cover_htax_tx_intf	100%	10 / 10 (...)	uvm_pkg.uvm_test_top

  

Ex	UIN	Name	Overall Average Grade	Overall Covered
		(no filter)	(no filter)	(no filter)
		DEST_PORT	100%	4 / 4 (100%)
		VC	100%	3 / 3 (100%)
		LENGTH	100%	16 / 16 (100%)
		DEST_VC	100%	12 / 12 (100%)
		DEST_LENGTH	100%	64 / 64 (100%)
		VC_LENGTH	100%	48 / 48 (100%)

  

Col #	Name	Value
	(no filter)	(no filter)
	At Least	1
	Combined Average Grade	100%
	Combined Covered	147.0
	Combined Covered Grade	100%
	Combined Total	147.0
	Combined Total Weighted Coverage	6.0

## htax\_intf covergroup

The screenshot displays the Cadence IMC (Integrated Model Checker) interface. The top toolbar includes various analysis and refinement tools. The main window shows the 'Cover Groups' tab with a tree view of the design hierarchy. The 'htax\_intf' covergroup is selected, and its details are shown in the 'Details' pane. The 'Attributes' pane lists various attributes and their values.

Ex	UIN	Name	Overall Average Grade	Overall Covered	Enclosing Entity
		(no filter)	(no filter)	(no filter)	
		cover_htax_packet	100%	147 / 14...	uvm_pkg.uvm_test_top
		cover_htax_tx_intf	100%	10 / 10 (...)	uvm_pkg.uvm_test_top

  

Ex	UIN	Name	Overall Average Grade	Overall Covered
		(no filter)	(no filter)	(no filter)
		tx_output_req	100%	4 / 4 (100%)
		tx_vc_req	100%	3 / 3 (100%)
		tx_vc_gnt	100%	3 / 3 (100%)

  

Col #	Name	Value
	(no filter)	(no filter)
	At Least	1
	Combined Average Grade	100%
	Combined Covered	10.0
	Combined Covered Grade	100%
	Combined Total	10.0
	Combined Total Weighted Coverage	3.0