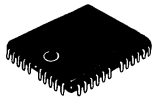
HA16642MP,HA16642NT ● Read/Write Functions for Floppy Disk Drive

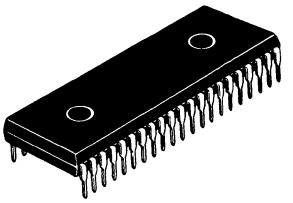
This IC can provide READ and WRITE functions in one chip for Floppy Disk Drive.

HA16642MP



(MP-44)

HA16642NT



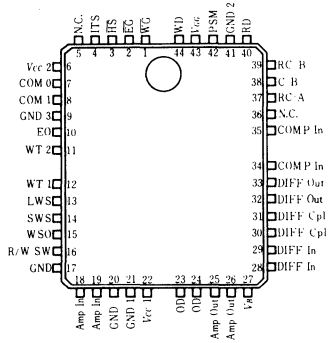
(DP-42S)

■ FEATURES

- Read Amplifier has a differential voltage gain of 200 typ., which is avairable to adjust by gain select terminal.
- READ Circuit can be applied for the signal amplitude of 0.5mVpp to 10mVpp which is read out from HEAD COIL, so that this IC has superior capability to apply for a FDD less than 5 inches.
- In the read circuit, the peak shift is less than 1% for the signal amplitude, 0.5mVpp to 10mVpp, at the Amp input.
- In the WRITE circuit, the COMMON DRIVER, the WRITE DRIVER, and the ERASE DRIVER can provide a large current capability, so that can be applied to various kinds of FDD's.
- Write current can be established at any value according to the external resistor. The write current is independent of the supply voltage drift and temperature drift, with the built-in stabilizing circuit.
- This IC provides a function to reduce the write current at the inner track on the disk with a external switching signal. The reduce ratio of the write current can be established at any value with the external resistor.
- The WRITE GATE signal and the ERASE GATE signal can be applied independently each other.
- A dual-mode supply voltage monitor circuit is built-in, to inhibit a miss writing and a miss erasing at the power supply timing, ON and OFF, and the abnormal supply voltage.
- READ and WRITE functions are integrated in one chip, resulting in broad reduction of external components.

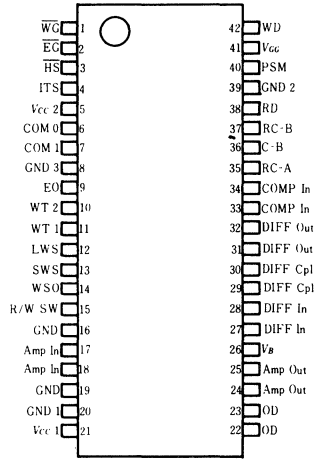
■ PIN ARRANGEMENT

● HA16642MP



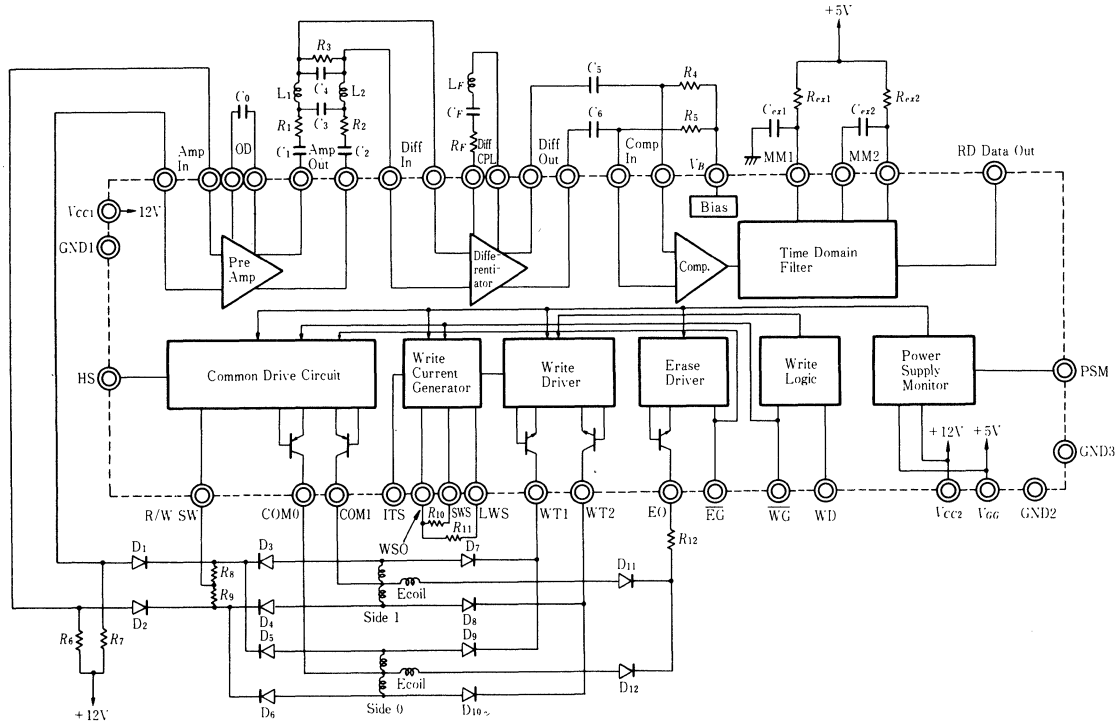
(Top View)

● HA16642NT



(Top View)

■BLOK DIAGRAM AND APPLICATION CIRCUIT



: Integrated Blocks

R_8, R_9 : To determine a bias current for read mode

R_{10} : To determine the increase ratio of a write current at the inner track.

R_{11} : To determine a write current at the outer track.

(Write current at the inner track is a summation of the currents determined by R_{10} and R_{11} respectively.)

■ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Item	Symbol	Ratings	Unit	Applicable Terminal
Supply Voltage	V_{CC1}	7.0	V	V_{CC1}
Supply Voltage	V_{CC2}	16.0	V	V_{CC2}
Input Voltage	V_{IN}	−0.2 to +7.0	V	AMP IN
Differential Input Voltage	$V_{IN(diff)}$	0 to +5.0	V	AMP IN
Output Voltage	V_{out}	−0.2 to +7.0	V	RD DATA OUT
Common Drive Current	I_{COM}	150	mA	COM 0, COM 1
Write Drive Current	I_{WT}	15	mA	WT 1, WT 2
Erase Drive Current	I_{ER}	120	mA	EO
Power Dissipation	P_T	800	mW	V_{CC1}, V_{CC2}, V_{GG}
Operating Temperature Range	T_{opr}	0 to +70	℃	
Storage Temperature Range	T_{stg}	−55 to +125	℃	

■ELECTRICAL CHARACTERISTICS (Ta=25℃)

Circuit Block	Item	Symbol	Test Condition		min	typ	max	Unit
	Supply Voltage Range	V_{GG}			4.5	5.0	5.5	V
		$V_{CC1,2}$			10.5	12.0	13.5	V
Pre Amp.	Differential Voltage Gain	A_{VD}	f=250kHz, V_{in}=5mVrms		—	200	—	V/V
	Input Bias Current	I_{IB}			—	—	15	μA
	Common Mode Input Voltage Range	V_{CM}			2.0	2.7	3.4	V
	Output Harmonic Distortion	THD	f=1kHz, V_{in}=10mVpp		—	—	5	%
Peak Detector	Peak Shift	PS	f=250kHz, V_{in}=0.5 to 10mVpp		—	—	2.5	%
Read Data Processor	Output Voltage	V_{OH}	V_{GG}=4.75V, I_{OH}=−400μA		2.7	—	—	V
		V_{OL}	V_{GG}=4.75V, I_{OL}=4mA		—	—	0.4	V
	Rising Time	t_{TLH}	V_{GG}=5V, V_{out}=0.4 to 2.7V		—	30	—	ns
	Falling Time	t_{THL}	V_{GG}=5V, V_{out}=2.7 to 0.4V		—	15	—	ns
	Timing Range #1	t_{1AB}	f=125 kHz		1.3	—	4	μs
			f=250 kHz		1.3	—	2	
	Timing Range #2	t_{2AB}	f=125 kHz		0.15	—	1.5	μs
			f=250 kHz		0.15	—	0.75	
Common Driver	Output Voltage at selected Write Mode	V_{WCMS}	V_{CC2}=12V, I_{COM}=120mA		—	11	—	V
	Output Voltage at unselected Write Mode	V_{WCMUS}	V_{CC2}=12V, at unselected		—	—	0.7	V
	Output Voltage at selected Read Mode	V_{RCMS}	V_{CC2}=12V, I_{COM}=1mA		—	2.7	—	V
	Output Voltage at unselected Read Mode	V_{RCMUS}	V_{CC2}=12V, at unselected		—	—	0.75	V
	Output Current Range	I_{COM}			—	—	150	mA
Erase Driver	Output Low Voltage	V_{OLE}	V_{GG}=5V, I_{OL}=100mA		—	—	0.5	V
	Output Leak Current	I_{OHE}	V_{OH}=12V, V_{GG}=5V		—	—	100	μA
	Erase Current Range	I_{ER}			—	—	120	mA
Write Driver	Write Current Accuracy	A_{CIW}	V_{GG}=5V, V_{CC2}=12V		−7	—	+7	%
	Write Current-Supply Voltage Sensitivity	P_{SIW}	V_{GG}=5V, V_{CC2}=10.8 to 13.2V		—	±1.5	—	%/V
	Write Current-Temperature Coefficient	T_{CIW}	V_{GG}=5V, V_{CC2}=12V, Ta=0 to+70℃		—	±0.05	—	%/℃
	Write Current Symmetry	$\triangle I_{WT}$	V_{GG}=5V, V_{CC2}=12V, $I_{WT1}-I_{WT2}$		−1	—	+1	%
	Write Current Range	I_{WT}	V_{GG}=5V, V_{CC2}=12V		1	—	10	mA
	Leak Current at Off Driver	I_{ohwt}	V_{GG}=5V, V_{CC2}=12V, V_{WT}=20V		—	—	50	μA
Supply Voltage Monitor	Detection Voltage for 5V Supply	V_{MON1}	V_{CC2}=12V		3.5	3.9	4.3	V
	Detection Voltage for 12V Supply	V_{MON2}	V_{GG}=5V		8.0	9.0	9.8	V
Logic Input Gate	Input High Voltage	V_{IH}	V_{GG}=5V		2.0	—	—	V
	Input Low Voltage	V_{IL}	$\overline{WG}$, $\overline{EG}$		—	—	0.8	V
Schmitt Type Logic Input Gate	Input High Voltage	V_{IHS}	V_{GG}=5V		2.0	—	—	V
	Input Low Voltage	V_{ILS}	HS, WD		—	—	0.5	V
Dissipation Current	12V Supply	I_{CC}	V_{CC}=13.5V	Read	—	25	40	mA
				Write	—	16	—	
	5V Supply	I_{GG}	V_{GG}=5.5V	Read	—	36	60	mA
				Write	—	33	—	

■ PIN DESCRIPTION

Symbol	Name	Description
AMP IN	Pre Amp Input	Terminal for differential input of pre amplifier in read circuit. A signal voltage picked up through R/W coil is applied.
OD	Gain Select	Terminal for DC offset compensation of pre amp, and for gain selection. The amp gain is available to be changed by connecting a resistor to the compensation capacitor in series.
AMP OUT	Pre Amp Output	Terminal for differential output of the pre amp in read circuit. A low pass filter is connected between the input terminal of differentiator and this terminal.
DIFF IN	Differentiator Input	Input terminal of differentiator in read circuit. Output voltage from the pre amp is applied to this terminal through the low pass filter.
DIFF CPL	Differential Coupling	Terminal for connecting a capacitor for differentiation. R_F, C_F and L_F are connected in series, as shown in the block diagram.
DIFF OUT	Differentiator Output	Output terminal of the differentiator. The differentiated signal is appeared on this terminal with the phase shifted by 90°. The output is coupled through the capacitor and is applied to the comparator input.
COMP IN	Comparator Input	Input terminal of the comparator in read circuit. A signal with the phase shifted by 90° through the differentiator is applied, and the zero-crossing point is detected. This terminal is pulled up to the bias source by the external resistor.
MM1	Mono Multi 1	A capacitor and a resistor are connected to these terminals. The capacitance and the resistance determine the output pulse width of the Pre Mono Multi Vibrator in the Time Domain Filter Circuit.
MM2	Mono Multi 2	A capacitor and a resistor are connected these terminals. The capacitance and the resistance determine the output pulse width of the Post Mono Multi Vibrator in the Time Domain Filter Circuit.
RD DATA OUT	READ Output	Output terminal of the read circuit. A pulse which is synchronized to the peak position of the read out signal from head coil is obtained. The output pulse width is determined by the external capacitor and resistor of MM 2. The signal output level is TTL compatible.
COM 0	Common Driver 0	Output terminal of Common Driver (SIDE 0). During the Head Select signal is selecting SIDE 0, a common voltage is appeared on this terminal. The voltage value at Write Mode and that at Read Mode are shown in the Electrical Characteristics. A current which equals to Write Current + Erase Current flows out from this terminal. When the SIDE 0 is unselected, a common voltage is not appeared, and this terminal is pulled down to ground by a high resistance in the IC.
COM 1	Common Driver 1	Output terminal of Common Driver (SIDE 1). The function is as same as that of COM 0.
$\overline{HS}$	Head Select	Input terminal for Head Select signal. This signal selects the SIDE 0 or SIDE 1 of the common driver. This terminal is consisted of Schmitt type input circuits. Input Low selects COM 1.
R/W SW	R/W Switch	A transistor output for switching the bias state in head coil and in diode SW circuit, according to READ/WRITE switching. This terminal is pulled down to ground level in READ Mode, and it is pulled up to 12V in WRITE Mode.
WSO	WRITE Regulated Voltage Output	Output from regulated supply source in Write Current Setting Circuit.
LWS	Low Current Set	Terminal to set a low level write current. The current is determined by connecting an external resistor $\bar{R}_{11}$ between terminal WSO and this terminal.
SWS	Difference Current Set	Terminal to set the current difference (I_{WDF}) between high level write current and low level write current. The difference current is determined by connecting an external resistor R_{10} between terminal WHO and this terminal. I_{WDF} = (High Level Write Current − Low Level Write Current) $I_{WH} = I_{WL} + I_{WDF}$ Where; I_{WH} is high level write current, and I_{WL} is low level write current. I_{WH}-to-I_{WL} current ratio is; $I_{WH}/I_{WL} = 1 + I_{WDF}/I_{WL}$ It can be set at any value by R_{10} and R_{11}.
ITS	Current Switch Signal Input	Input terminal for Write Current SW signal at inner & outer tracks. High Level Write Current is selected at input Low, and Low Level Write Current at input High.
WD	Write Data Input	Write Data Input Terminal. The signal is devided through the F/F circuit in the IC, and drives the Write Driver.

(to be continued)

Symbol	Name	Description
WT 1, 2	Write Driver 1, 2	Output terminal of Write Driver. The current determined by external resistors at terminal SWS and terminal MWS is sinked. WT 1 and WT 2 turns on alternately, according to the Write Data "1" or "0".
$\overline{WG}$	Write Gate	Input terminal for Write Gate signal. The write gate is enable at input Low, and allows data writing.
$\overline{EG}$	Erase Gate	Input terminal for Erase Gate signal. The erase gate is enable at input Low, and allows erasing.
EO	Erase Driver	Output terminal of Erase Driver. It turns on at erase gate input LOW. The output on this terminal is an open collector output of NPN transistor, and the erase current is determined by external resistor R_{12}.
PSM	Power Supply Monitor	The monitor circuit monitors the V_{GG} (+5V) and V_{CC2} (+12V), and will inhibit the common driver, the write driver and the erase driver when the supply voltage becomes abnormally low, and the FLAG signal will appear on this terminal PSM. The Driver Inhibit is released only when both V_{GG} and V_{CC2} are more that the specified voltages, regardless of the supply sequence.
V_{CC1}	Amp Voltage	Voltage for Pre Amp in read circuit.
V_{CC2}	Voltage for 12V	Another Voltage (Excepting for Pre Amp.)
V_{GG}	Voltage for 5V	
GND 1	Amp GND	GND for Pre Amp read circuit.
GND 2		GND for read circuit. (Excepting for Pre Amp.)
GND 3		GND for write circuit.