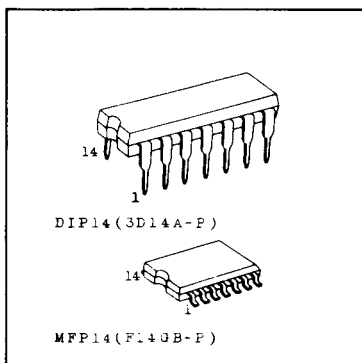
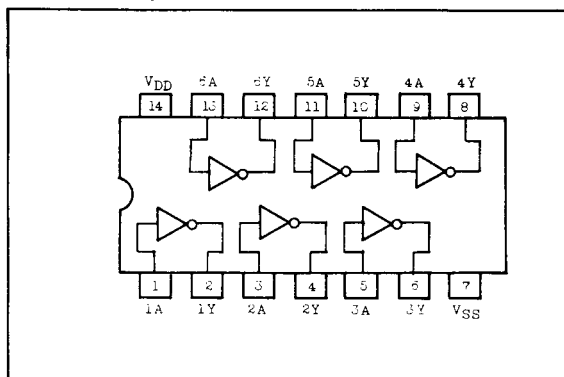


C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC40H004P/F

TC40H004 HEX INVERTER

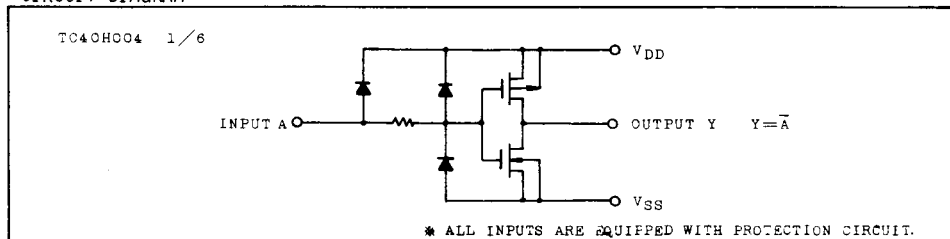
PIN CONNECTION



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+10$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	300 (DIP) / 180 (MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$
Lead Temp./Time	T_{sol}	$260^{\circ}\text{C} \cdot 10 \text{ sec}$	

CIRCUIT DIAGRAM

RECOMMENDED OPERATING CONDITIONS ($V_{SS}=0.0\text{V}$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	-	2.0	-	8.0	V
Input Voltage	V_{IN}	-	0	-	V_{DD}	V
Operating Temperature	T_{opr}	-	-40	-	85	$^{\circ}\text{C}$

TC40H004P/F

ELECTRICAL CHARACTERISTICS ($V_{SS}=0.0V$)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$ I_{OUT} < 1\mu A$ $V_{IN}=V_{SS}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$ I_{OUT} < 1\mu A$ $V_{IN}=V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	
High Level Output Current		I_{OH}	$V_{OH}=4.6V$ $V_{IN}=V_{SS}$	5	-0.52	-	-0.44	-	-	-0.36	-	mA
Low Level Output Current		I_{OL}	$V_{OL}=0.4V$ $V_{IN}=V_{DD}$	5	1.4	-	1.1	-	-	0.8	-	
Input Voltage	High Level	V_{IH}	$ I_{OUT} < 1\mu A$ $V_{OUT}=0.5V$	5	4.0	-	4.0	-	-	4.0	-	V
	Low Level	V_{IL}	$V_{OUT}=4.5V$ $V_{IN}=V_{SS}, V_{DD}$	5	-	1.0	-	-	1.0	-	1.0	
Input Current	"H" Level	I_{IH}	$V_{IH}=8.0V$	8	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IL}	$V_{IL}=0.0V$	8	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Supply Current		I_{DD}	$*V_{IN}=V_{SS}, V_{DD}$	5	-	2.0	-	10^{-3}	2.0	-	10.0	μA

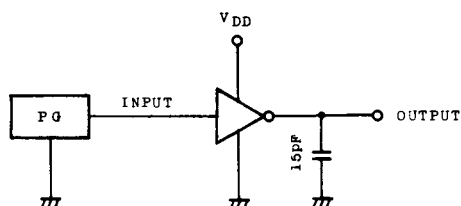
* All valid input combinations.

SWITCHING CHARACTERISTICS ($T_a=25^\circ C$, $V_{SS}=0.0V$, $C_L=15pF$)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}	Circuit 1	5	-	14	30	ns
Output Fall Time		t_{of}	Circuit 1	5	-	11	30	
Propagation Delay Time	(Low-High)	t_{pLH}	Circuit 1	5	-	15	20	ns
	(High-Low)	t_{pHL}		5	-	13	20	
Input Capacitance		C_{IN}			-	5		pF

SWITCHING TIME TEST CIRCUIT

CIRCUIT 1.



$t_r = t_f = 10\text{ns}$

Timing diagram for a 74VHC04 inverter. The diagram shows the input and output waveforms. The input signal is a square wave with a rise time (t_r) and fall time (t_f) of 10ns. The output signal is an inverted square wave with a propagation delay (t_{pHL} and t_{pLH}) and a rise/fall time (t_{or} and t_{of}). The input signal levels are V_{DD} and 0, and the output signal levels are V_{OH} and V_{OL} . The input signal has 10%, 50%, and 90% level markers. The output signal has 10%, 50%, and 90% level markers. The propagation delay is measured from the 50% input level to the 50% output level. The rise and fall times are measured from the 10% to 90% levels.

