EE5311 Tutorial_3 Report

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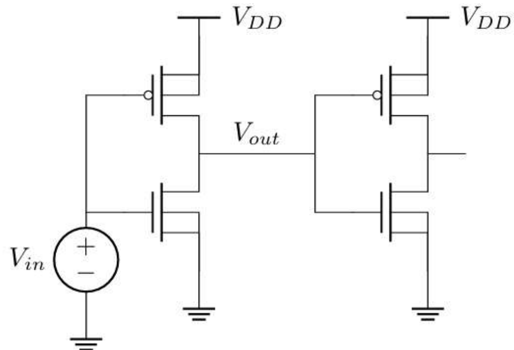
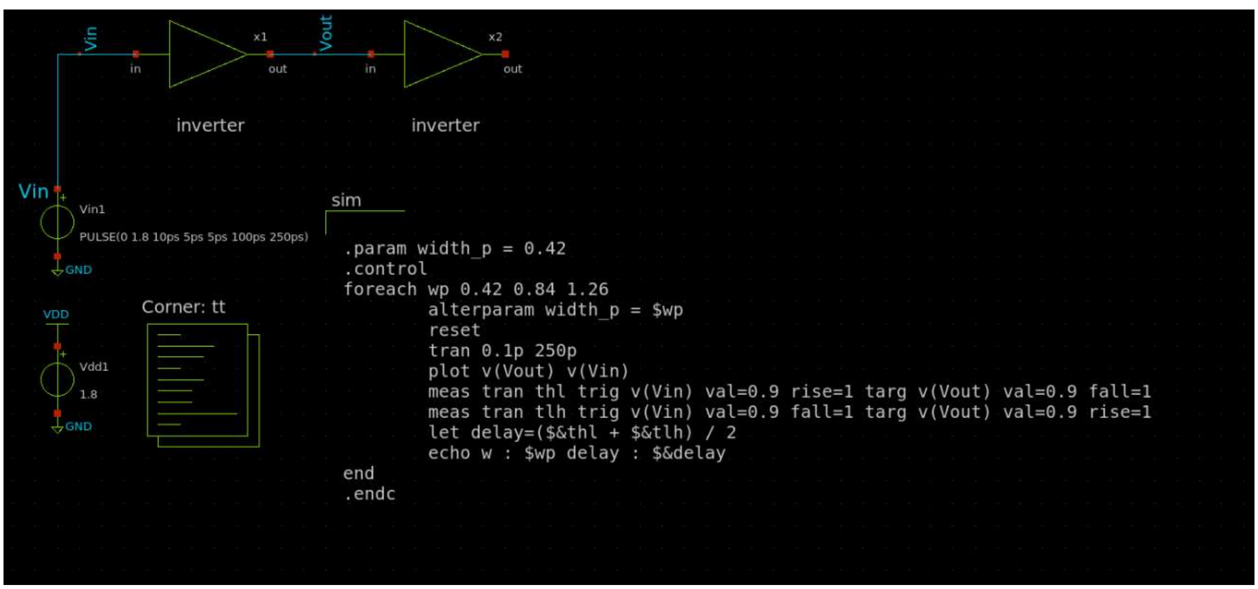
Consider the static CMOS inverter shown below. It drives another identical inverter. The input V_{in} is a pulse between 0 and V_{DD}, with a rise and fall time equal to 5 ps and a pulse width of 250 ps. The output is V_{out}.



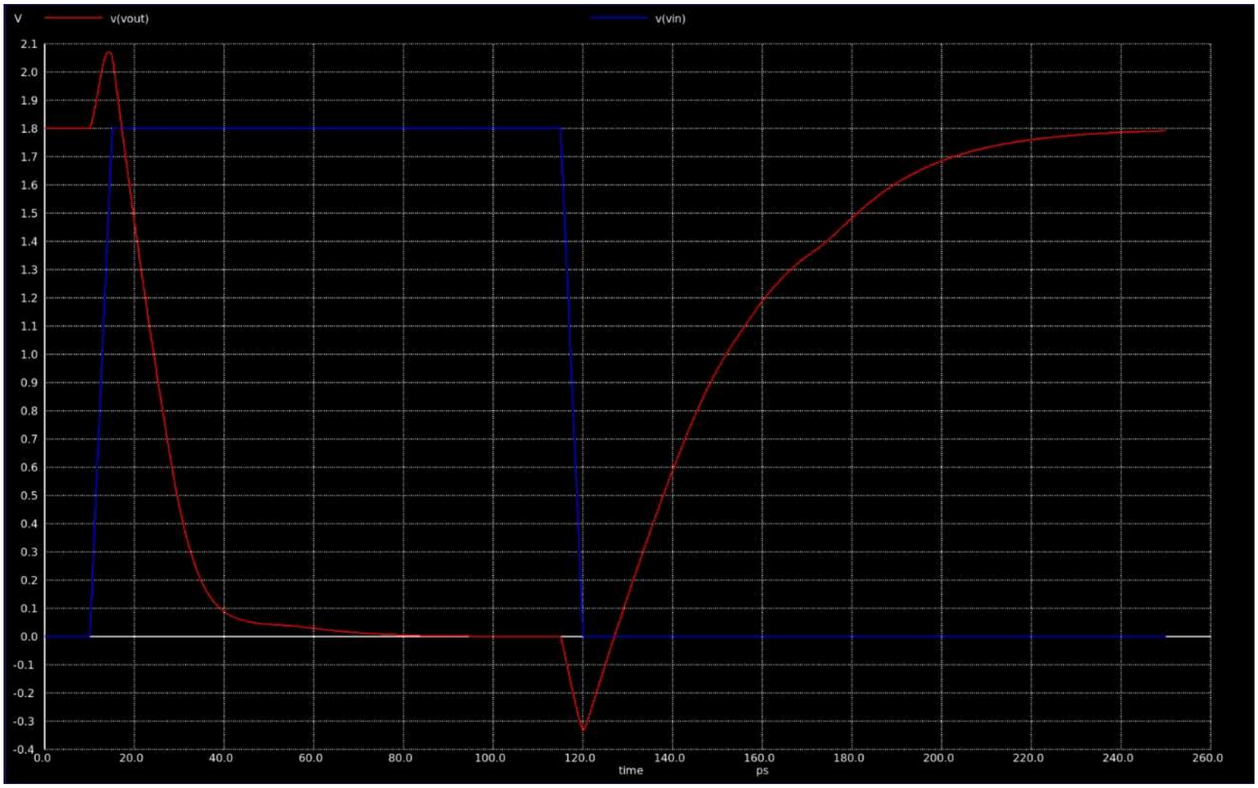
(a) Set $V_{DD} = 1.8V$. Assume that $L_n = L_p = 0.15\,\mu m$ and $W_n = 0.42\,\mu m$. Obtain the delay for $W_p = 0.42\,\mu m, 0.84\,\mu m, 1.26\,\mu m$.



w=0.42um	w=0.84um	w=1.26um
2.18e-11 s	1.99e-11 s	2.11e-11 s

Optimal width for less delay is 0.84 um

Width = 0.42um

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Circuit: ** sch_path: /home/ee22b074/ee5311/tutorial_3/parta.sch

Reset re-loads circuit ** sch_path: /home/ee22b074/ee5311/tutorial_3/parta.sch

Circuit: ** sch_path: /home/ee22b074/ee5311/tutorial_3/parta.sch

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

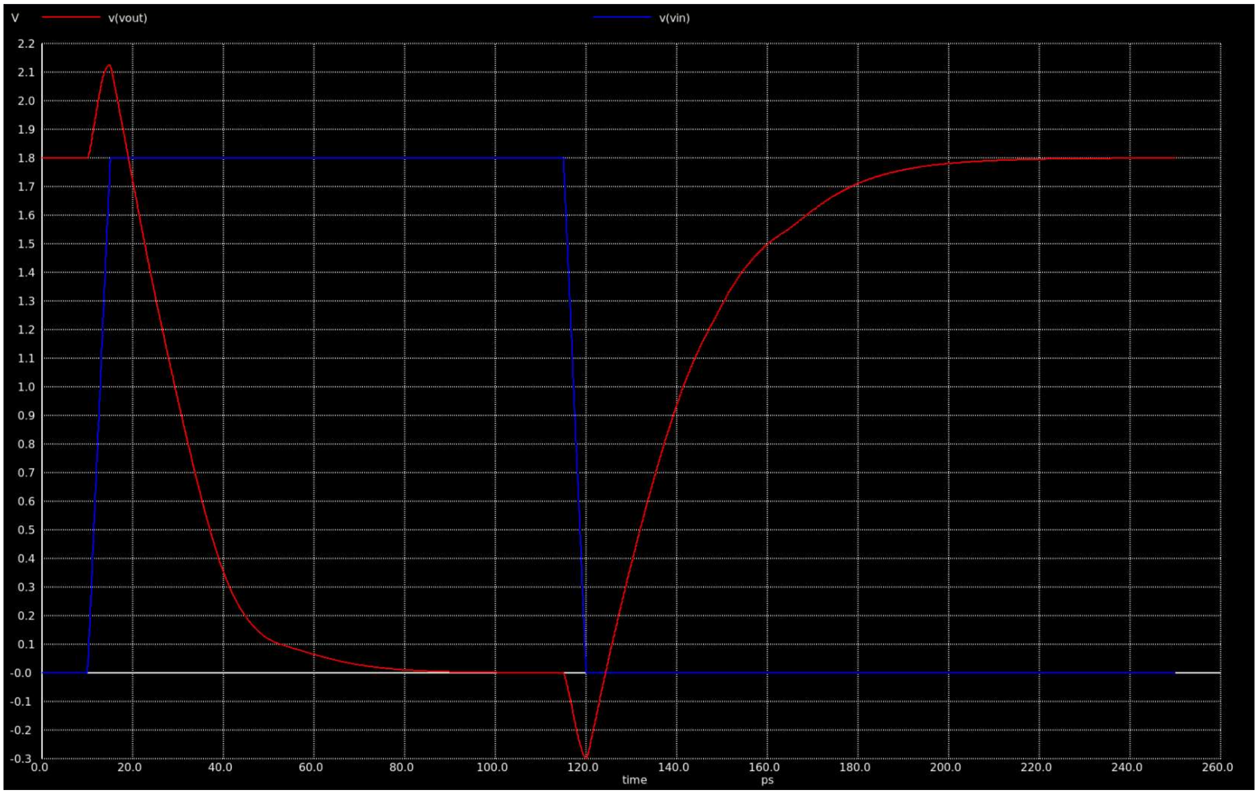
Using SPARSE 1.3 as Direct Linear Solver

Initial Transient Solution
--------------------------

Node                                    Voltage
----                                    -------
vdd                                         1.8
vin                                           0
vout                                        1.8
net1                                4.53092e-08
vin1#branch                                   0
vdd1#branch                        -1.81498e-11

 Reference value :  0.00000e+00
No. of Data Rows : 2520
thl                  =  1.277011e-11 targ=  2.527011e-11 trig=  1.250000e-11
tlh                  =  3.088289e-11 targ=  1.483829e-10 trig=  1.175000e-10
w : 0.42 delay : 2.18265E-11
ngspice 7 ->
```

Width = 0.84um




```
Circuit: ** sch_path: /home/ee22b074/ee5311/tutorial_3/parta.sch

Reset re-loads circuit ** sch_path: /home/ee22b074/ee5311/tutorial_3/parta.sch

Circuit: ** sch_path: /home/ee22b074/ee5311/tutorial_3/parta.sch

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

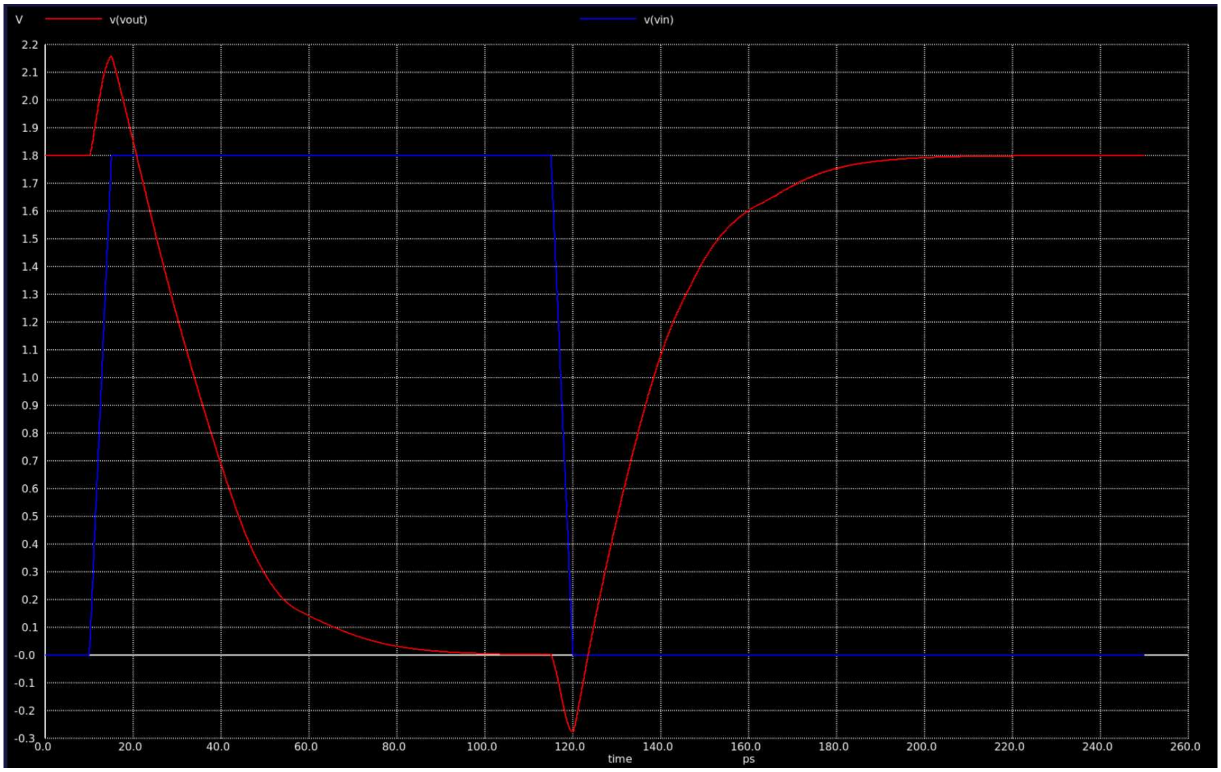
Using SPARSE 1.3 as Direct Linear Solver

Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
vdd                                        1.8
vin                                          0
vout                                       1.8
net1                               6.71229e-07
vin1#branch                                  0
vdd1#branch                       -2.43518e-10

 Reference value :  0.00000e+00
No. of Data Rows : 2520
thl                 =  1.822964e-11 targ=  3.072964e-11 trig=  1.250000e-11
tlh                 =  2.167976e-11 targ=  1.391798e-10 trig=  1.175000e-10
w : 0.84 delay : 1.99547E-11
ngspice 7 -> █
```

Width = 1.26um

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Note: No compatibility mode selected!

Circuit: ** sch_path: /home/ee22b074/ee5311/tutorial_3/parta.sch

Reset re-loads circuit ** sch_path: /home/ee22b074/ee5311/tutorial_3/parta.sch

Circuit: ** sch_path: /home/ee22b074/ee5311/tutorial_3/parta.sch

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver

Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
vdd                                        1.8
vin                                          0
vout                                       1.8
net1                               9.60947e-07
vin1#branch                                  0
vdd1#branch                       -3.47833e-10

 Reference value :  0.00000e+00
No. of Data Rows : 2520
thl                 =  2.327333e-11 targ=  3.577333e-11 trig=  1.250000e-11
tlh                 =  1.896577e-11 targ=  1.364658e-10 trig=  1.175000e-10
w : 1.26 delay : 2.11195E-11
ngspice 7 ->
```
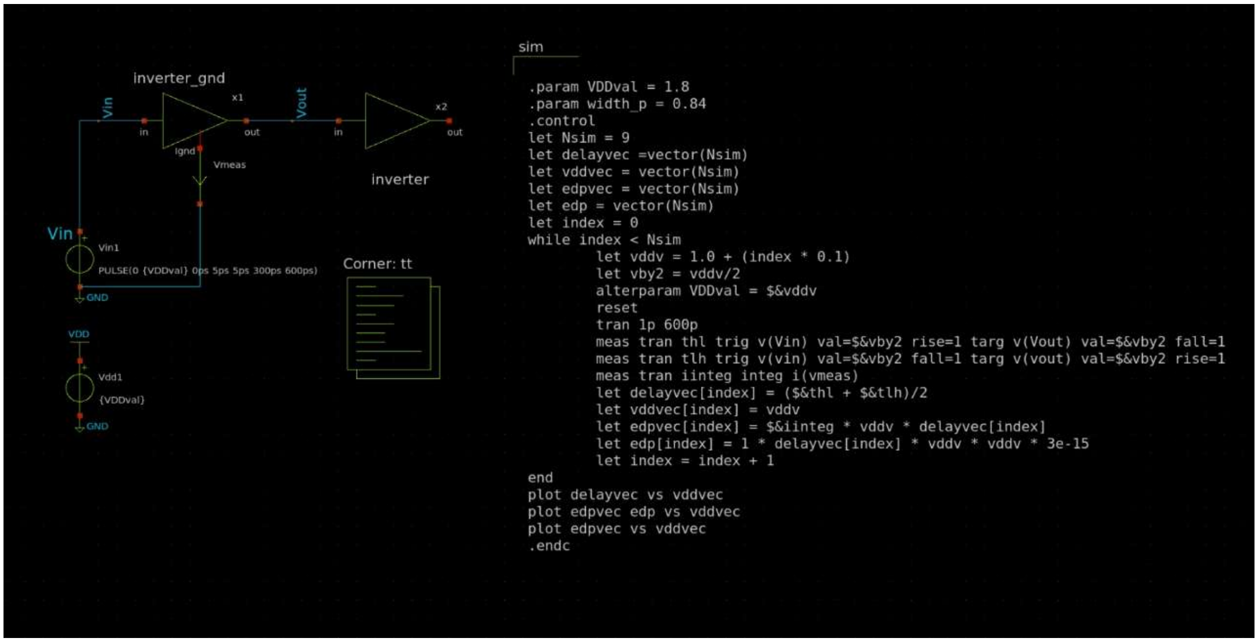
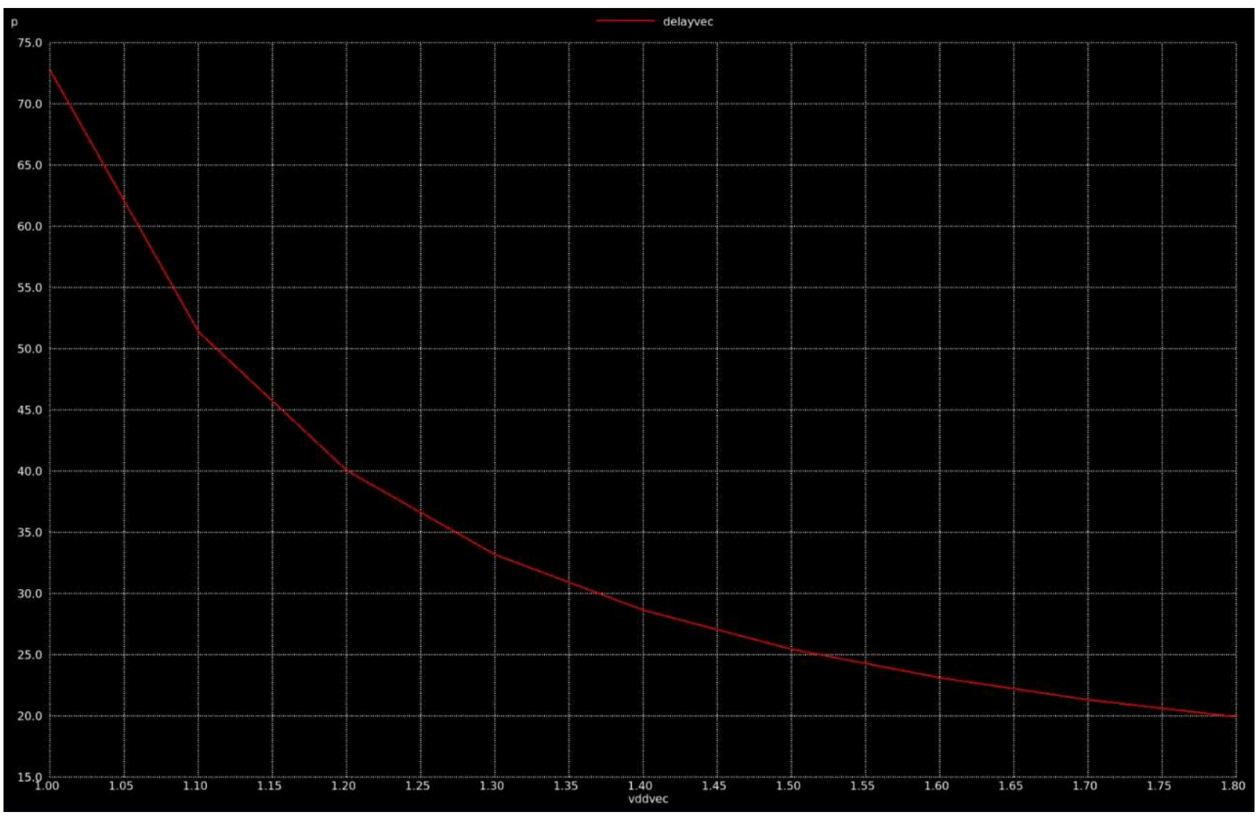

(b) Set W_p so that delay is minimised. Plot the delay as a function of V_{DD} for $V_{DD} = 1\text{V}$ to 1.8V in steps of 0.1V. How does it compare with analytical estimates?





Delay vs vdd graph

$$C_{total} = (C_{oxn}L_n + C_{jn}L_{diff} + C_{jswn} + 2C_{gdo})W_n + 2L_{diff}C_{jswn} +$$
$$(C_{oxp}L_p + C_{jp}L_{diff} + C_{jswp} + 2C_{gdo})W_p + C_{jswp}(2L_{diff})$$
$$\simeq aW_n + aW_p + b$$

$$t_{pLH} = \frac{aW_n + aW_p + b}{\underbrace{dW_p}} = \frac{a}{d}\left(\frac{W_n}{W_p}\right) + \frac{b}{d}\left(\frac{1}{W_p}\right) + \frac{a}{d}$$

pmos current : some constant $\times W_p$

$$t_{pHL} = \frac{aW_n + aW_p + b}{eW_n} = \frac{a}{e}\left(\frac{W_p}{W_n}\right) + \frac{b}{e}\left(\frac{1}{W_n}\right) + \frac{a}{e}$$

$t_p = \frac{t_{pHL} + t_{pLH}}{2}$, optimize t_p wrt W_p

$$\frac{\partial t_p}{W_p} = 0 \Rightarrow \frac{\partial}{\partial W_p}\left(\frac{a}{d}\frac{W_n}{W_p} + \frac{b}{d}\cdot\frac{1}{W_p} + \frac{a}{e}\frac{W_p}{W_n}\right) = 0 \Rightarrow -\frac{a}{d}\frac{W_n}{W_p^2} - \frac{b}{d}\frac{1}{W_p^2} + \frac{a}{e}\frac{1}{W_n} = 0$$

$$\Rightarrow -aeW_n^2 - beW_n + adW_p^2 = 0 \Rightarrow \boxed{W_p = \sqrt{\frac{aeW_n^2 + beW_n}{ad}}}$$

$$\frac{e}{d} \rightarrow \frac{\dfrac{K_n/L_n \cdot E_{cn}L_n(V_{DD}-V_{Tn})^2}{E_{cn}L_n + V_{DD} - V_{Tn}}}{\dfrac{K_p/L_p \; E_{cp}L_p + (V_{DD} - |V_{Tp}|)^2}{E_{cp}L_p + V_{DD} - |V_{Tp}|)}} \approx \frac{K_n}{K_p}$$

$$W_p \approx \sqrt{\frac{K_n}{K_p}}\, W_n$$ → width optimizes propagation delay

$$W_p = \sqrt{\frac{\mu_n C_{oxn}}{\mu_p C_{oxp}}}\, W_n = \sqrt{\frac{25 \times 834}{9 \times 816}}\, W_p = \sqrt{2.83} \times 0.42$$
$$= 1.68 \times 0.42$$
$$\simeq 0.70 \quad \approx 0.84 \mu m$$

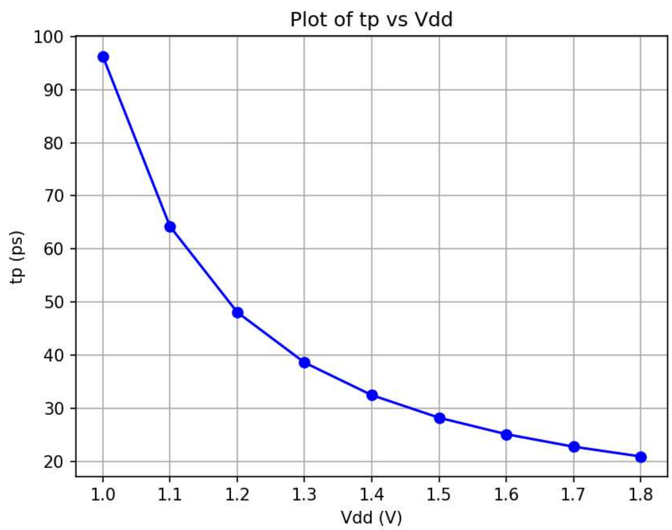
Analytical Expectation:

From delay models, the propagation delay τp of a CMOS inverter is approximately given by:

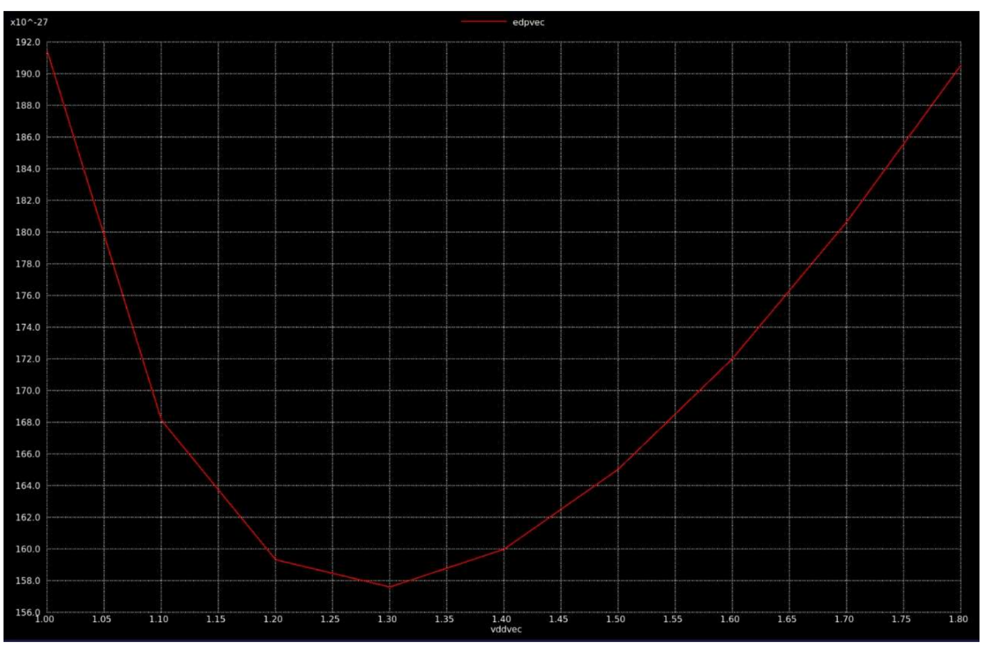
τp=k*VDD/(VDD−VT)^2

For sufficiently large VDDV, the dominant term simplifies to:
τp≈1/VDD

Thus, we expect **delay to decrease as VDD increases**, following an inverse relationship.



(c) Plot the measured and estimated energy-delay product as a function of V_{DD}. What is the optimum V_{DD}?



Energy delay product (EDP)

$$EDP = PDP \times t_p = \frac{1}{2} C V_{DD}^2 \cdot t_p \qquad C = C_{total}$$

How does this vary with V_{DD}?

For simplicity, $t_{pLH} = t_{pHL}$ (assumption)

$$t_p \propto \frac{V_{DD}(E_C L + V_{DD} - V_T)}{(V_{DD} - V_T)^2}$$

$$EDP \propto \frac{V_{DD}^3(E_C L + V_{DD} - V_T)}{(V_{DD} - V_T)^2} = D.$$

$$\frac{\partial EDP}{\partial V_{DD}} = 0 \Rightarrow V_{DD_{min}} = \frac{5V_T - E_C L}{4} + \frac{\sqrt{(5V_T - E_C L)^2 + 24V_T(E_C L - V_T)}}{4}$$

$$\approx 1.4V$$

Blue line in estimated and redone is measured values of energy delay products