EE5311 Tutorial_5 Report

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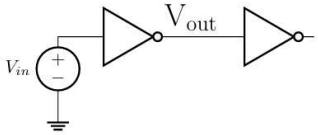
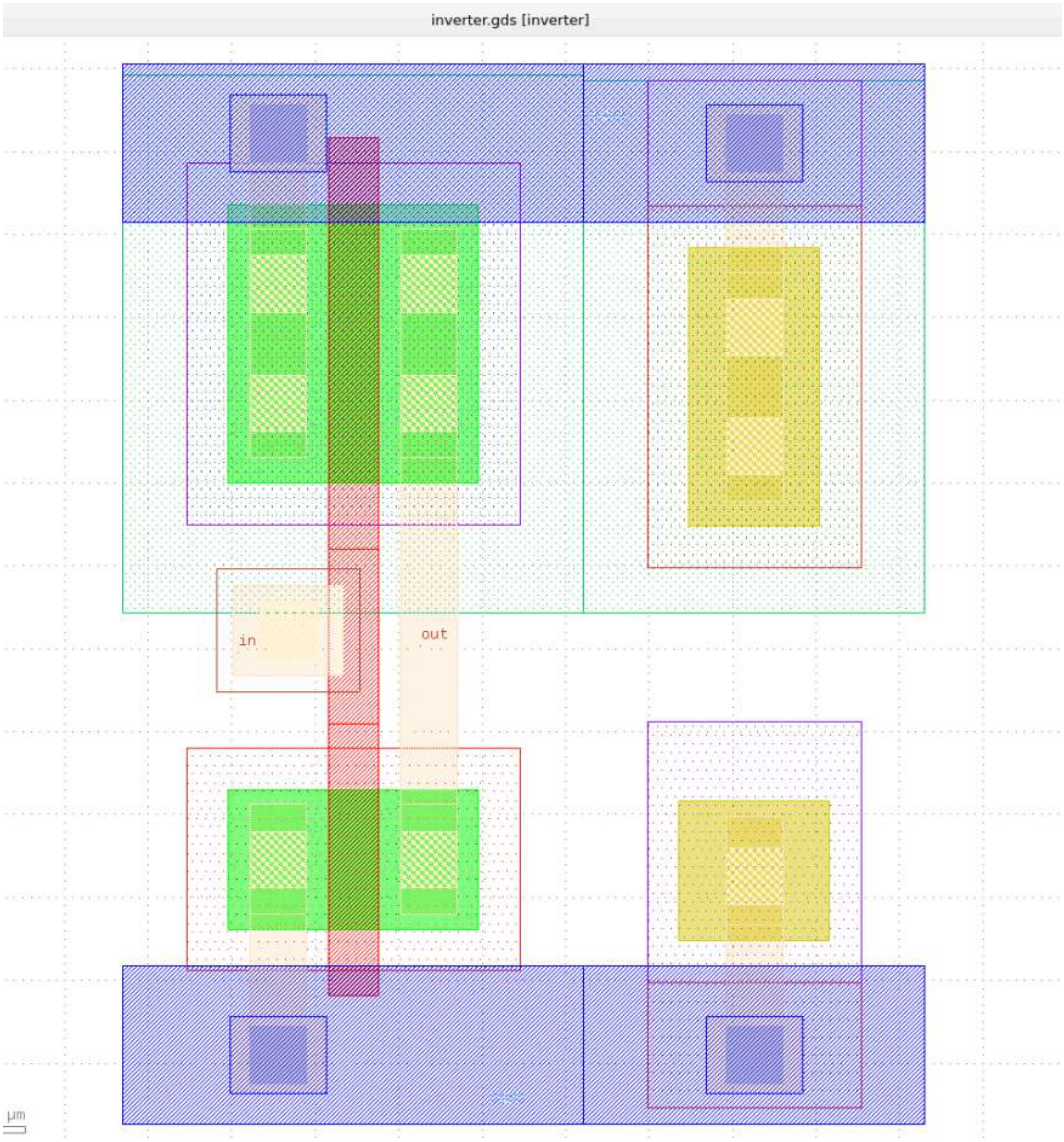
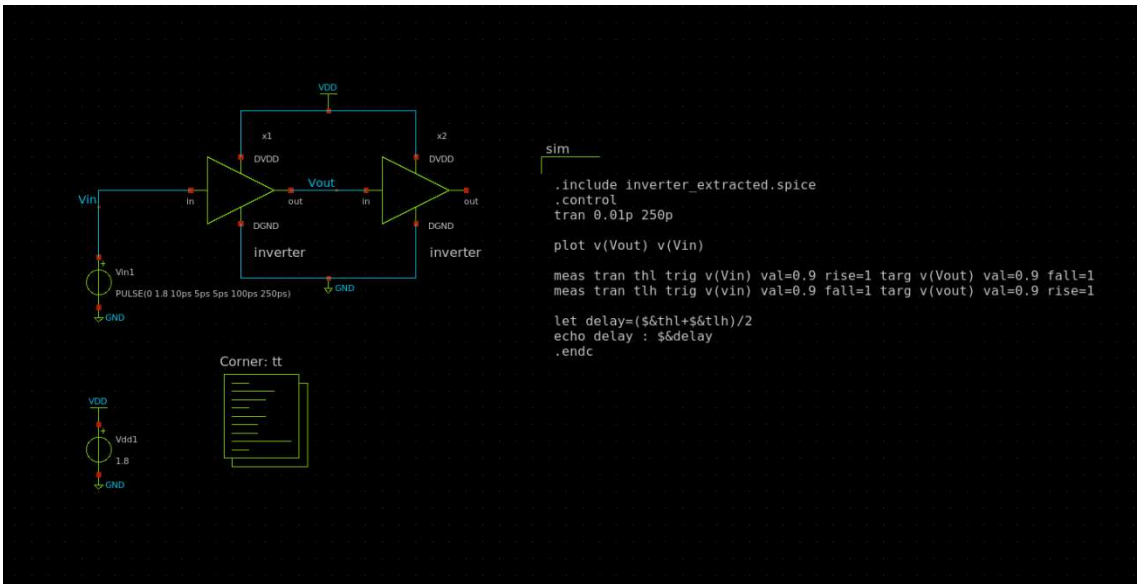
1. Draw a DRC and LVS clean layout of the CMOS inverter with the minimum delay from Assignment 3.
   (a) Extract the parasitic values from the layout and find the delay of the inverter using the circuit:



   (b) Measure the delay including the layout parasitic of net V_{out}.

Layout of CMOS inverter





Delay before the parasitic capacitances = 2.07e-11

```
Initial Transient Solution
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Node                                   Voltage
----                                   -------
vout                                       1.8
vin                                          0
vdd                                        1.8
net1                                 3.1174e-07
vdd1#branch                         -3.21945e-10
vin1#branch                                  0

 Reference value :  2.36045e-10
No. of Data Rows : 25020
thl                =  1.189162e-11 targ=  2.439162e-11 trig=  1.250000e-11
tlh                =  2.962604e-11 targ=  1.471260e-10 trig=  1.175000e-10
delay : 2.07588E-11
ngspice 7 -> 
```

Parasitic values of the given cmos from the extracted file

R0 in.n0 in.t0 249.532
R1 in.n0 in.t1 193.299
R2 in in.n0 158.875
R3 DVDD DVDD.t0 949.322
R4 DVDD DVDD.t1 398.459
R5 out out.t1 408.697
R6 out out.t0 280.94
R7 DGND DGND.t0 4634
R8 DGND DGND.t1 278.224
C0 out DVDD 0.102731f
C1 in DVDD 0.106389f
C2 out in 0.039402f
C3 out DGND 0.124072f
C4 in DGND 0.227955f
C5 DVDD DGND 0.773996f

Delay after the parasitic capacitances = 2.49e-11

```
Circuit: ** sch_path: /home/ee22b074/ee5311/tutorial_5/tb.sch

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver

Initial Transient Solution
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Node                                   Voltage
----                                   -------
x1.out.t1                                  1.8
x1.in.t0                                     0
x1.dvdd.t1                                 1.8
x1.dvdd.t0                                 1.8
x1.out.t0                                  1.8
x1.in.t1                                     0
x1.dgnd.t1                          9.78908e-12
x1.dgnd.t0                          8.34439e-09
x1.in.n0                                     0
vin                                          0
vdd                                        1.8
vout                                       1.8
x2.out.t1                           7.9196e-07
x2.in.t0                                   1.8
x2.dvdd.t1                                 1.8
x2.dvdd.t0                                 1.8
x2.out.t0                           6.25287e-07
x2.in.t1                                   1.8
x2.dgnd.t1                          6.72417e-08
x2.dgnd.t0                          3.27277e-15
x2.in.n0                                   1.8
net1                                6.93185e-07
vdd1#branch                        -2.43518e-10
vin1#branch                                  0

 Reference value :  2.19235e-10
No. of Data Rows : 25020
thl                =  2.254870e-11 targ=  3.504870e-11 trig=  1.250000e-11
tlh                =  2.742707e-11 targ=  1.449271e-10 trig=  1.175000e-10
delay : 2.49879E-11
ngspice 7 -> 
```
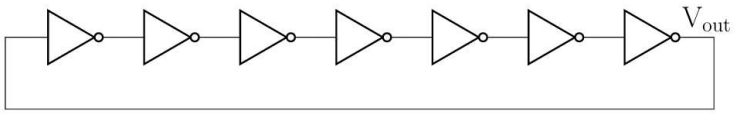

2. Using the inverter layout above, draw the layout of a seven stage ring oscillator shown below.



To ensure oscillation in the transient simulation, set the node $V_{out} = 0$V initially using: `.ic v(Vout)=0`

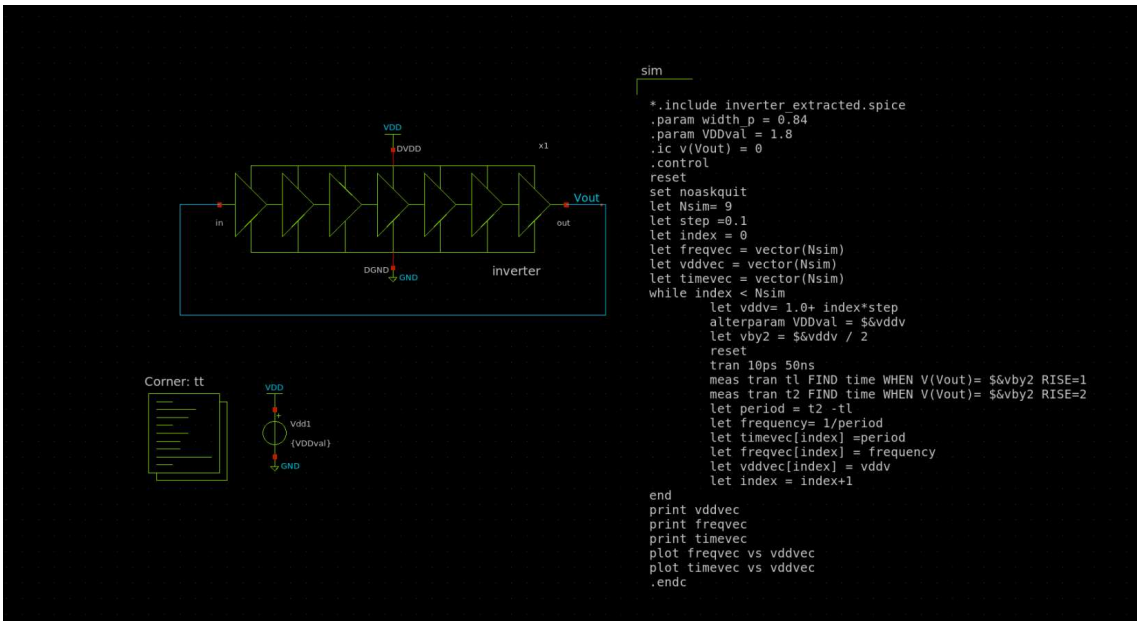
(a) Measure the oscillating frequency for $V_{DD} = 1.8$V with the layout parasitics.

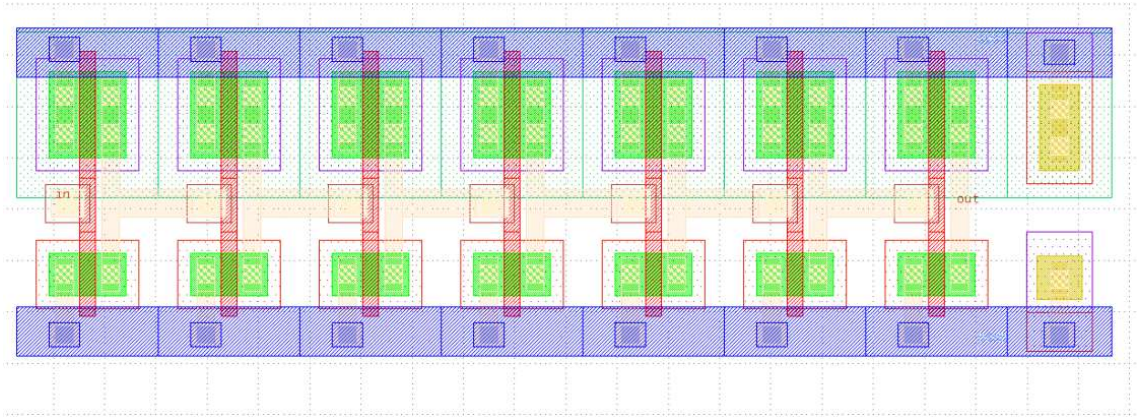
(b) Plot the oscillating frequency and time period as a function of V_{DD} for $V_{DD} = 1$V to 1.8V in steps of 0.1V.

(c) Compare the frequencies against pre-layout simulation in Assignment 4.

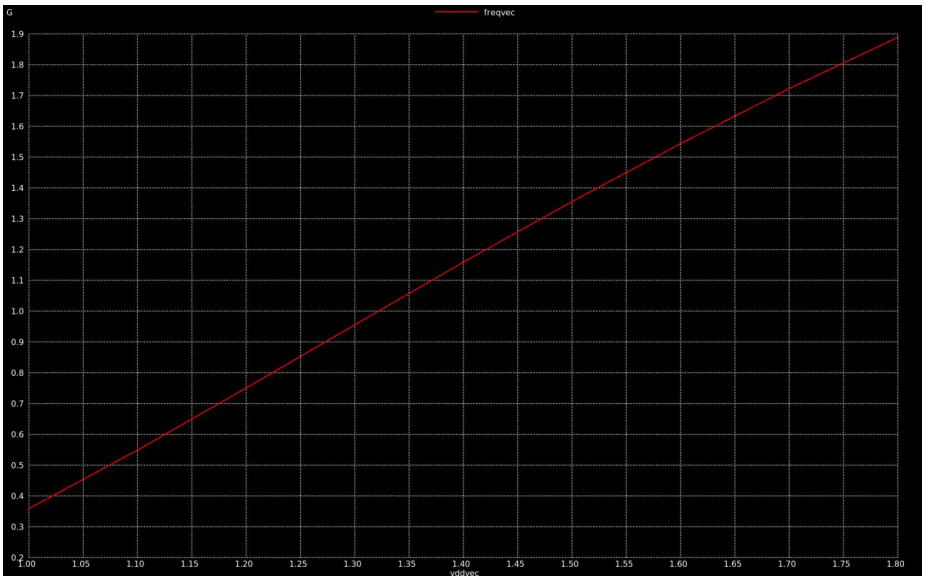
oscillating frequency for Vdd=1.8 with the layout parasitics

Frequency = 3.59e+08

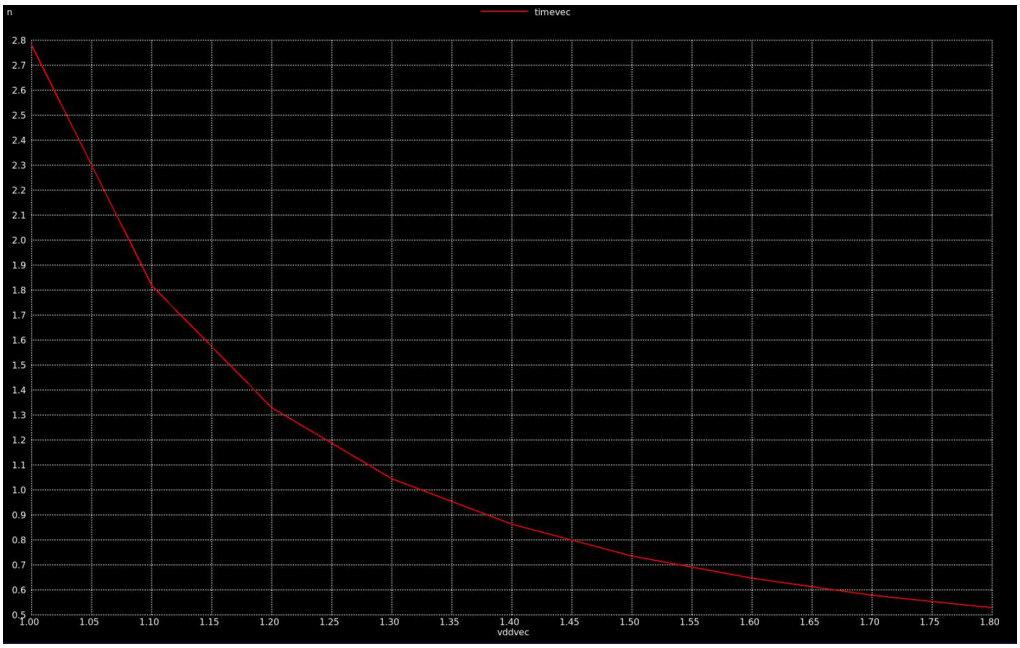




frequency vs Vdd



Time period vs Vdd



Values of frequency and time period with parasitic values

Constant values
constants Wed Jan 22 06:48:28 UTC 2025

Index	vddvec
0	1.000000e+00
1	1.100000e+00
2	1.200000e+00
3	1.300000e+00
4	1.400000e+00
5	1.500000e+00
6	1.600000e+00
7	1.700000e+00
8	1.800000e+00

Constant values
constants Wed Jan 22 06:48:28 UTC 2025

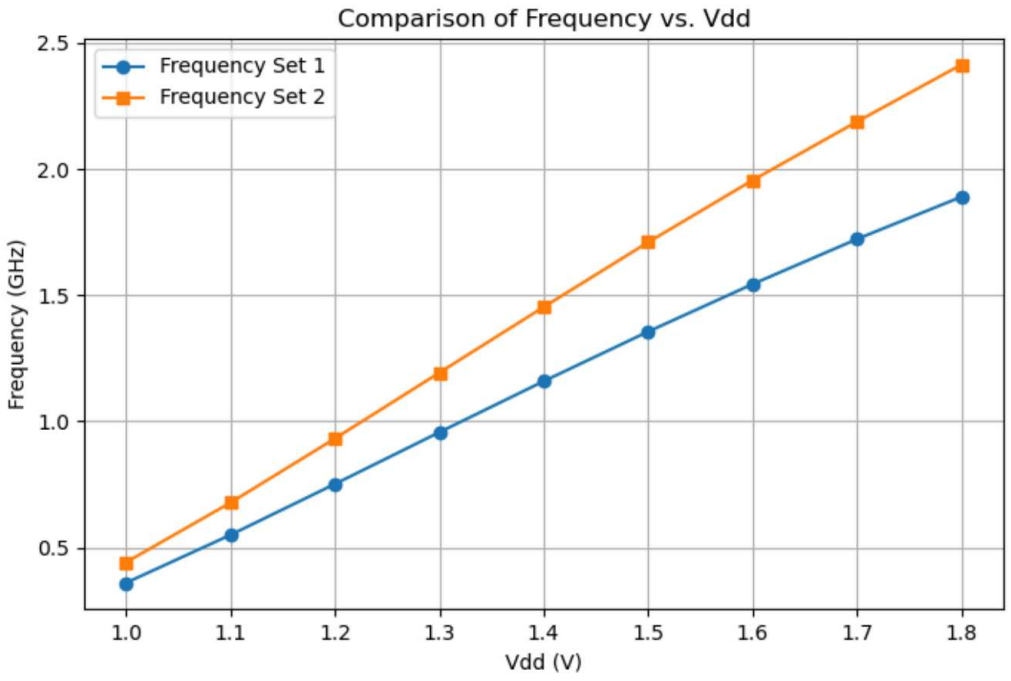
Index	freqvec
0	3.597717e+08
1	5.496954e+08
2	7.516428e+08
3	9.568004e+08
4	1.159311e+09
5	1.356036e+09
6	1.544175e+09
7	1.722834e+09
8	1.890524e+09

Constant values
constants Wed Jan 22 06:48:28 UTC 2025

Index	timevec
0	2.779541e-09
1	1.819189e-09
2	1.330419e-09
3	1.045150e-09
4	8.625811e-10
5	7.374435e-10
6	6.475952e-10
7	5.804389e-10
8	5.289539e-10

Values of frequency and time period with out parasitic values

```
Index   vddvec
--------------------------------------------------------------------------------
0       1.000000e+00
1       1.100000e+00
2       1.200000e+00
3       1.300000e+00
4       1.400000e+00
5       1.500000e+00
6       1.600000e+00
7       1.700000e+00
8       1.800000e+00
                                Constant values
                                constants  Wed Jan 22 06:48:28 UTC 2025
--------------------------------------------------------------------------------
Index   freqvec
--------------------------------------------------------------------------------
0       4.410685e+08
1       6.774513e+08
2       9.318293e+08
3       1.192913e+09
4       1.453660e+09
5       1.710315e+09
6       1.955991e+09
7       2.188518e+09
8       2.414532e+09
                                Constant values
                                constants  Wed Jan 22 06:48:28 UTC 2025
--------------------------------------------------------------------------------
Index   timevec
--------------------------------------------------------------------------------
0       2.267232e-09
1       1.476121e-09
2       1.073158e-09
3       8.382838e-10
4       6.879189e-10
5       5.846876e-10
6       5.112497e-10
7       4.569302e-10
8       4.141589e-10
ngspice 7 ->
```



Frequency set 1 : frequency of the ring oscillator without the layout capacitance
Frequency set 2 : frequency of the ring oscillator with the layout capacitance