EE5311 Tutorial2

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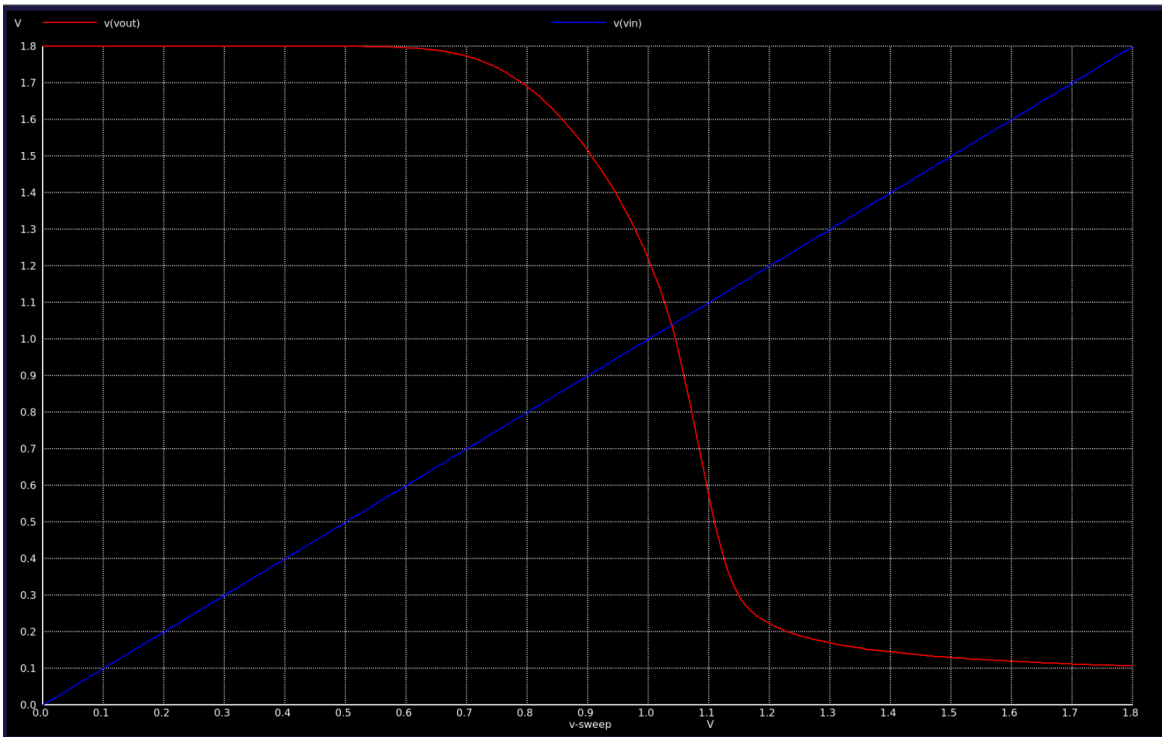
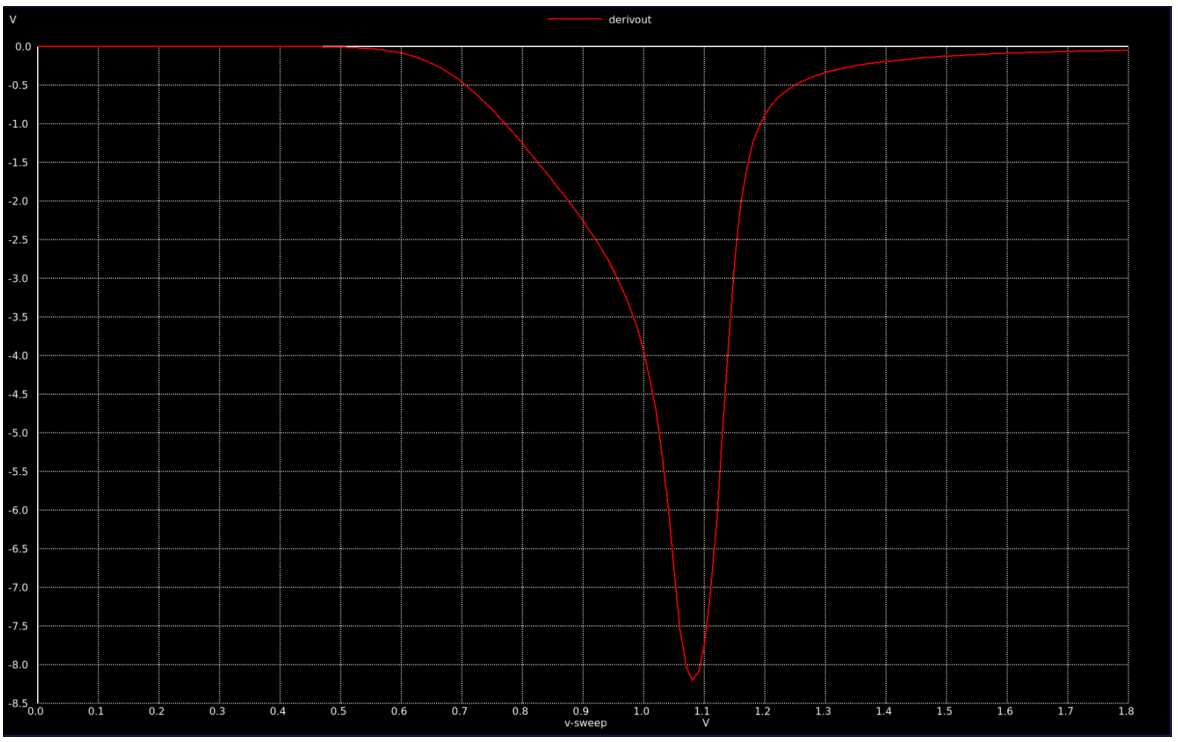
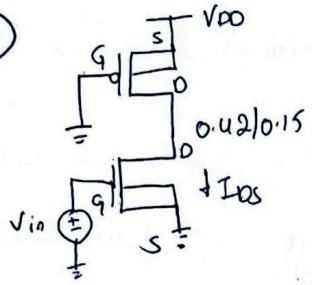
1. Size the pMOS transistor so that VOL = 0.1V. Using Ngspice, plot the DC transfer characteristic.



derivative and and low noise margins



1)



saturation

linear

$$(I_{D,lin})_n = (I_{D,sat})_p$$

$$\left(\frac{W_n}{L_n}\right)\mu_n C_{ox_n}\frac{(V_{GS}-V_{TH})V_{DS}(1+\lambda V_{DS})}{1+E_{DS}/E_{nL}} = \frac{\mu_p C_{ox_p}}{2}(V_{GS}-V_{tp})^2(1+\lambda|V_{DS}|)\times\frac{E_{CP}L}{E_{CP}L+V_{GS}-V_{tp}}\left(\frac{W_p}{L_p}\right)$$

$$25\times 834\times 2.8\left(\frac{1.1}{1.1}\right)\times 0.1\times(1.018) = \frac{9\times 816}{2}(1.1)^2(1+0.306)\times\frac{0.83}{1.93}\left(\frac{(W_P)}{0.15}\right)$$

$$W_P = \frac{50\times 834\times 2.8\times 0.11\times 1.018\times 1.93\times 0.15}{9\times 816\times 1.306\times 0.83\times 1.1\times 1.21} = \frac{3785}{7960\times 1.21} = 0.39\,\mu m$$

$$: 0.34\mu m$$

for $L: 0.3\mu m$

$$W_P = \frac{0.34\times 0.42\times 2}{0.62} = 0.46$$

$$(W/L)_P = 1.53$$

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Using SPARSE 1.3 as Direct Linear Solver
 Reference value :  0.00000e+00
No. of Data Rows : 181
vil                    =  7.712411e-01
vih                    =  1.191576e+00
vm                     =  1.058823e+00
NML: 0.771241 NMH: 0.608424
ngspice 7 -> 
```

(a) Find the inverter threshold voltage. (b) Plot the derivative and obtain the high and low noise margins. Do an approximate calculation using the analytical models and compare with the simulated value. (c) Assuming Vin = VDD, find the average power dissipated and compare with the analytically obtained value

a) $V_{inv} = \frac{\sqrt{K_r}}{\sqrt{K_r}+1}(V_{DD}-|V_{TP}|) + \frac{V_{TN}}{1+\sqrt{K_r}}$

$K_r = \frac{k_p(W/L)_p}{k_n(W/L)_n} = \frac{1.53 \times 9 \times 816}{2.8 \times 25 \times 834} = \frac{11236}{58380} = 0.19$

$V_{inv} = \frac{0.43}{1.43}(1.1) + \frac{0.7}{1.43} = \frac{1.18}{1.43} = 0.82V$

b) $V_{iH} = V_{th} + 2V_{out} - \frac{1}{2R_L k_n (W/L)_n}$

$= 0.7 + 0.2 - \frac{1}{2 \times 26 \times 10^{-3} \times 0.025 \times 0.0083 \times 2.8}$

$= 0.7 + 0.2 - \frac{1}{15.17}$, $0.9 - 0.06 = 0.84V$

$V_{iL} = V_{th} + \frac{1}{R_L(2k_n(W/L)_n)} = 0.7 + 0.06 = 0.76V$

c) $P_{dis} = V_{in} I_{ds} = V_{in}\left\{\left(\frac{W}{L}\right)_p \times \frac{\mu_p C_{ox}}{2}(V_{GS}-V_{TP})^2(1+\lambda V_{DS}) \times \frac{E_{tpL}}{E_{tL}+V_{GS}-V_{TP}}\right]$

$= 1.8 \times \left[1.53 \times \frac{9 \times 816}{2} \times 0.62 \times 1.306 \times 1.21\right] \times 10^{-8}$

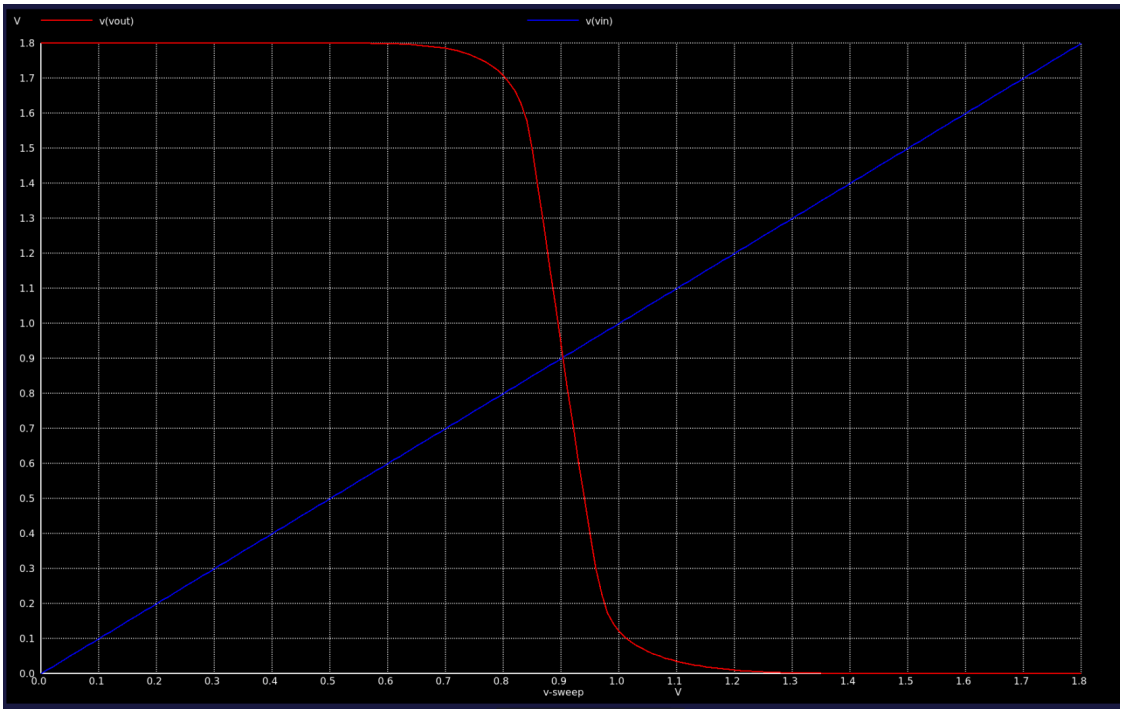
$= 1.8V \times [55\mu A]$

$= 100\mu W$

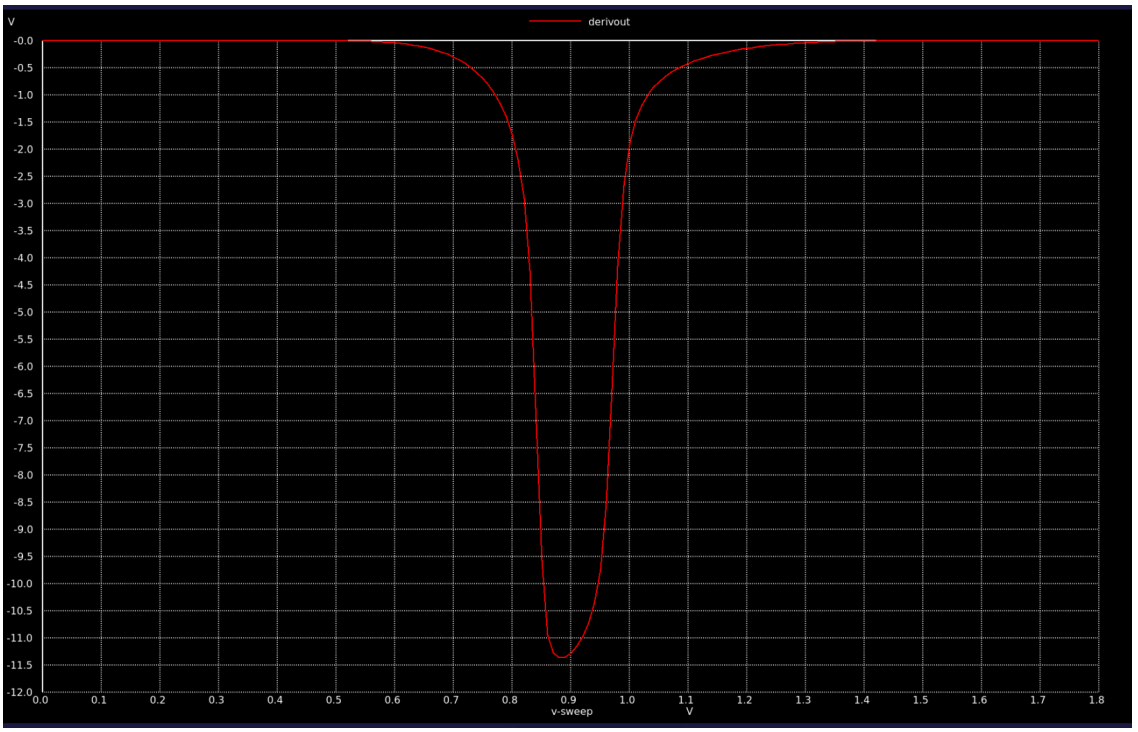
$= 0.1mW$

Power according to the simulated is IV
I = 45uA
V=1.8v
Power = 0.8mW

2. inverter threshold voltage Vinv = VDD/2. And DC transfer characteristic.



derivative and obtain the noise margins

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Using SPARSE 1.3 as Direct Linear Solver
 Reference value :  0.00000e+00
No. of Data Rows : 181
vil                =  7.712492e-01
vih                =  1.030598e+00
vm                 =  9.030870e-01
NML: 0.771249 NMH: 0.769402
ngspice 7 -> 
```
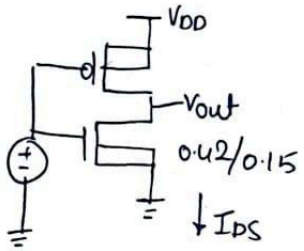

② 

a) $V_{inv} = V_{DD}/2$

$$V_{inv} = \frac{\sqrt{K_r}}{\sqrt{K_r}+1}(V_{DD}-|V_{TH}|) + \frac{V_{Tn}}{\sqrt{K_r}+1}$$

$$0.9 = \frac{1.1\sqrt{K_r}+0.7}{1+\sqrt{K_r}} \Rightarrow \frac{0.9}{1} + \frac{0.9}{1}\sqrt{K_r} = 1.1\sqrt{K_r}+0.7$$

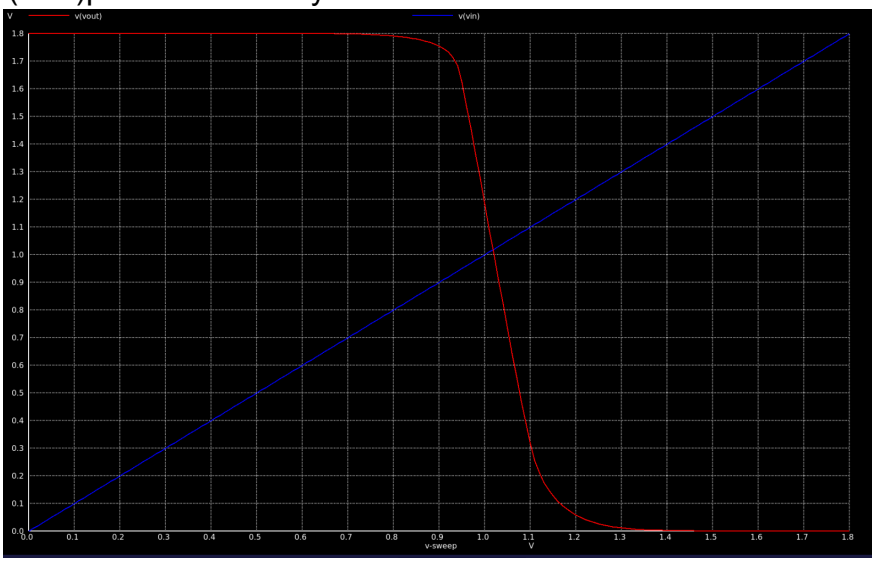
$$0.2\sqrt{K_r} = 0.2 \Rightarrow K_r = \frac{1.21}{0.49} = 2.46 \quad K_r = 1$$

$$K_r = \frac{K_p(W/L)_p}{K_n(W/L)_n} \Rightarrow$$

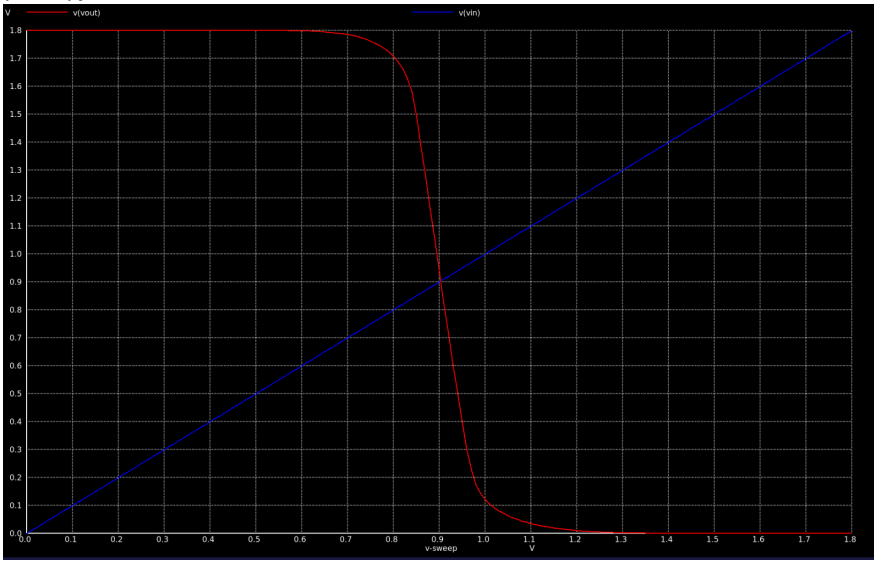
$$\Rightarrow (W/L)_p = \frac{K_n}{K_p}(W/L)_n = \frac{25\times834}{9\times816}(W/L)_n$$

$$(W/L)_p = 2.83\left(\frac{W}{L}\right)_n = 7.9$$

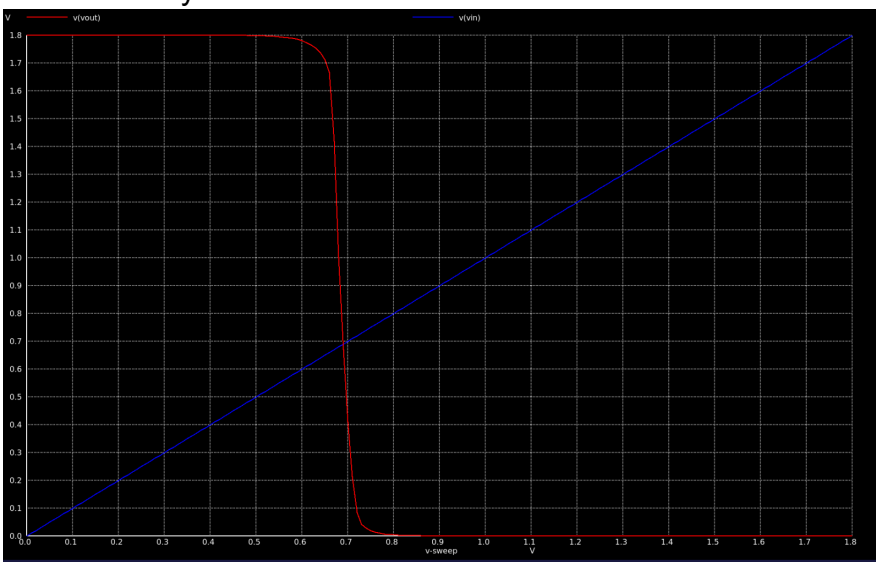
(W/L)p is increased by a factor of 10



(W/L)p is constant



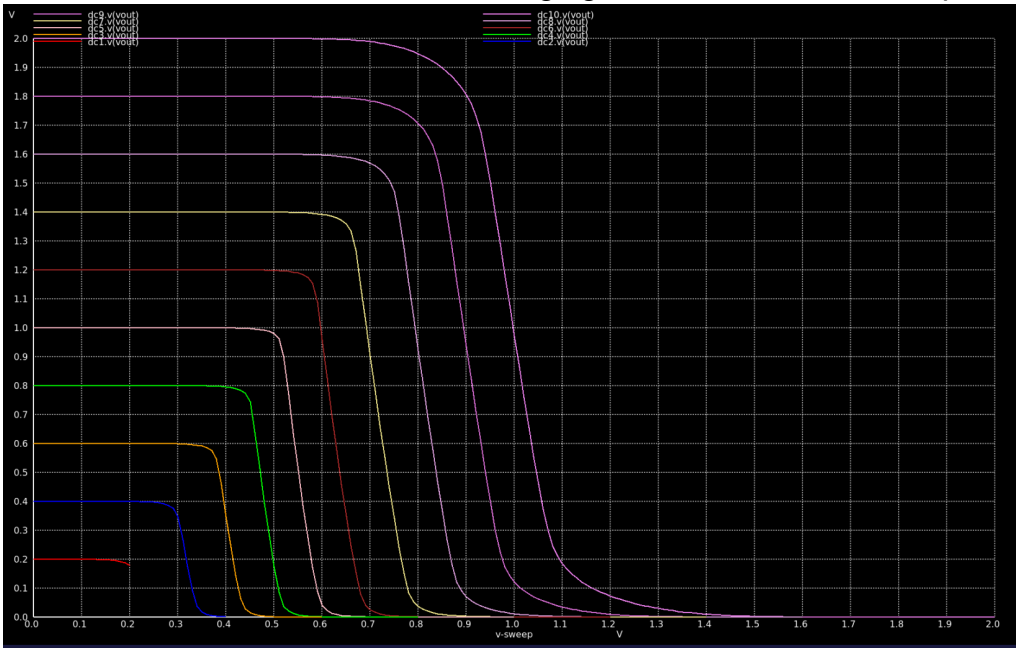
Decreased by a factor of 10



- **Increasing (W/L)p(W/L)_p(W/L)p by a factor of 10:**
  - The PMOS transistor becomes stronger (higher drive current for the same VgsV_{gs}Vgs).
  - The transition region shifts towards lower VinV_{in}Vin, meaning VinvV_{inv}Vinv decreases.
  - The slope of the DC transfer characteristic becomes steeper, which may improve noise margins.
- **Decreasing (W/L)p(W/L)_p(W/L)p by a factor of 10:**
  - The PMOS transistor becomes weaker.
  - The transition region shifts towards higher VinV_{in}Vin, meaning VinvV_{inv}Vinv increases.
  - The slope of the DC transfer characteristic becomes shallower, reducing noise margins.

In summary, increasing (W/L)p(W/L)_p(W/L)p shifts the threshold voltage downward, while decreasing it shifts the threshold upward.

DC transfer characteristic for VDD ranging from 0.2V to 1.8V in steps of 0.2V.



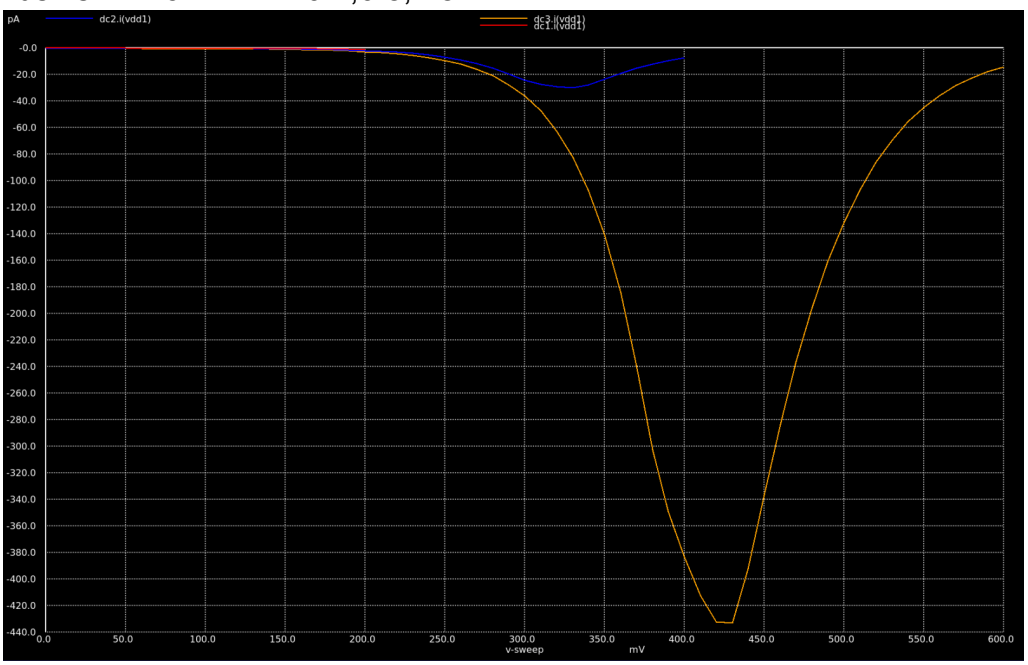
Evaluating for Different VDDV_{DD}VDD Values:

- At very low VDDV_{DD}VDD (e.g., 0.2V), both NMOS and PMOS may operate in subthreshold regions, leading to a poor transition.
- At higher VDDV_{DD}VDD (e.g., 1.8V), the transistors operate in strong inversion, leading to a well-defined switching behavior.

Adjusting (W/L)p(W/L)_p(W/L)p to Achieve Vinv≈VDD/2V_{inv} \approx V_{DD}/2Vinv≈VDD/2:

- If VinvV_{inv}Vinv is too high, increase (W/L)p(W/L)_p(W/L)p to strengthen PMOS.
- If VinvV_{inv}Vinv is too low, decrease (W/L)p(W/L)_p(W/L)p to weaken PMOS.

Ids vs Vin for VDD = 0.2,0.8,1.8V.



Peak Ids Values

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Using SPARSE 1.3 as Direct Linear Solver

No. of Data Rows : 221
imax: 1.19233E-12 2.98999E-11 4.32958E-10
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