EE5311 Tutorial_6b Report

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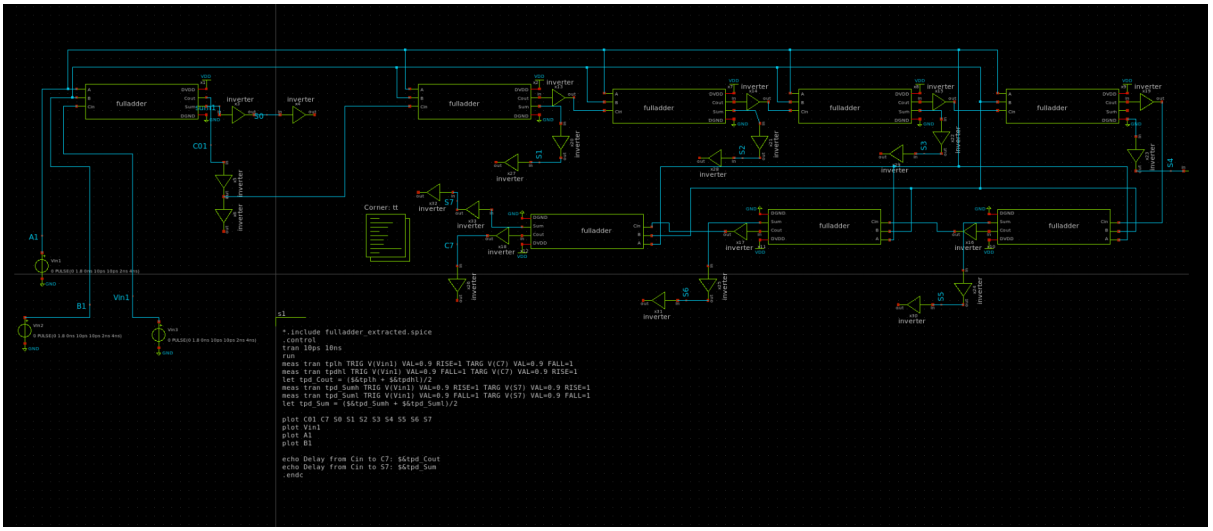
2. Draw the schematic of a 8-bit ripple-carry adder using the above mirror-symmetric full adder and trace its critical path.
   (a) Measure the delay of the critical path if the MSB sum and carry bits (S_7, C_7) drive a unit inverter each.
   (b) Compare the measured delay with the delay estimated using logical/electrical/branching effort.
   (c) Draw the layout of the complete ripple-carry adder using the above full-adder layout and inverter layout from Assignment 5. Ensure that aspect ratio (width/height) of your layout is in the range $[0.9, 1.1]$. Measure the layout extracted delay and compare it with the pre-layout delay.

Critical Path

- The **critical path** is the longest delay path.
- In RCA, it's from **Cin** → **C1** → **C2** → **...** → **C7** → **S7**.
- The delay adds up due to carry propagation through all 8 stages.



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run simulation not started
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tpdhl               =  -1.889691e-09 targ=  1.253093e-10 trig=  2.015000e-09
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Delay from Cin to S7: 3.28595E-10
ngspice 7 -> 
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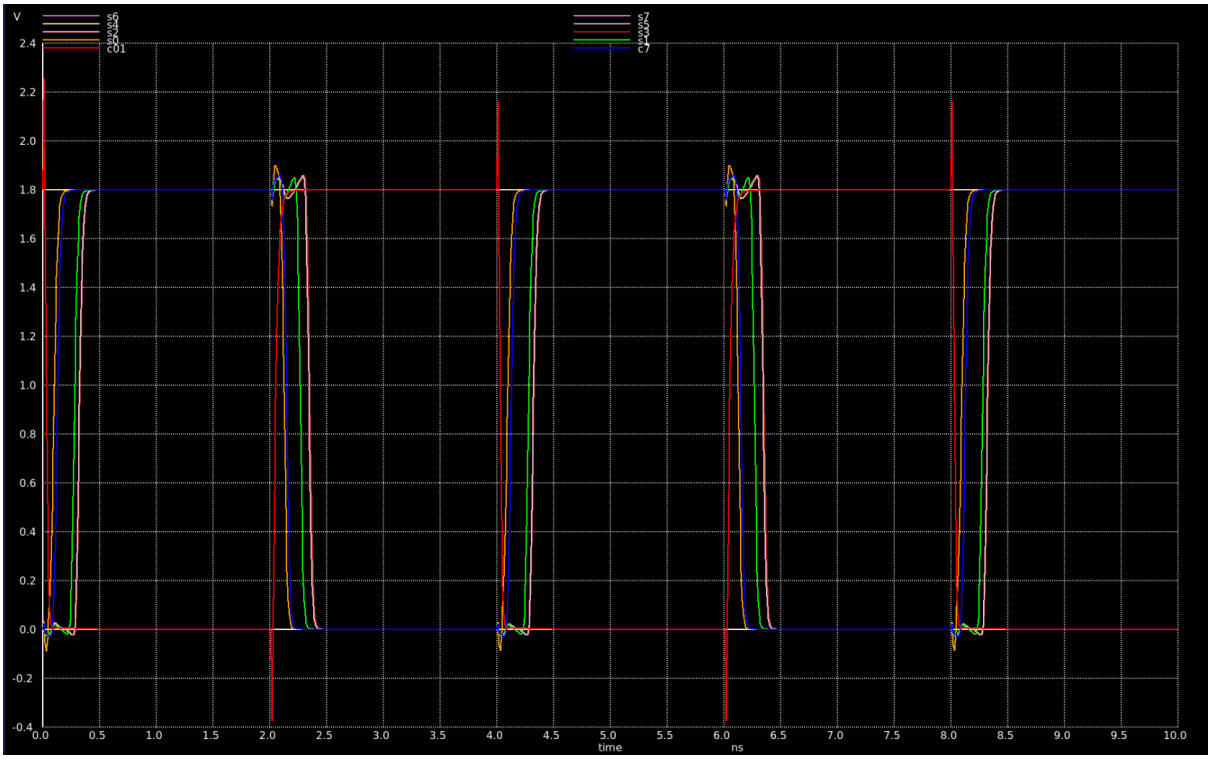
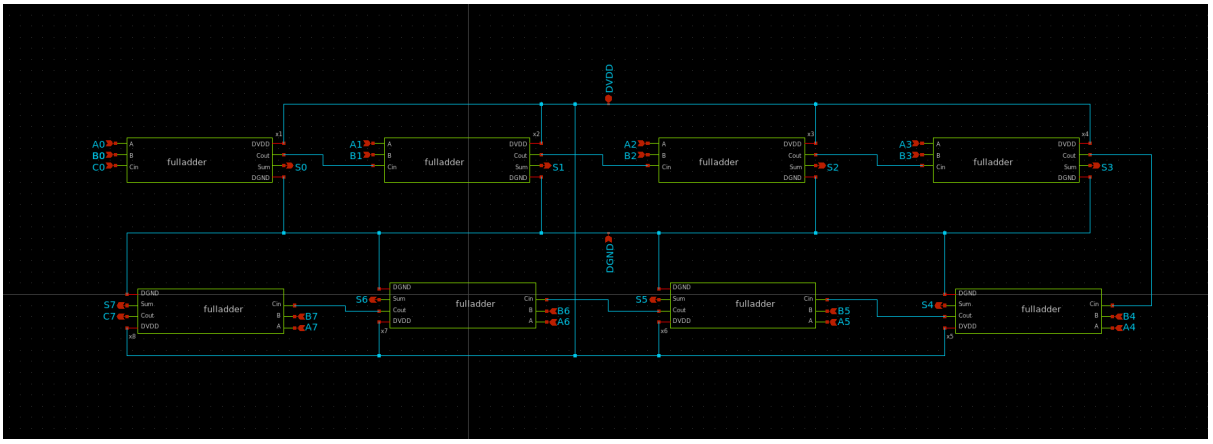
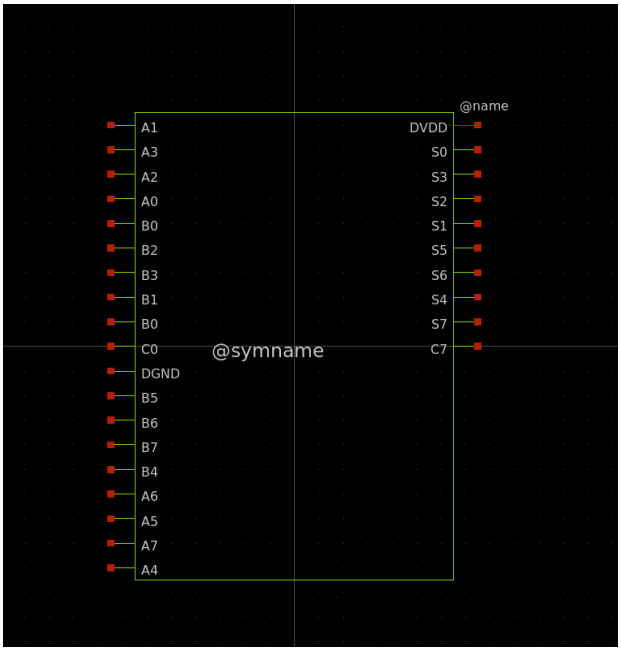
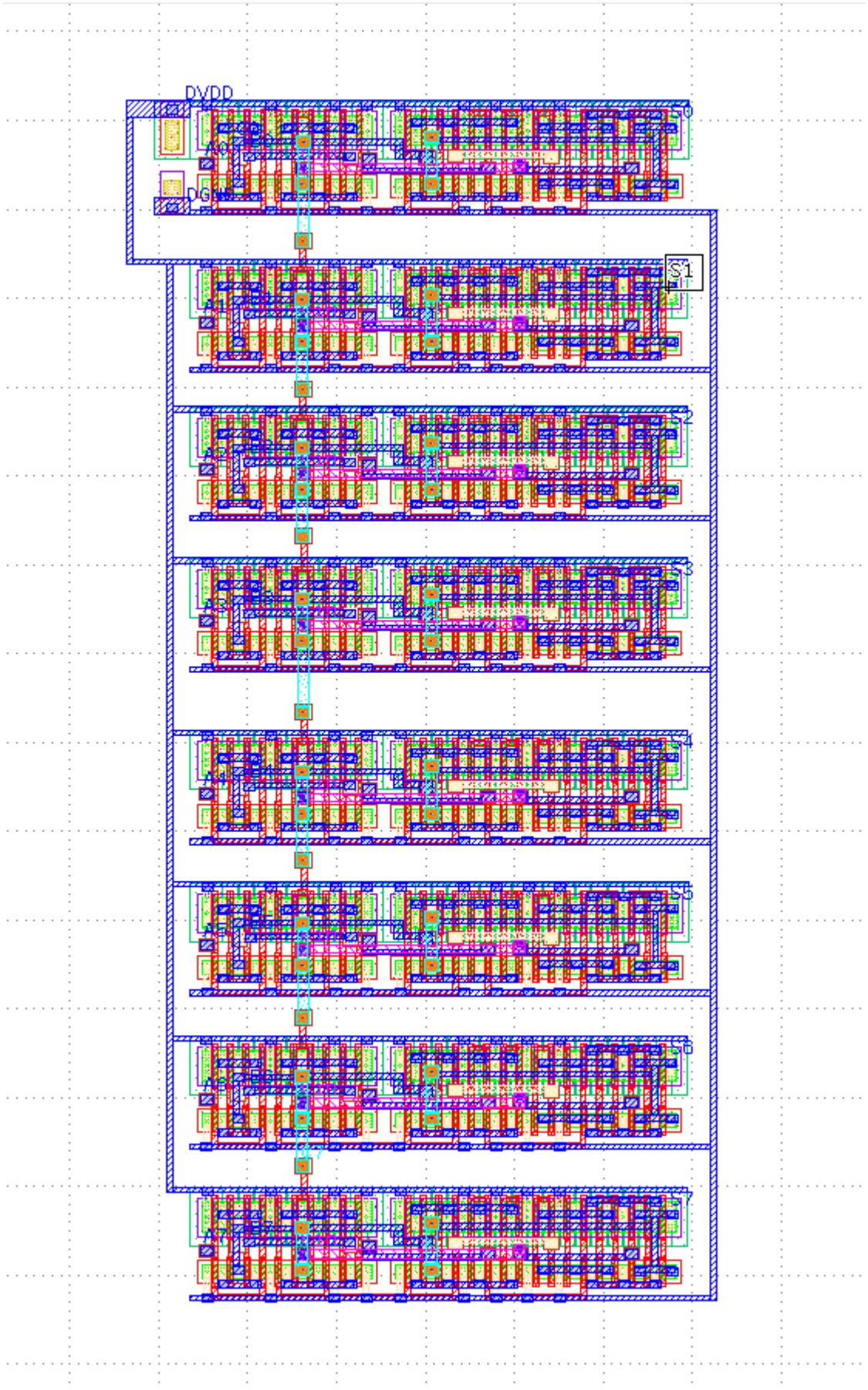


(b) Compare Delay with Logical/Electrical/Branching Effort

- **Logical Effort (LE)**: An estimation technique using logical effort (`g`), parasitic delay (`p`), and electrical effort (`h = C_load / C_in`).
- For RCA:
  - Each full adder stage has `g ≈ 1` for carry path.
  - Let `p ≈ 1` and fanout ≈ 1 (as load is a unit inverter).
- Total delay:
  $D = N \times (g \cdot h + p)$
  For `N = 8`:
  $D_{LE} = 8 \times (1 \cdot 1 + 1) = 16 \text{ units}$


DVDD
DGND
A0
B0
C0
A1
B1
A2
B2
A3
B3
fulladder
S0
S1
S2
S3
S7
C7
S6
S5
S4
B7
A7
B6
A6
B5
A5
B4
A4


@name
@symname
A1
A3
A2
A0
B0
B2
B3
B1
B0
C0
DGND
B5
B6
B7
B4
A6
A5
A7
A4
DVDD
S0
S3
S2
S1
S5
S6
S4
S7
C7


DVDD
S1