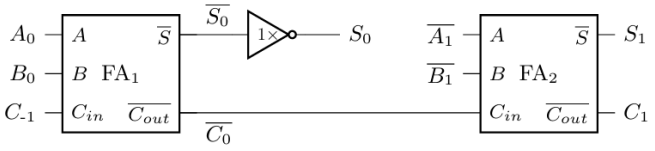
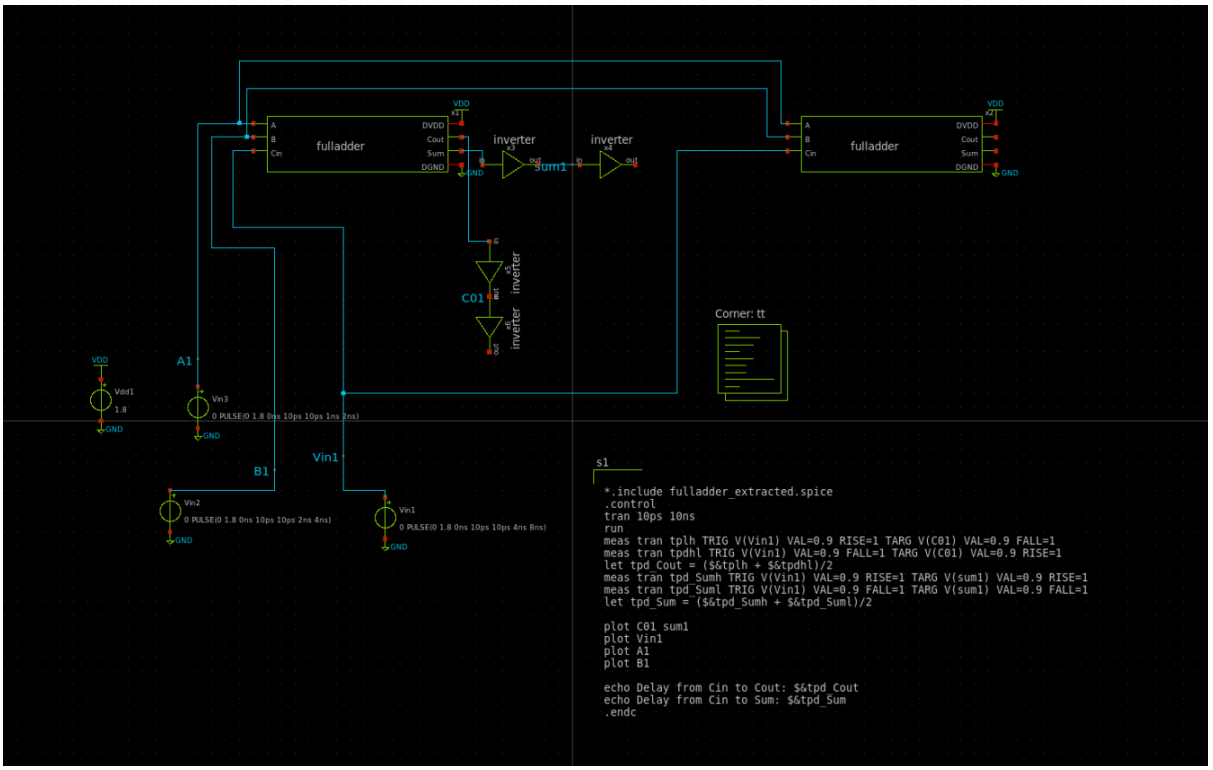
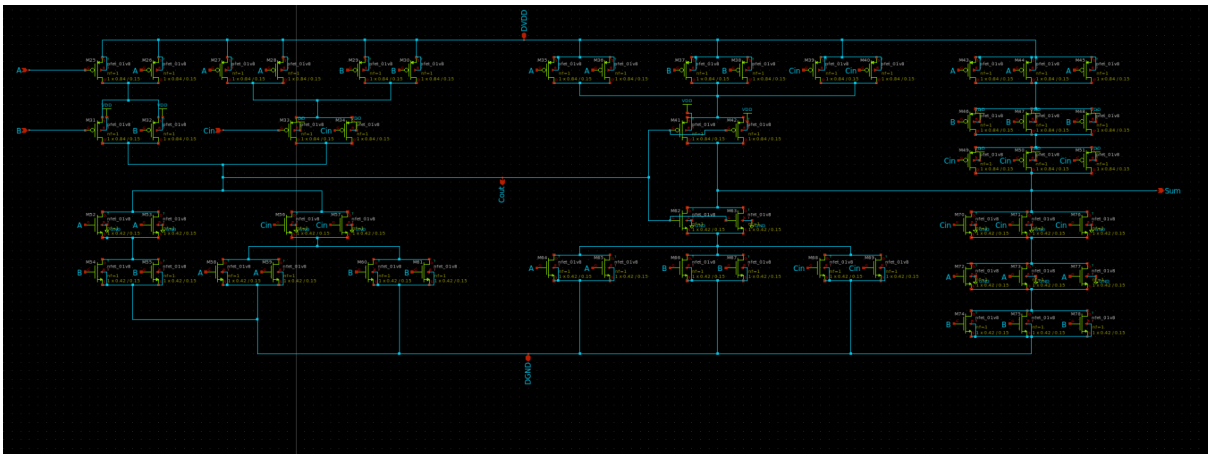
EE5311 Tutorial_6a
L.Pradeep EE22B074

1. Draw schematic for the carry and sum logic in a mirror-symmetric full adder done in class. Size the p/nMOS to minimize the delay from input to output carry and the stage effort of the carry logic is four when used in a ripple carry adder. Create a symbol for the full adder and connect two full adders as shown below:

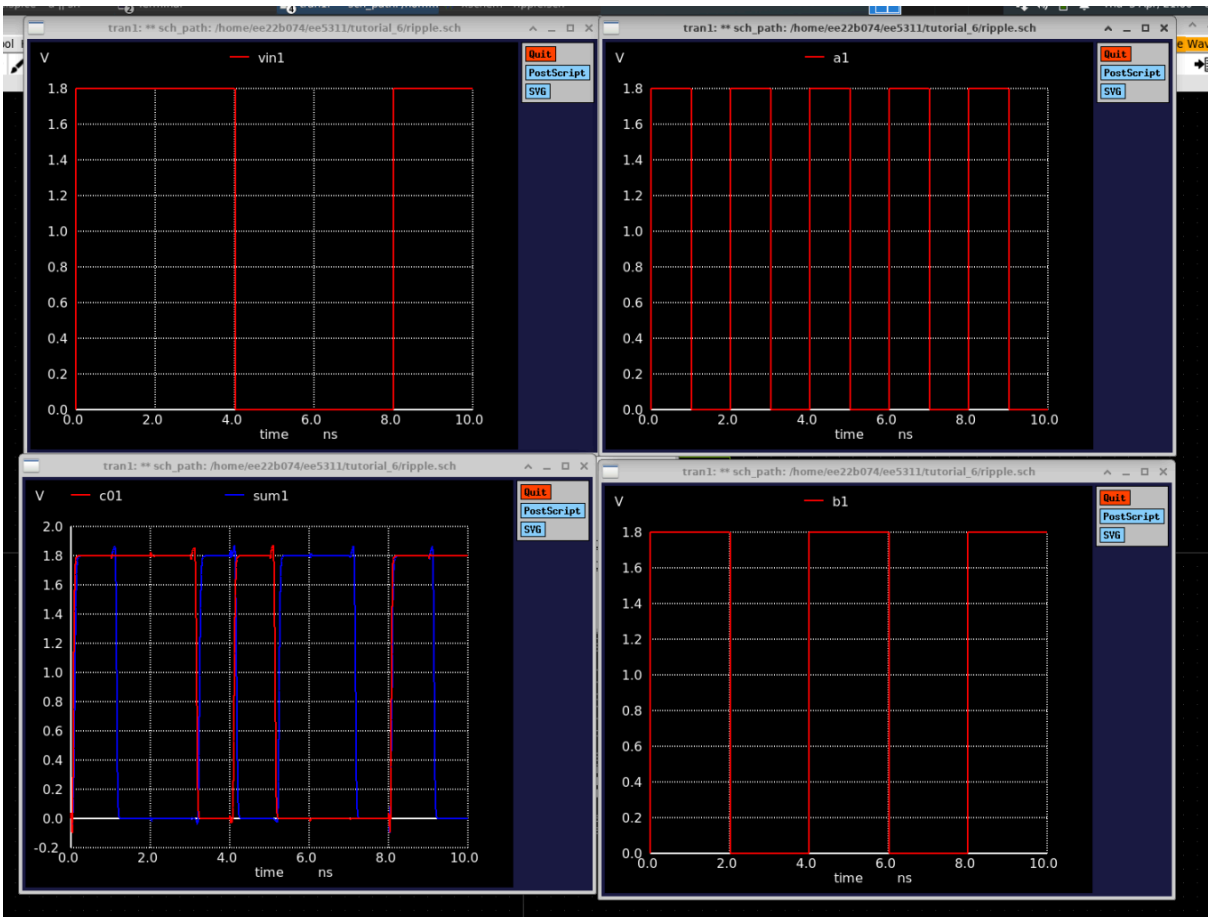




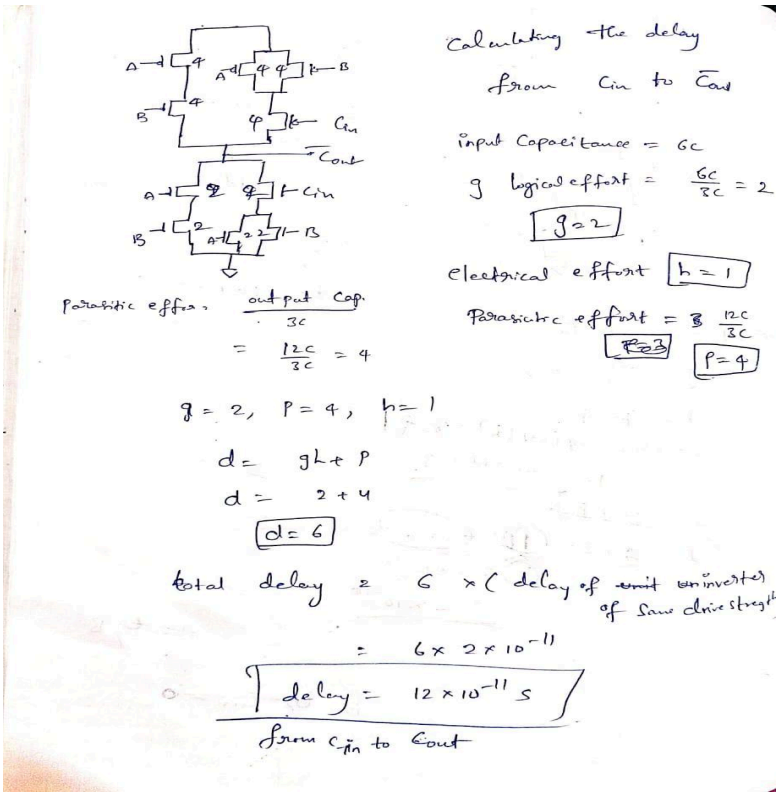


(a) Measure the delays: (i) from C_{-1} to $\overline{C_0}$, and (ii) from C_{-1} to $\overline{S_0}$.

```
 Reference value :  8.23960e-09
No. of Data Rows : 1040
Warning: No job (tran, ac, op etc.) defined:
run simulation not started
tplh                =  2.727253e-11 targ=  3.227253e-11 trig=  5.000000e-12
tpdhl               =  3.335492e-11 targ=  2.048355e-09 trig=  2.015000e-09
tpd_sumh            =  2.076368e-09 targ=  2.081368e-09 trig=  5.000000e-12
tpd_suml            =  -1.976783e-09 targ=  3.821670e-11 trig=  2.015000e-09
Delay from Cin to Cout: 3.03137E-11
Delay from Cin to Sum: 4.9795E-11
ngspice 7 ->
```



(b) How do the measured delays compare against that estimated using logical and electrical effort?



Calculating the delay from Cin to Cout

input Capacitance = 6c

g logical effort = $\frac{6c}{3c} = 2$

g = 2

electrical effort h = 1

Parasitic effort = 3 $\frac{12c}{3c}$

P = 4

Parasitic effort = $\frac{\text{output Cap.}}{3c}$

$= \frac{12c}{3c} = 4$

g = 2, P = 4, h = 1

d = gh + P

d = 2 + 4

d = 6

total delay = 6 × (delay of unit inverter of same drive strength

$= 6 \times 2 \times 10^{-11}$

delay = 12×10^{-11} s

from Cin to Cout

delay Calculation.
(Cin to Sum)

Calculation of logical effort

$g = \frac{6+4}{3} = \frac{10}{3}$

$h = \frac{(3+2)2}{10} = 1\frac{10}{10} = 1$

$P = \frac{10}{3} = \frac{10}{3}$

delay = gh + P

$= \frac{10}{3} + \frac{10}{3} = \frac{20}{3}$

$d = \frac{20}{3} \times 2 \times 10^{-11}$

$d = \frac{40}{3} \times 10^{-11} = 13.33 \times 10^{-11}$

$d = 1.33 \times 10^{-10}$ sec

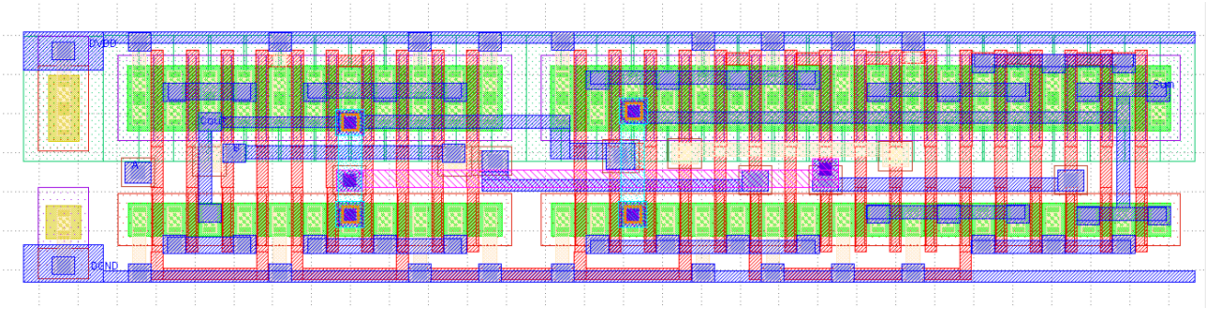
delay from Cin

total delay from Cin to Sum

delay = $1.33 \times 10^{-10} + 1.2 \times 10^{-10}$

delay = 2.53×10^{-10} sec

(c) Draw the layout for the full-adder and measure the layout extracted delay and compare it against the pre-layout delay. Use diffusion sharing and num fingers to create a compact layout. The height of the full adder should be the same as the inverter in Assignment 5.

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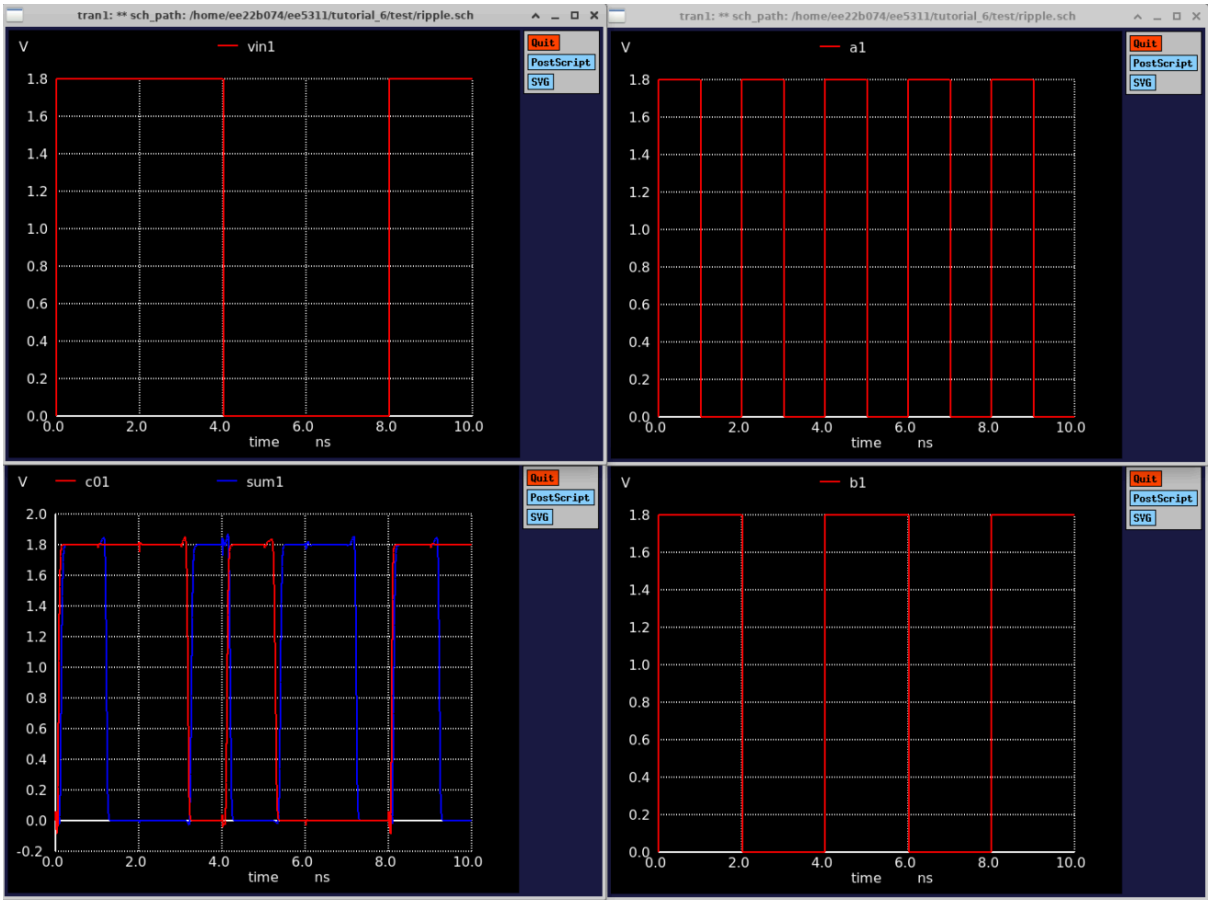
run simulation not started
tplh                =  3.753856e-11 targ=  4.253856e-11 trig=  5.000000e-12
tpdhl               =  5.204765e-11 targ=  2.067048e-09 trig=  2.015000e-09
tpd_sumh            =  2.103724e-09 targ=  2.108724e-09 trig=  5.000000e-12
tpd_suml            =  -1.922801e-09 targ=  9.219862e-11 trig=  2.015000e-09
Delay from Cin to Cout: 4.47931E-11
Delay from Cin to Sum: 9.046E-11
ngspice 7 -> 
```



Stick Diagrams