DHEERAJ SINGH

MEMORY LAYOUT DESIGN ENGINEER
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SUMMARY:

Experienced Memory Layout Engineer proficient in Cadence Virtuoso, Custom Compiler, Glade and Calibre tools (DRC,LVS, Antenna). Strong knowledge of CMOS, Memory Layout fundamentals, and Shell Scripting, with a keen eye for detail and problem-solving. Proficient in Layout design, routing and debugging DRC issues.

TECHNICAL SKILLS:

- 2year experience working as Memory layout Engineer.
- Experience in the Custom Compiler, Cadence tools including Virtuo so schematic editor,Virtuoso Layout L/XL, Glade, LTspice and Hspice.
- Wide knowledge of ICV/Calibre tools like DRC /LVS /RC-extraction and Antenna check.
- Design Knowledge of CMOS technologies in 110nm, 90nm, 65nm, 15nm.
- Knowledge of CMOS, FinFET and BJT.
- Solid grasp of Fundamental semiconductor physics.
- Strong Knowledge of Short Channel Effects and Second Order Effects.
- Familiarity with Layout fundamentals (e.g. Matching, Latch-up, Electro-migration, cross-talkand shielding, IR - drop, active and passive parasitic devices, Current Mirrors etc).
- Sound knowledge of routing, debugging DRC, and managing Layout design.
- Experience Operating System : Windows, Linux.

TOOLS SKILL-SET:

Custom Layout	Custom Compiler, Cadence Virtuoso, Glade
Physical Verification	ICV /Calibre (DRC, LVS, RC extraction)

PROJECT DETAIL:

PROJECT 1

Project Name	Layout of Standard cells
Description	Worked on logic gates i.e.. Inverter, AND,OR, NAND, NOR, XOR, XNOR, All cells have under one through Half DRC with Minimum Poly pitches.
Role & Contribution	Layout Design & physical Verification DRC, LVS
Tools	Custom Compiler, ICV

PROJECT 2

Project Name	BITCELL (6TSRAM)
Description	A bitcell (6TSRAM) is a device that stores one bit of data. It is composed of 6 transistors.
Role & Contribution	Layout Design & physical Verification DRC,LVS
Tools	Custom Compiler, ICV

PROJECT 3

Project Name	Digital Multiplexer
Description	A Multiplexer is a device that allows one of the several analog or digital input signals which are to be selected and transmits the input that is selected into a single medium. Multiplexer is Also known as Data Selector
Role & Contribution	Layout Design & physical Verification DRC,LVS
Tools	Custom Compiler, ICV

PROJECT4

Project Name	Sense Amplifier
Description	A sense amplifier is a crucial component in memory circuits that detects and amplifies small voltage differences between complementary Bitlines, helping to read and Interpret stored data in memory cells.
Role & Contribution	Layout Design & physical Verification DRC,LVS
Tools	Custom Compiler, ICV

PROJECT 5

Project Name	Internal Clock Generator(ICG)
Description	The Internal Clock Generator is a circuit that produces stable clock signals, synchronizing the Timing of read and write operations with in the memory cells.
Role & Contribution	Layout Design & physical Verification DRC, LVS
Tools	Custom Compiler, ICV

TOTAL EXPERIENCE :- Up to 4 Years
Relevant Experience of 2 Years

ELBRUSLABS (INSEMI TECHNOLOGY PVT.LMT.)
DURATION - 21/06/2022 To 25/04/2024
DESIGNATION – JUNIOR ENGINEER (MEMORY LAYOUT)

Universal Telecom, Noida
DURATION:- Apr 2020 - March 2022

Linkquest TelecomLtd, Lucknow
DURATION:-Mar 2019 – Dec 2019

EDUCATION:

Qualification	University	Percentage
B.Tech (Electrical and Electronics Engineering)	**AKTU University Lucknow**	**61.03%**

PERSONAL DETAILS:-

Father's Name	:	Shonveer
Date of Birth	:	08,Oct,1996
Marital Status	:	Unmarried
Languages	:	English, Hindi
Nationality	:	Indian

DECLARATION

I here by declare that all above – mentioned information is true to the best of my knowledge and belief.

Date:

Place: