Unit 11 System Bus Structure

Structure:

11.1 Introduction

In the previous unit, you studied about numeric coprocessor, its data types, its architecture and other related concepts. The sometimes you may require that the 8086 has to adapt to as many situations as possible. So 8086 microprocessor operates in two, the minimum mode and the maximum mode. In this unit we will discuss these two modes of 8086. We know that bus is a set of conductors used for communicating information between the components in a computer system. A bus could be an internal bus or an external bus. Because an internal bus is ordinarily internal to an IC device and its construction is dependent on the device, the exact construction of these buses is of little interest to us. External buses, on the other hand, have common characteristics that must be understood when designing the overall architecture of a computer system. In this unit you will be introduced to the bus interface and the peripheral component interconnect (PCI) bus, the parallel printer interface (LPT) and universal serial bus (USB).

Objectives:

After studying this unit, you should be able to:

- list the types of basic 8086 configurations
- explain the 8086 configuration in minimum mode.
- explain the 8086 configuration in maximum mode
- discuss on 8086 system bus timing
- explain peripheral component interconnect (PCI) bus,
- discuss on parallel printer interface (LPT)

11.2 Basic 8086 Configurations

In order to adapt to as many situations as possible, the 8086 has been given two modes of operation, the minimum mode and the maximum mode. The minimum mode is used for a small system with a single processor, a system in which the 8086 generates all the necessary bus control signals directly (thereby minimizing the required bus control logic). The Maximum mode is for medium-size to large systems, which often include two or more processors. In order to understand this once again we look at the 8086 pin diagram shown in figure 11.1. Pin 33 (MN / $\overline{MX}$) determines the configuration option. When it is strapped to ground, the processor is to be used in a maximum mode configuration and when it is strapped to + 5 V it is to be operated in its minimum mode.

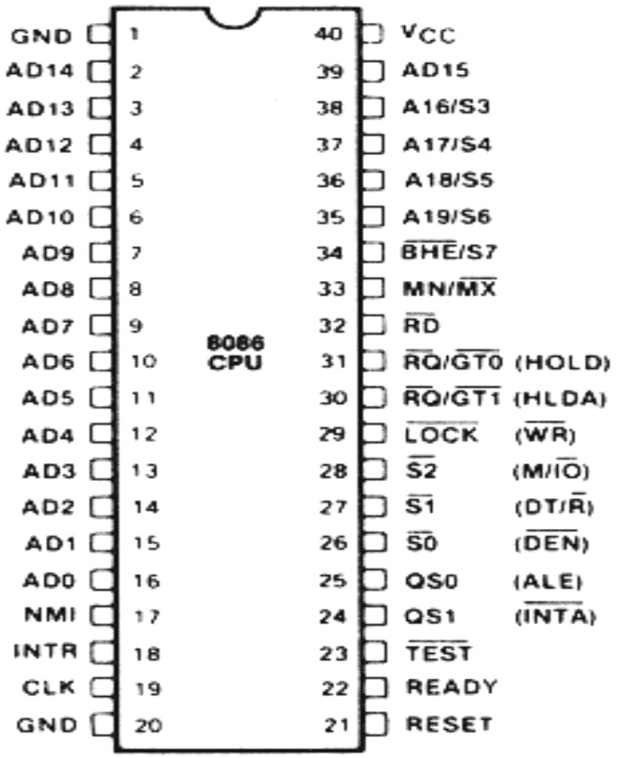


Figure 11.1: 8086 Pin diagram

11.2.1 Minimum Mode

A processor is in minimum mode when its MN / $\overline{MX}$ pin is strapped to +5 V. The definitions for pin: 24 through 31 for the minimum mode are given in figure 11.2 and a typical minimum mode configuration is shown in figure. 11.3.

Pin (s)	Symbol	In/Out (3 State)	Description
24	/INTA	O-3	Indicates recognition of an interrupt request. Consists of two negative going pulses in two consecutive bus cycles.
25	ALE	O	Outputs a pulse at the beginning of the bus cycle and is to indicate an address is available on the address pins.
26	/DEN	O-3	Output during the latter portion of the bus cycle and is to inform the transceivers that the CPU is ready to send or receive data.
27	DT / /R	O-3	Indicates to the set of transceivers whether they art to transmit (1) or receive (0) data.
28	M / /IO	O-3	Distinguishes a memory transfer from an I/O transfer. For a memory transfer it is 1. (For the 8088, the symbol is IO / /M and a 1 indicates an I/O transfer.
29	/WR	O-3	When 0, it indicates a write operation is being performed. It is used in conjuction with pins 28 (M / /IO) and 32 (/RD) to specify the type of transfer
30	HLDA	O	Outputs a bus grant to a requesting master. Pins with trisate gates are put in high impedance state while HLDA=1.
31	HOLD	I	Receivec bus requests from bus masters. The 8086/8088 will not gain control of the bus until this signal is dropped.

Figure 11.2: Pin definitions for the minimum mode

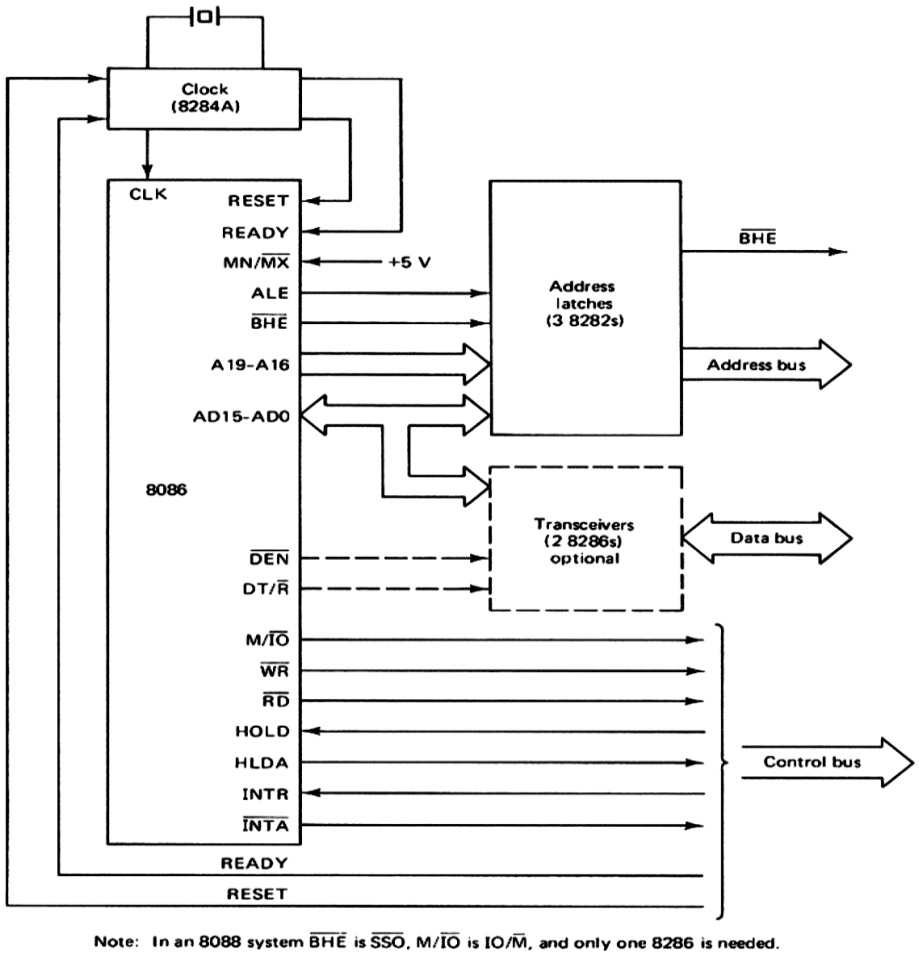


Figure 11.3: Minimum mode system

The address must be latched since it is available only during the first part of the bus cycle. To signal that the address is ready to be latched a 1 is put on pin 25, the address latch enable (ALE) pin. Typically, the latching is accomplished using Intel 8282s, as shown in figure 11.4. Because 8282 is an 8-bit latch, two of them are needed for a 16-bit address and three are needed if a full 20-bit address is used. In an 8086 system, $\overline{BHE}$ would also have to be latched. A signal on the strobe STB pin of 8282 latches the bits applied to the input data lines DI7-DI0. Therefore, STB is connected to the 8086's ALE pin and DI7-DIO are attached to eight of the address lines. An active low signal on the $\overline{OE}$ enables the latch's outputs DO7-DO0, and a

1 at this pin forces the outputs into their high-impedance state. In an 8086 single-processor system that does not include a DMA controller this pin is grounded.

If a system includes several interfaces, then drivers and receivers, which may not be needed on small, single-board systems, will be required for the data lines. The Intel IC device for implementing the transceiver (driver/receiver) block shown in figure 11.3 is the 8286 transceiver device. The 8286 contains 16 tristate elements, eight receivers, and eight drivers. Therefore, two 8286 ICs are needed in a 8086 system. Figure 11.4 shows how 8286s are connected into a system and a logic diagram of one of its cells.

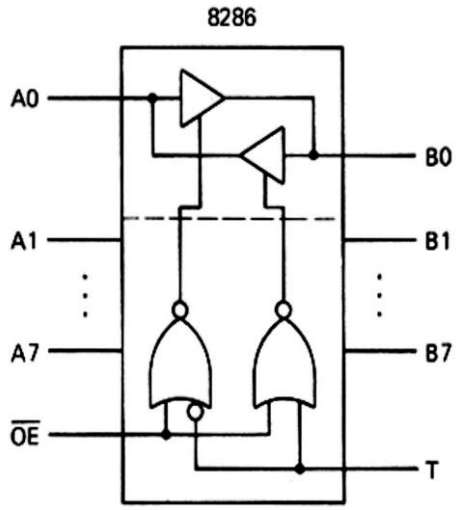


Figure 11.4: Internal logic of an 8286

The 8286 is symmetric with respect to its two sets of data pins, either the pins A7-A0 can be the inputs and B7-B0 the outputs, or vice versa: The output enable ($\overline{OE}$) pin determines whether or not data are allowed to pass through the 8286 and the transmit (T) pin controls the direction of the data flow. When $\overline{OE}$ = 1, data are not transmitted through the 8286 in either direction. If it is 0, then T = 1 causes A7-A0 to be the inputs and T = 0 results in B7-B0 being the inputs. In an 8086-based system the $\overline{OE}$ pin would be connected to the $\overline{DEN}$ pin, which is active low whenever the processor is performing an I/O operation. The A7-A0 pins are connected to

the appropriate address/data lines and the T pin is tied to the processor's DT/$\overline{R}$ pin. Thus, when the processor is outputting the data flow is from A7-A0 to B7-B0, and when it is inputting the flow is in the other direction. The processor floats the $\overline{DEN}$ and DT/$\overline{R}$ pins in response to a bus request on the HOLD pin.

The third component, other than the processor, that appears in figure 11.4 is an 8284 clock generator. This device, which is actually more than just a clock, is shown in figure 11.5 in addition to supplying a train of pulses at a constant frequency it synchronizes by bus ready(RDY) signals, which indicate an interface is ready to complete a transfer, and reset ($\overline{RES}$) signals, which initialize the system, with the clock pulses. Although these two signals may be sent at any time, the 8284A will not reflect them in its READY and RESET outputs until the trailing edge of the clock pulse in which they are received.

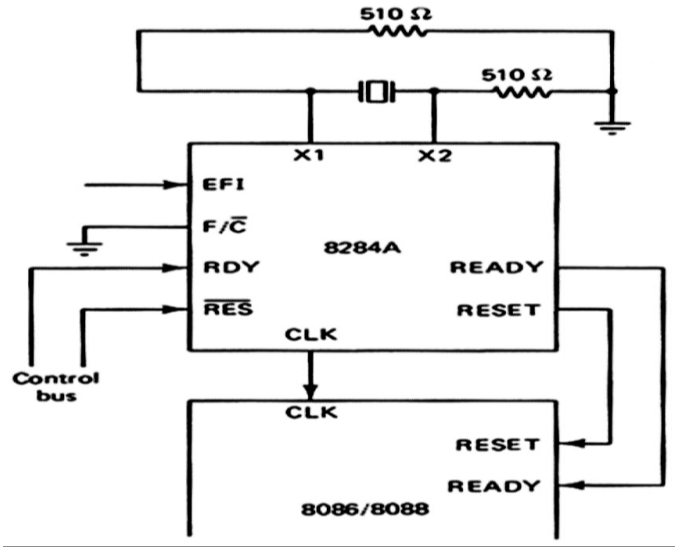


Figure 11.5: 8284A clock generator

Self Assessment Questions

1. A processor is in minimum mode when its _____ pin is strapped to +5 V.
2. _____is the Intel's IC transceiver device.
3. _____ is the clock generator.

11.2.2 Maximum Mode

A processor is in maximum mode when its MN/$\overline{MX}$ pin is grounded. The maximum mode definitions of pins 24 through 31 are given in figure 11.6 and a typical maximum mode configuration is shown in figure 11.7.

Pin(s)	Symbol	In/Out(3 State)	Description
24,25	QS1, QS0	O	Reflects the status of the instruction queue. This status indicates the activity in the queue during the previous clock cycle - see Chap. 11.
26, 27, 28	/S0, /S1, /S2	O-3	Indicates the type of transfer to take place during the current bus cycle: /S2 /S1 /S0 0 0 0 Interrupt acknowledge 0 0 1 Read I/O port 0 1 0 Write I/O port 0 1 1 Halt 1 0 0 Instruction fetch 1 0 1 Read memory 1 1 0 Write memory 1 1 1 Inactive - passive (1 represents high and 0 represents low.) The status becomes active prior to the beginning of a bus cycle and returns to inactive during the later part of the cycle.
29	/LOCK	O-3	Indicates the bus is not to be relinquished to other potential bus masters. It is initiated by a LOCK instruction prefix and is maintained until the end of the next instruction - see Chap.11. It is also active during and between the two /INTA pulses.
30	/RQ / /GT1	I/O	For inputting bus requests and outputting bus grants.
31	/RQ / /GT0	I/O	Same as /RQ / /GT1 except that a request on /RQ / /GT0 has higher priority.

Note: In maximum mode the 8086 and 8088 pins have the same definitions except for pin 34, which on the 8088 is always 1.

Figure 11.6: Maximum mode pin definitions

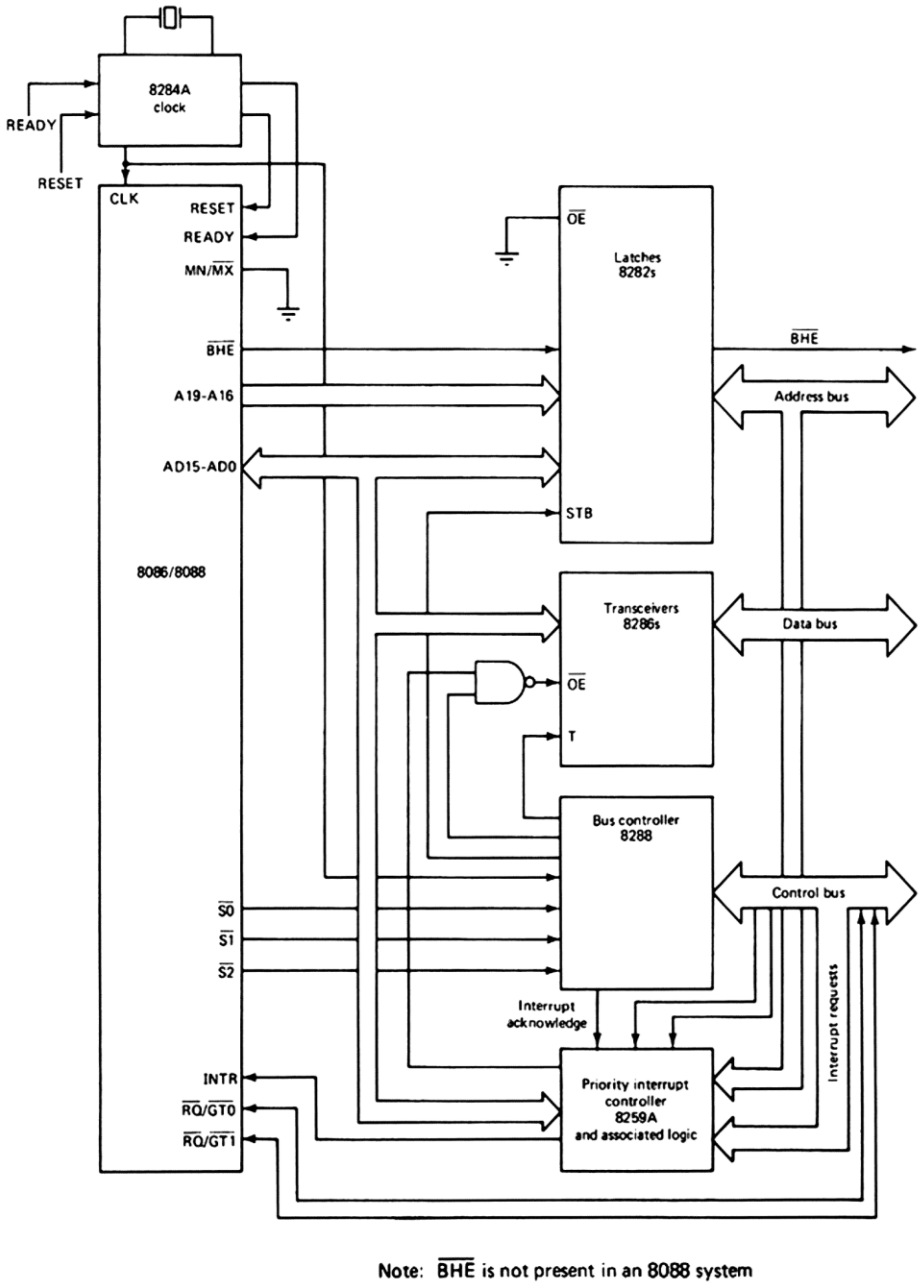


Figure 11.7: Maximum mode configuration

It is clear from figure 11.7 that the main difference between minimum and maximum mode configurations is the need for additional circuitry to translate

the control signals. This circuitry is for converting the status bits $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ into the I/O and memory transfer signals needed to direct data transfers, and for controlling the 8282 latches and 8286 transceivers. It is normally implemented with an Intel 8288 bus controller. Also included in the system is an interrupt priority management device; however, its presence is optional.

The $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ status bits specify the type of transfer that is to be carried out and when used with an 8288 bus controller they obviate the need for the M/$\overline{IO}$, $\overline{WR}$, $\overline{INTA}$, ALE, and DT/$\overline{R}$ and $\overline{DEN}$ signals that are output over pins 24 through 29 when the processor is operating in minimum mode. Except for the case $\overline{S0} = \overline{S1} = 1$, $\overline{S2}$ = 0 indicates a transfer between an I/O interface and the CPU and $\overline{S2}$ = 1 implies a memory transfer. The $\overline{S1}$ bit specifies whether an input or output is to be performed. From the status the 8288 is able to originate the address latch enable signal to the 8282s, the enable and direction signals to the 8286 transceivers and the interrupt acknowledge signals to the interrupt controller. The QS0 and QS1 pins are to allow the system external to the processor to interrogate the status of the processor instruction queue so that it can determine which instruction it is currently executing, and the $\overline{LOCK}$ pin indicates that an instruction with a LOCK prefix is being executed and the bus is not to be used by another potential master. The HOLD and HLDA pins become the $\overline{RQ}/\overline{GT0}$ and $\overline{RQ}/\overline{GT1}$ pins. Both bus requests and bus grants can be given through each of these pins. They are exactly the same except that if requests are seen on both pins at the same time, then the one on $\overline{RQ}/\overline{GT0}$ is given higher priority. A request consists of a negative pulse arriving before the start of the current bus cycle. The grant is a negative pulse that is issued at the beginning of the current bus cycle provided that:

1. The previous bus transfer was not the lower byte of a word to or from an odd address if the CPU is an 8086.
2. The first pulse of an interrupt acknowledgment did not occur during the previous bus cycle.
3. An instruction with a LOCK prefix is not being executed.

If condition 1 or 2 is not met, then the grant will not be given until the next bus cycle, and if condition 3 is not met, the grant will wait until the locked

instruction is completed. In response to the grant the three-state pins are put in their high impedance state and the next bus cycle will be given to the requesting master. The processor will be effectively disconnected from the system bus until the master sends a second pulse to the processor through the $\overline{RQ}$/ $\overline{GT}$ pin. An expanded view of a maximum mode system which shows only the connections to an 8288 is given in figure.11.8.

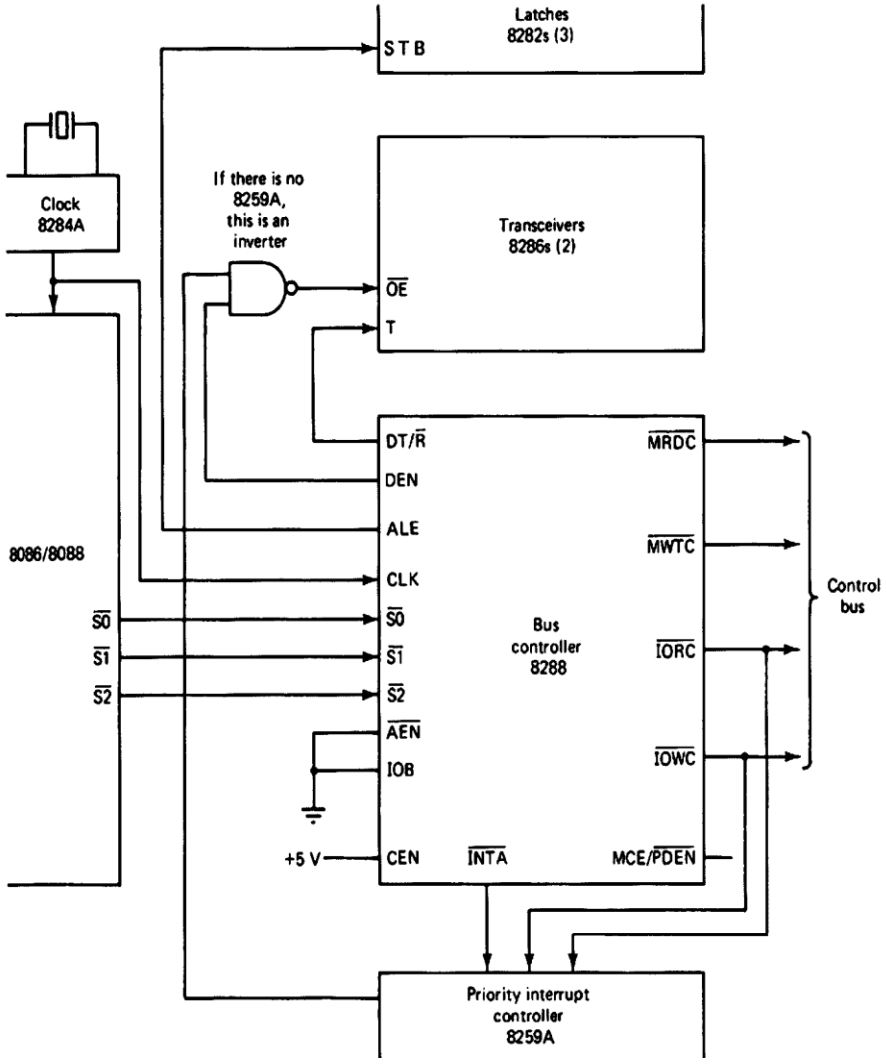


Figure 11.8: Connection to an 8288 bus controller.

The $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ pins are for receiving the corresponding status bits from the processor. The ALE, DT/$\overline{R}$ and Data Enable (DEN) pins provide the same outputs that are sent by the processor when it is in minimum mode. The CLK input permits the bus controller activity to be synchronized with that of the processor. The Address Enable ($\overline{AEN}$), Input/output Bus (IOB), and Command Enable (CEN) pins are for multiprocessor systems. In a single-processor system $\overline{AEN}$, Input/output Bus(IOB) are normally grounded and a 1 is applied to CEN. The meaning of the Master Cascade Enable/ Peripheral Data Enable (MCE/$\overline{PDEN}$) output depends on the mode, which is determined by the signal applied to IOB. When IOB is grounded it assumes its master cascade enable (MCE) meaning and can be used to control cascaded 8259. As in the event that +5 V is connected to IOB, the peripheral data enable ($\overline{PDEN}$) meaning, which is used in multiple-bus configurations, is assumed.

The remaining pins given in figure 11.8 have the following definitions:

$\overline{INTA}$ - Issues the two interrupt acknowledgment pulses to a priority interrupt controller or an interrupting device when $\overline{S0} = \overline{S1} = \overline{S2} = 0$

$\overline{IORC}$ **(**I/O Read Command**) –** Instructs an I/O interface to put the data contained in the addressed port on the data bus.

$\overline{IOWC}$ **(**I/O Write Command**) –** Instructs an I/O interface to accept the data on the data bus and put the data into the addressed port.

$\overline{MRDC}$ **(**Memory Read Command**) –** Instructs the memory to put the contents of the addressed location on the data bus.

$\overline{MWTC}$ **(**Memory Write Command**) –** Instructs the memory to accept the data on the data bus and put the data into the addressed memory location.

These signals are active low and are output during the middle portion of a bus cycle. Clearly, only one of them will be issued during any given bus cycle.

Self Assessment Questions

4. The _____ pins are to allow the system external to the processor to interrogate the status of the processor instruction queue so that it can determine which instruction it is currently executing.
5. The meaning of the MCE/$\overline{\text{PDEN}}$ output depends on the mode, which is determined by the signal applied to _____.

11.3 System Bus Timing

The length of a bus cycle in an 8086 system is four clock cycles, denoted by T1 through T4, plus an indeterminate number of wait state clock cycles, denoted by Tw. If the bus is to be inactive after the completion of a bus cycle, then the gap between successive cycles is filled with idle state clock cycles represented by T1. Wait states are inserted between T3 and T4 when a memory or I/O interface is not able to respond quickly enough during a transfer. A typical succession of bus cycles is given in figure 11.9.

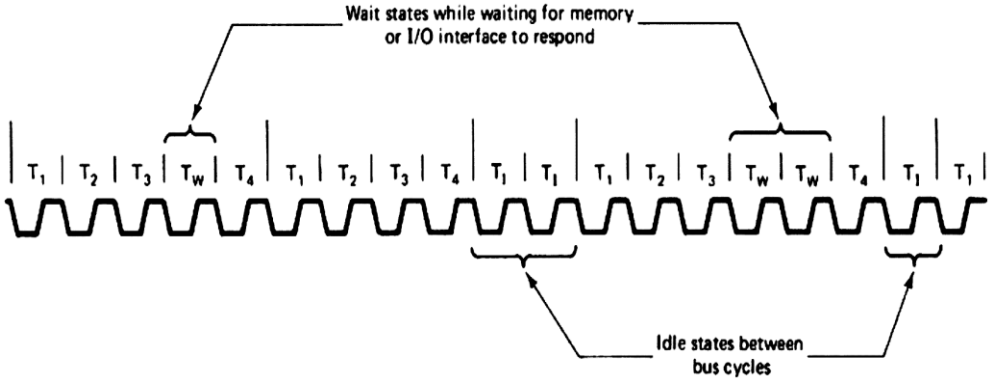
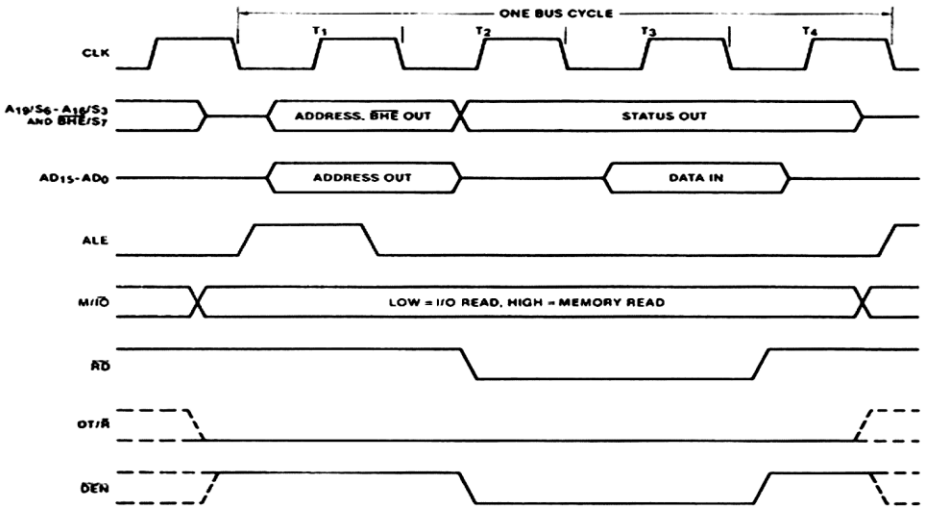


Figure 11.9: Typical sequence of bus cycles

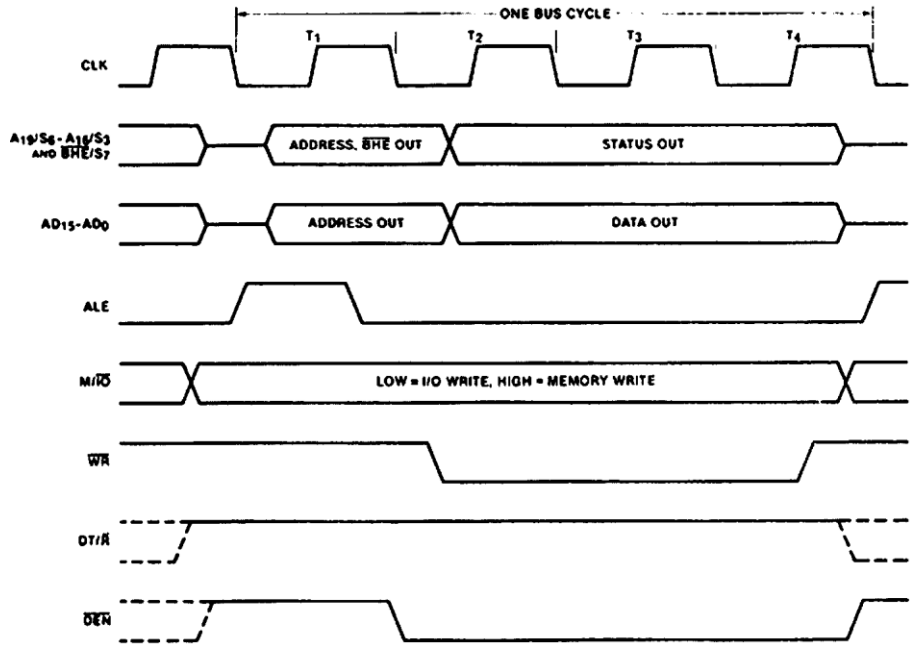
The timing diagrams for 8086 minimum mode input and output transfers that require no wait states are shown in figure 11.10. When the state of the processor is such that it is ready to initiate a bus cycle it applies a pulse to the ALE pin during T1. Before the trailing edge of the ALE signal the address, $\overline{\text{BHE}}$, M/$\overline{\text{IO}}$, $\overline{\text{DEN}}$, and DT/$\overline{\text{R}}$ signals should be stable, with $\overline{\text{DEN}}$ = 1 and DT/$\overline{\text{R}}$ = 0 for an input and DT/$\overline{\text{R}}$ = 1 for an output. At the trailing edge of the ALE signal the 8282s latch the address. During T2 the address is dropped and S3 through S7 are output on AD16/S3-AD19/S6

and $\overline{BHE}$ /S7, and $\overline{DEN}$, is lowered to enable the 8286 transceivers. If an input is being conducted, $\overline{RD}$ is activated low during T2 and AD15-AD0 enter a high-impedance state in preparation for input. If the memory or I/O interface can perform the transfer immediately, there are no wait states and the data are put on the bus during T3. After the input data are accepted by the processor, $\overline{RD}$ is raised to 1 at the beginning of T4 and, upon detecting this transition, the memory or I/O interface will drop its data signals. For an output, the processor applies the $\overline{WR} = 0$ signal and then the data during T2, and in T4 $\overline{WR}$ is raised and the data signals are dropped. For either an input or output, $\overline{DEN}$ is raised during T4 to disable the transceivers and the M/$\overline{IO}$, signal is set according to the next transfer at this time or during a subsequent T1 state.

The timing diagrams for input and output transfers on a maximum mode system are given in figure 11.11. The $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ bits are set just prior to the beginning of the bus cycle. Upon detecting a change from the passive $\overline{S0} = \overline{S1} = \overline{S2} = 1$ state, the 8288 bus controller will output a pulse on its ALE pin and apply the appropriate signal to its DT/$\overline{R}$ pin during T1. In T2, the 8288 will set $\overline{DEN} = 1$, thus enabling the transceivers, and, for an input, will activate either $\overline{MRDC}$ or $\overline{IORC}$. These signals will be maintained until T4. For an output, the $\overline{AMWC}$ or $\overline{AIOWC}$ is activated from T2 to T4 and the $\overline{MWTC}$ or $\overline{IOWC}$ is activated from T3 to T4. The status bits $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ will remain active until T3 and will become passive (all 1s) during T3 and T4. As with the minimum mode, if the READY input is not activated before the beginning of T3, wait states will be inserted between T3 and T4.

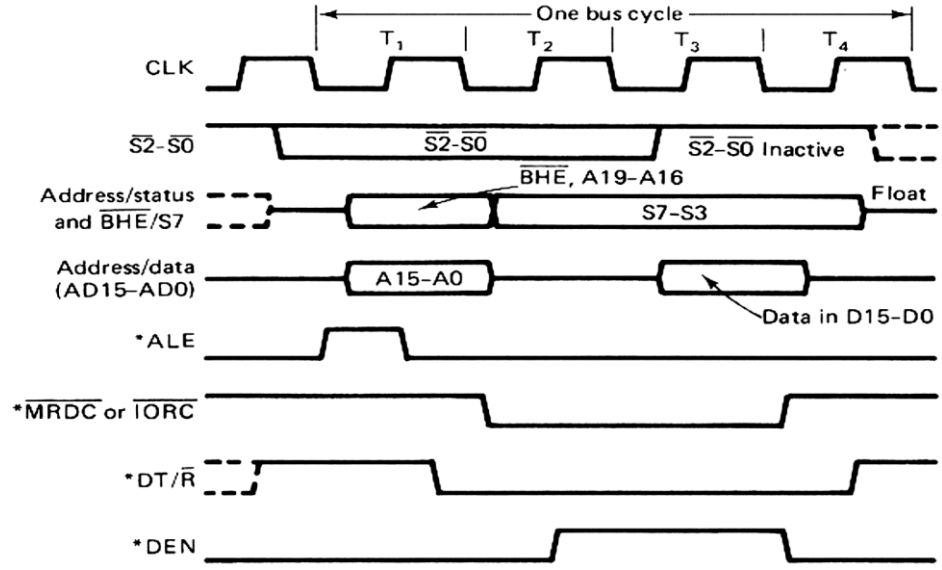


(a) Input

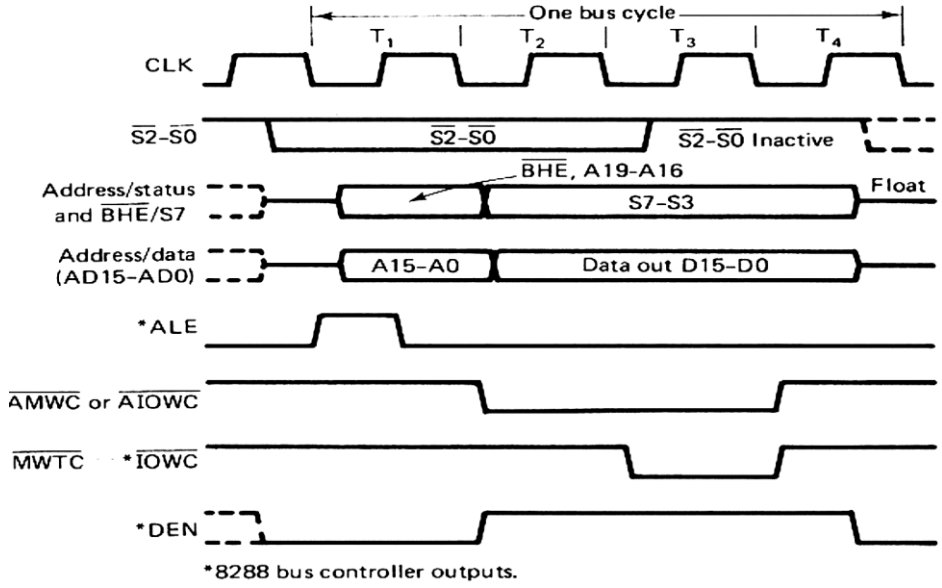


(b) Output

Figure 11.10: 8086 minimum mode bus timing diagrams



(a) Input



(b) Output

Figure 11.11: Timing diagrams for maximum mode system

Self Assessment Questions

6. If the bus is to be inactive after the completion of a bus cycle, then the gap between successive cycles is filled with idle state clock cycles represented by T1. (True/False)
7. Wait states are inserted between _____ when a memory or I/O interface is not able to respond quickly enough during a transfer.
8. If an input is being conducted, $\overline{RD}$ is activated low during T2 and AD15-AD0 enter a _____ state in preparation for input.

11.4 Bus Interface

A bus is a set of conductors used for communications between the components in a computer system. A bus can be an internal bus or an external bus. If a bus connects two minor components within a major component (e.g., the control unit to the set of working registers within the CPU), it is called an ***internal bus***. When a bus connects two major components, such as a CPU and an interface, it is called an ***external bus***. Many applications require some knowledge about the bus systems located within the personal computer (PC). In this section you will be introduced to the peripheral component interconnect (PCI) bus, the parallel printer interface (LPT) and universal serial bus (USB).

Peripheral Component Interface (PCI)

The Peripheral Component Interface (PCI) bus was introduced by Intel Corporation in July 1992. It was designed primarily for high speed operation of the expansion bus. PCI is the most popular 'bus' in the mid-1990s and is usually combined on a motherboard with an ISA or EISA expansion bus. For example, many motherboards have a number of pure Industry Standard Architecture (ISA) or Extended Industry Standard Architecture (EISA) slots, some PCI slots, and one or more PCI/ISA combination slots. PCI is a 32-bit bus that normally runs at a maximum of 33 MHz yielding a maximum data transfer rate of 132Mbytes per second. The PCI bus is part of the Plug and Play. The PCI standard provides an interface to the ISA, EISA, and Micro Channel Architecture (MCA) buses, but PCI can replace these older buses in a motherboard design. A pure PCI bus machine is possible, but most motherboards for years will still have an interface to ISA and EISA expansion slots. Remember: Most motherboards have both PCI and ISA, or PCI and EISA, or even PCI and MCA slots. The PCI I/O controller will route

traffic from the CPU to the proper bus - either the PCI bus or the ISA/EISA bus. The PCI bus was introduced with the Pentium computer. The 16-bit and 32-bit bus architecture would limit the performance of the 64-bit Pentiums. The PCI bus supports both 32 and 64-bit data paths and uses a chipset that will also support ISA and EISA architectures. This means that the PCI bus can be used for both 486 computers and Pentiums, and motherboards can have a combination of PCI and ISA or EISA slots.

The PCI bus communicates with the processor through a bridge circuit, which acts like an interpreter. This means that it can be processor independent. It can work with CISC or RISC technologies as long as it has the proper bridge circuit to interpret the information. PCI bus is designed to variety of processors based on configurations including both single and multiprocessor systems.

The standard describes the way that the system components are electrically connected and the way that they should behave. Figure 11.12 is a logical diagram of an example of PCI based system.

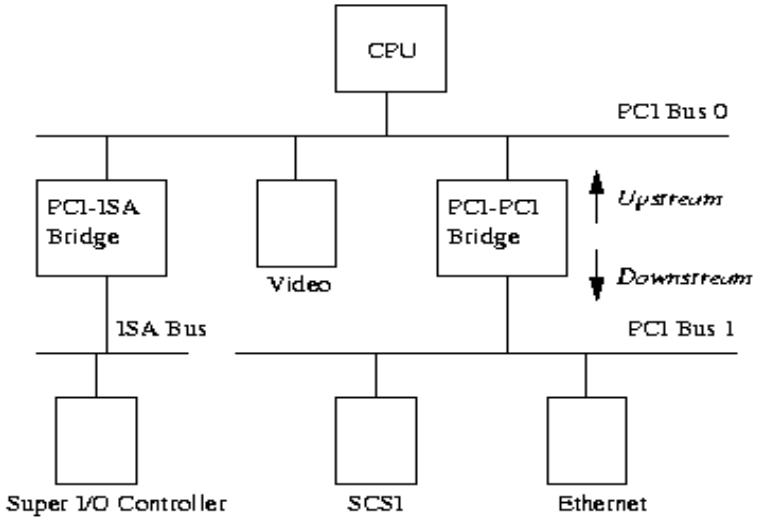


Figure 11.12: Example of PCI Based System

The PCI buses and PCI-PCI bridges are the glue connecting the system components together; the CPU is connected to PCI bus 0, the primary PCI bus as is the video device. A special PCI device, a PCI-PCI bridge connects

the primary bus to the secondary PCI bus, PCI bus 1. In the jargon of the PCI specification, PCI bus 1 is described as being downstream of the PCI-PCI bridge and PCI bus 0 is up-stream of the bridge. Connected to the secondary PCI bus are the SCSI and ethernet devices for the system. Physically the bridge, secondary PCI bus and two devices would all be contained on the same combination PCI card. The PCI-ISA bridge in the system supports older, legacy ISA devices and the diagram shows a super I/O controller chip, which controls the keyboard, mouse and floppy.

Parallel Printer Interface (LPT)

The parallel printer interface (LPT) is located on the rear panel of the PC. The LPT stands for line printer. The Parallel Port Interface on the PC compatible computer is one of the most flexible interfaces for connecting the PC to a wide range of devices. The interface was originally intended purely for connection to printers but due to the simple nature of the digital control lines it has found many other uses. Its simplicity relies on the fact that the data to and from the port forms an 8 bit binary on/off pattern. Unlike serial ports which rely on a chip to do the data transmission, parallel data is handled entirely with software. This means that, user has complete control of the actual on/off condition of the output lines directly from his/her program. This control is achieved by writing data to specific areas of PC I/O memory. Parallel ports have three registers: one for data out, one for output control lines and one for input control lines. The PC standard starts the I/O ports for the first parallel interface at 0x378, and for the second at 0x278. The first port is a bidirectional data register; it connects directly to pins 2 through 9 on the physical connector. The second port is a read-only status register; when the parallel port is being used for a printer, this register reports several aspects of printer status, such as being online, out of paper, or busy. The third port is an output-only control register, which, among other things, controls whether interrupts are enabled.

Universal Serial Bus (USB)

The two main problems associated with peripherals connected to computer systems today are "plug and play" and speed of data transfer. USB (Universal Serial Bus) is designed to overcome these problems. Each USB port provides a single connector for any device that previously used parallel, serial, keyboard, and mouse or game ports. USB provides a serial bus standard for connecting peripherals devices to PC with simplified addition

and removal. USB can connect peripherals such as mice, keyboards, game pads and joysticks, scanners, digital cameras, printers, external storage, networking components, etc. The design of USB is standardized by the USB Implementers Forum (USB-IF), an industry standards body incorporating leading companies from the computer and electronics industries. The figure 11.13 shows the typical Universal Serial Bus (USB).

Figure 11.13: Universal Serial Bus (USB)

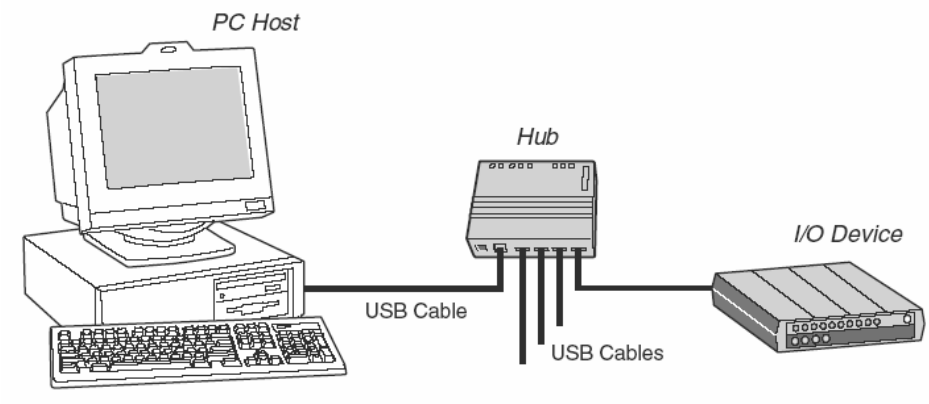
The Universal Serial Bus (USB) standard was originally developed in 1995, to minimize the number of ports in the back of the PC. Universal Serial Bus (USB) is a standard used for connecting devices such as computers, set-top boxes, game consoles, Personal Digital Assistants (PDAs) and peripherals among other devices. There are various versions of USB specificationUSB1.0, USB1.1, USB2.0 and USB On-the-Go (OTG). The major goal of USB was to define an external expansion bus which makes adding peripherals to a PC at low cost and as easy as hooking up a telephone to a wall-jack. USB featured a maximum bandwidth of 1.5Mbit for low speed devices such as mice and keyboards, and a maximum bandwidth of 12Mbit for higher speed devices such as web cams, printers, scanners and external CD-RW drives. Frustrated by Apples royalty fees on firewire devices, in April 2000, seven industry-leading companies, consisting of Compaq, Hewlett Packard, Intel, Lucent, Microsoft, NEC, and Philips published the specifications for USB2.0. It has taken approximately 2 years for USB 2.0 to become adopted as a mainstream USB1.1 replacement. In

just a few short months USB 2.0 will be the high speed PC peripheral connectivity choice over IEEE-1394.

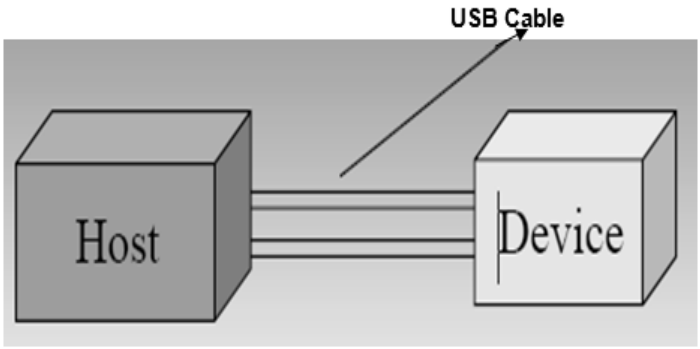
The general features of USB are:

- supports plug and play
- supports connection and disconnection of devices live (when turned on)
- multiple device connection via "hub"
- each USB device has a unique address
- maximum signal distance of 16 feet (five meters)
- Simplifies the connection process and enables instantaneous addition and removals of peripherals
- PC acts as host. Once plugged PC automatically detects peripherals and configures them.
- Connects peripherals with 4 wire connection.
- Supports 3 data rates 480 Mbps (USB 2)(high Speed) 12 Mbps (full speed) and 1.5 Mbps(low speed)used to connect human interface devices such as mouse, keyboard etc.
- Many peripherals can be connected to one port using a special peripheral device called USB hub through which one can go upto 127 devices using single port.
- Peripherals share available bandwidth through token based protocol.
- Distributes power to many low power peripherals. Uses single interrupt line.
- Replaces serial and parallel port.
- Windows 98, 2000 and XP supports USB.
- Individual devices can run up to 5 meters and with hub they can go up to 30 meters.
- PC controls the peripherals.
- No user settings
- Low cost.
- Simple cables
- Low power consumption
- flexibility

USB System: The figure 11.14 shows the examples of USB systems.



(a)



(b)

Figure 11.14: Examples of USB Systems

USB system consist of three units

1) USB host
2) USB Cable and
3) USB Device.

USB Host detects the attachment and removal of USB devices. It installs the device when pluged in, Manages flow of control information between host and USB devices, Manages flow of data, Collects activity and status information of devices and Provides power to low power devices. USB cables are designed to ensure correct connections. By having different connectors on host and device, you can connect two hosts or two devices

together. USB Device monitors device address in each communication and selects itself. It responds to all requests made by the host, adds bits for checking errors for the data being sent by the device. If the USB device is self powered, it manages its own power supply. USB uses two lines for differential data connections (designated D+ and D–) and also two lines for supplying power to the cable – one is VBUS (nominal value +5V) and the other customary GND wire.

There are two types of USB connectors – Series A and Series B or Type A and Type B. 'A' Type connectors are used in USB devices while 'B' type connectors are meant for device vendors in order to provide a standard detachable cable. 'Keyed connector' protocol is used by USB. Figure 11.15 shows a typical type 'A' connector, showing the standard USB icon and a top locator on the cable end side of the connector.

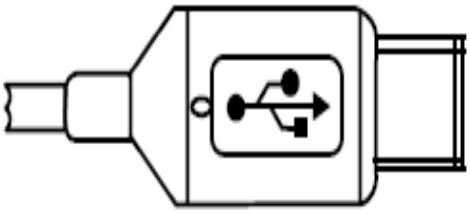


Figure 11.15: USB cable connector

Figure 11.16 and figure 11.17 show respectively Type A and Type B connectors and table 11.1 shows the signals corresponding to the pins and the recommended color coding also.

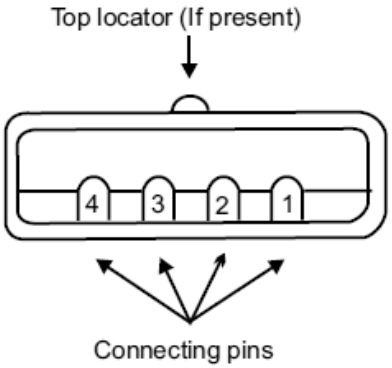


Figure 11.16: USB connector (type A)

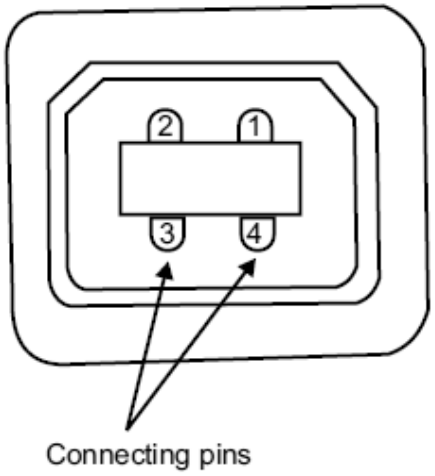


Figure 11.17: USB connector (type B)

Table 11.1: USB pin connections)

Pin number	Signal	Recommended colour
1	V_{BUS}	Red
2	D–	White
3	D+	Green
4	GND	Black
Shell	Shield	Drain Wire

Full speed devices use B type connector allowing the device to use detachable USB cable. Thus devices can be built without hardwired cable and cable replacement becomes very easy if the need so arises.

USB 2.0

The initial specification, Rev 0.9 was released in December 1999. It sets the speed of USB 2.0 at 480Mb/s (megabits per second), 40 times faster than USB 1.1. This high data transfer speed will allow USB 2.0 to connect to peripherals such as video conferencing cameras and high-speed printers. For example, downloading a 40MB photo will be reduced from around

6 minutes on USB 1.1 to a few seconds on USB 2.0. This reduces the need for using a high speed interface such as Small Computer System Interface (SCSI). USB 2.0 will users to connect multiple high-speed devices simultaneously and retains all the existing benefits of USB 1.1, including plug-and-play, dynamic attach and detach, power distribution to devices, and support for power management. The new specification is backward compatible with USB 1.1. Existing USB 1.1 devices, cables and connected are supported.

Self Assessment Questions

9. When a bus connects two major components, such as a CPU and an interface, it is called a _____.
10. PCI stands for _____.
11. The parallel printer interface (LPT) is located on the front panel of the PC. (True/False).
12. _____is a standard used for connecting devices such as computers, set-top boxes, game consoles, PDAs and peripherals among other devices.

11.5 Summary

In this unit we got to know the types of 8086 configurations and also we studied the concept of bus interface. Let us recap the important points discussed in the unit:

- The minimum mode is used for a small system with a single processor, a system in which the 8086 generates all the necessary bus control signals directly.
- The Maximum mode is for medium-size to large systems, which often include two or more processors.
- The length of a bus cycle in an 8086 system is four clock cycles, denoted T1 through T4, plus an indeterminate number of wait state clock cycles, denoted Tw.
- If a bus connects two minor components within a major component (e.g., the control unit to the set of working registers within the CPU), it is called an *internal bus.*
- PCI is a 32-bit bus that normally runs at a maximum of 33 MHz yielding a maximum data transfer rate of 132Mbytes per second.

- The Parallel Port Interface on the PC compatible computer is one of the most flexible interfaces for connecting the PC to a wide range of devices.
- Universal Serial Bus (USB) is a standard used for connecting devices such as computers, set-top boxes, game consoles, PDAs and peripherals among other devices.

11.6 Terminal Questions

1. Discuss on important configurations of 8086 microprocessor.
2. Explain the operation of 8086 in minimum mode configuration.
3. Explain the operation of 8086 in maximum mode configuration.
4. Discuss on 8086 system bus timing.
5. Write a note on parallel printer interface(LPT)

11.7 Answers

Self Assessment Questions

1. MN/$\overline{MX}$
2. 8286
3. 8284
4. QS0 and QS1
5. IOB
6. True
7. T3 and T4
8. high-impedance
9. External bus
10. Peripheral Component Interface
11. False
12. Universal Serial Bus (USB)

Terminal Questions

1. In order to adapt to as many situations as possible, the 8086 has been given two modes of operation, the minimum mode and the maximum mode. Refer to section 11.2 for details.
2. A processor 8086 will be in minimum mode when its MN / $\overline{MX}$ pin is strapped to +5 V. Refer to sub-section 11.2.1 for more details.

3. A processor is in maximum mode when its MN/$\overline{MX}$ pin is grounded. The main difference between minimum and maximum mode configurations is the need for additional circuitry to translate the control signals. Refer to sub- section 11.2.2 for details.
4. The length of a bus cycle in an 8086 system is four clock cycles, denoted T1 through T4, plus an indeterminate number of wait state clock cycles, denoted Tw. Refer to section 11.3 for details.
5. The parallel printer interface (LPT) is located on the rear panel of the PC. The LPT stands for line printer. Refer to section 11.4 for details.