EE709 Testing and Verification

Unit18 VCO PLL Magic Task (Due Date - 26 March 2022)

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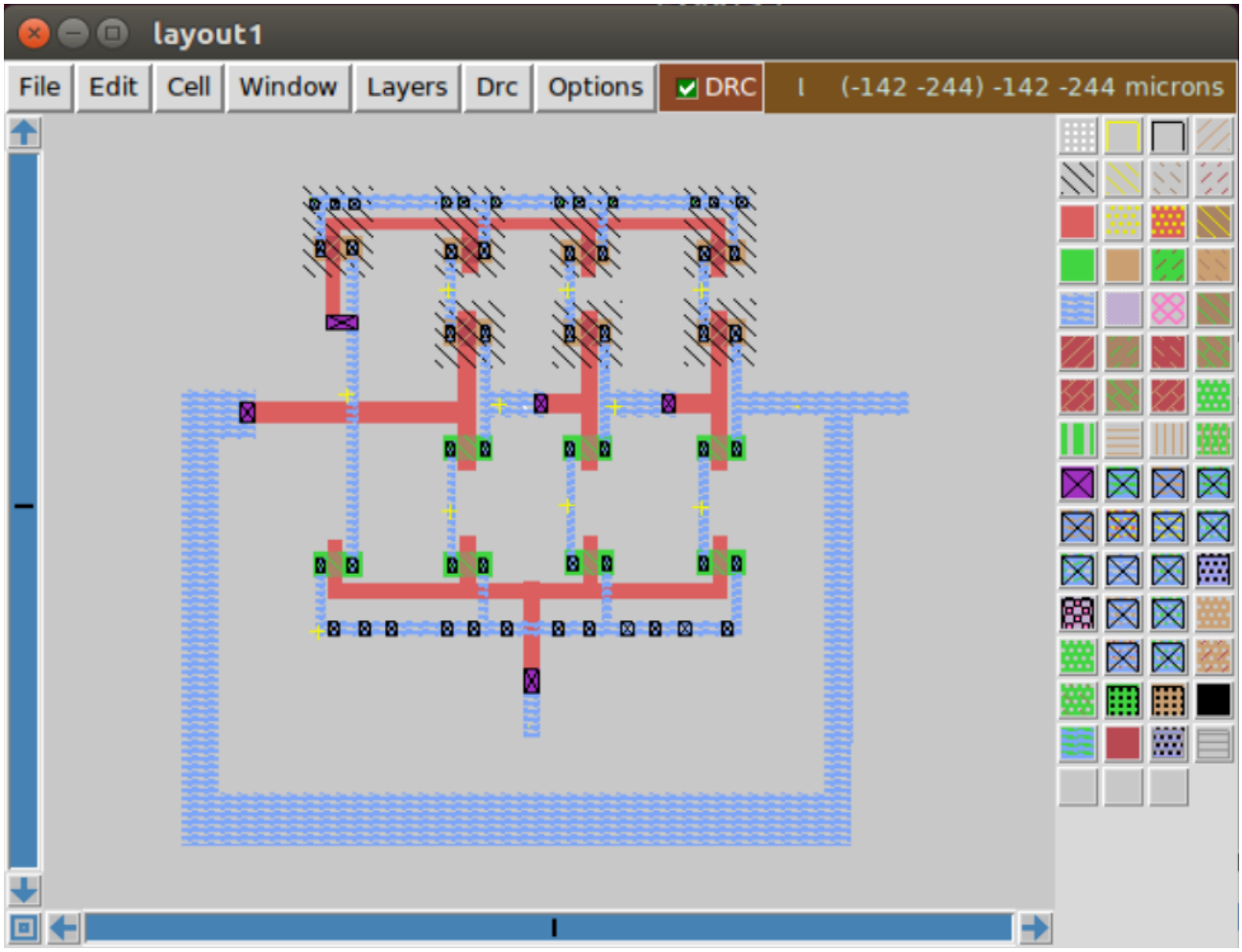
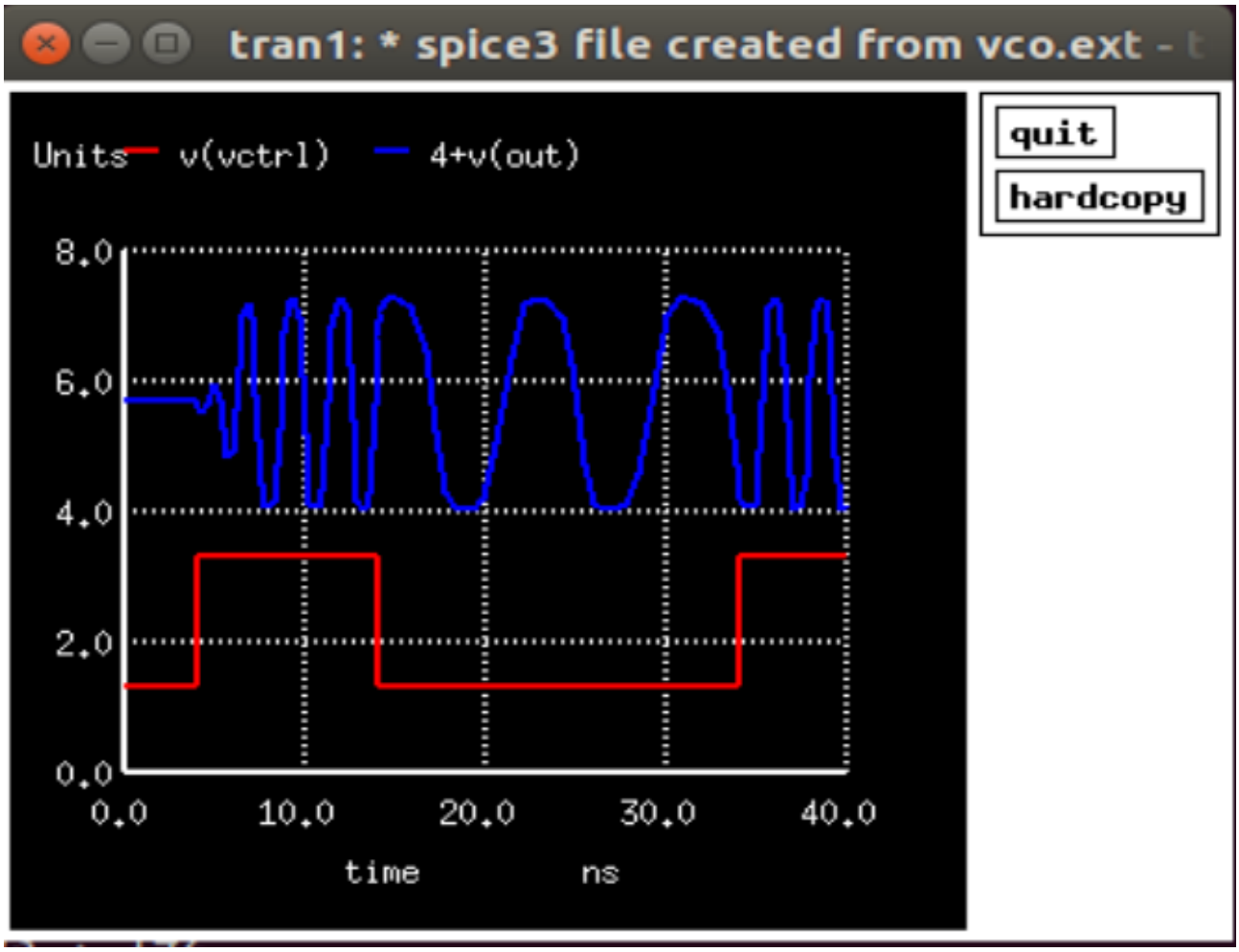
Problem 1 Design a layout of a voltage controlled oscillator (VCO) circuits also do post layout simulation using ngspice tool and verify the functioning of VCO circuit

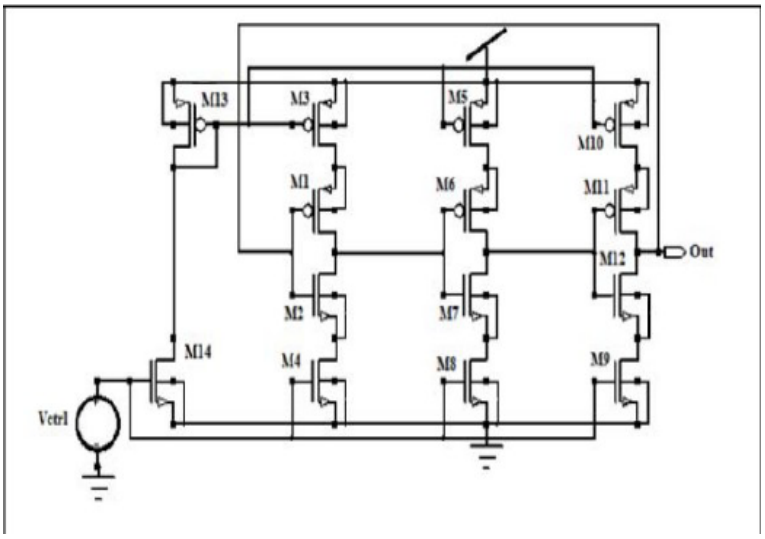
Solution The snippet of the designed layout is given below-



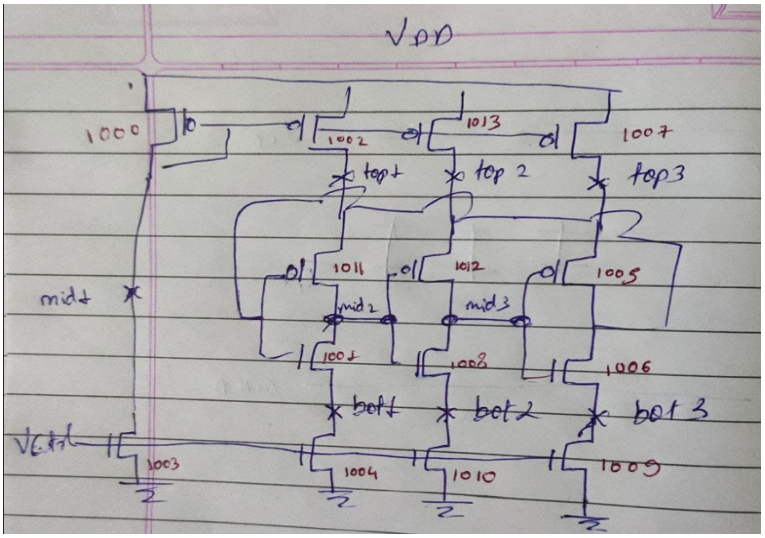
The snippet of the waveform is given below-



The snippet of the circuit-



The snippet of the rough diagram for understanding and debugging-

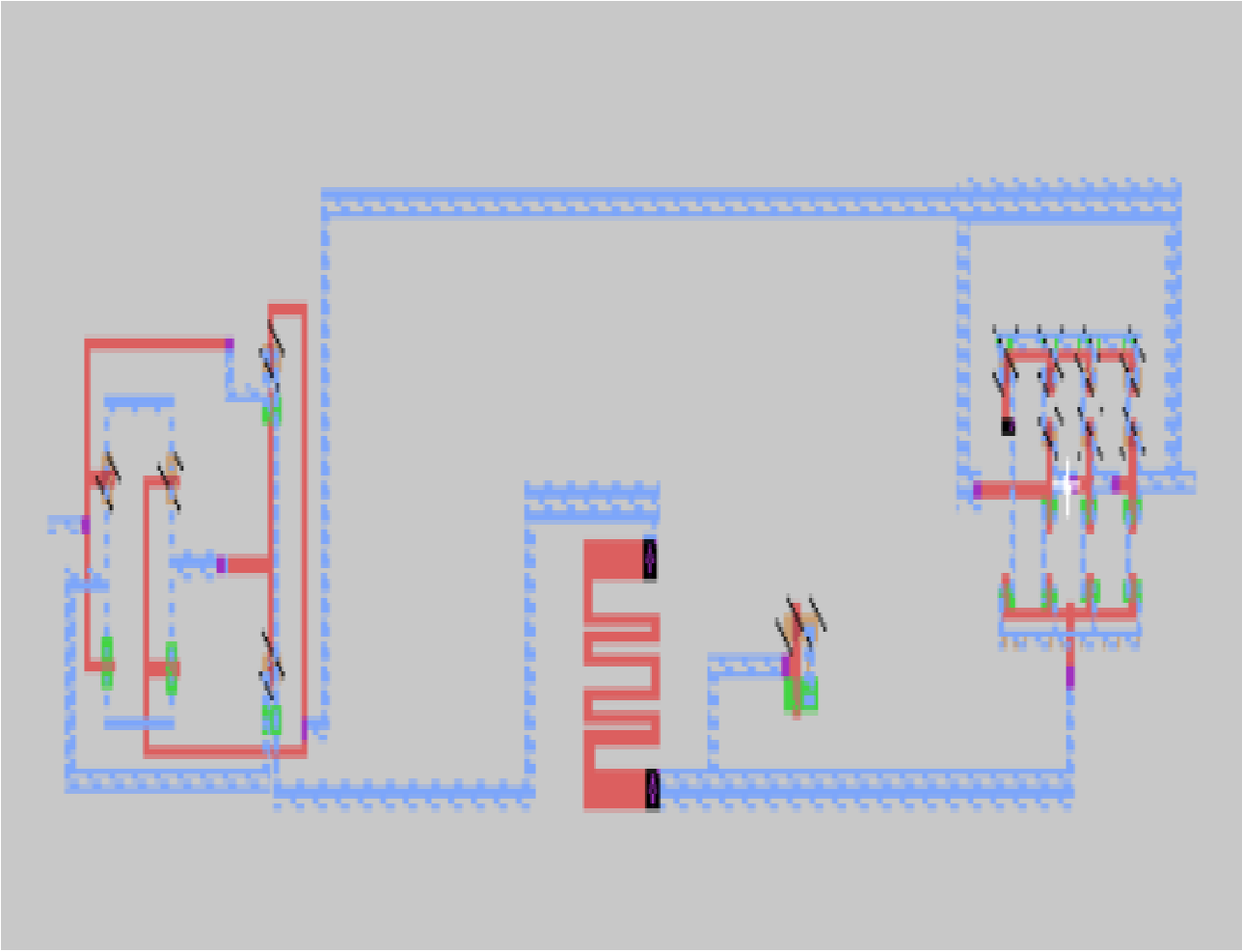


Analysis:-

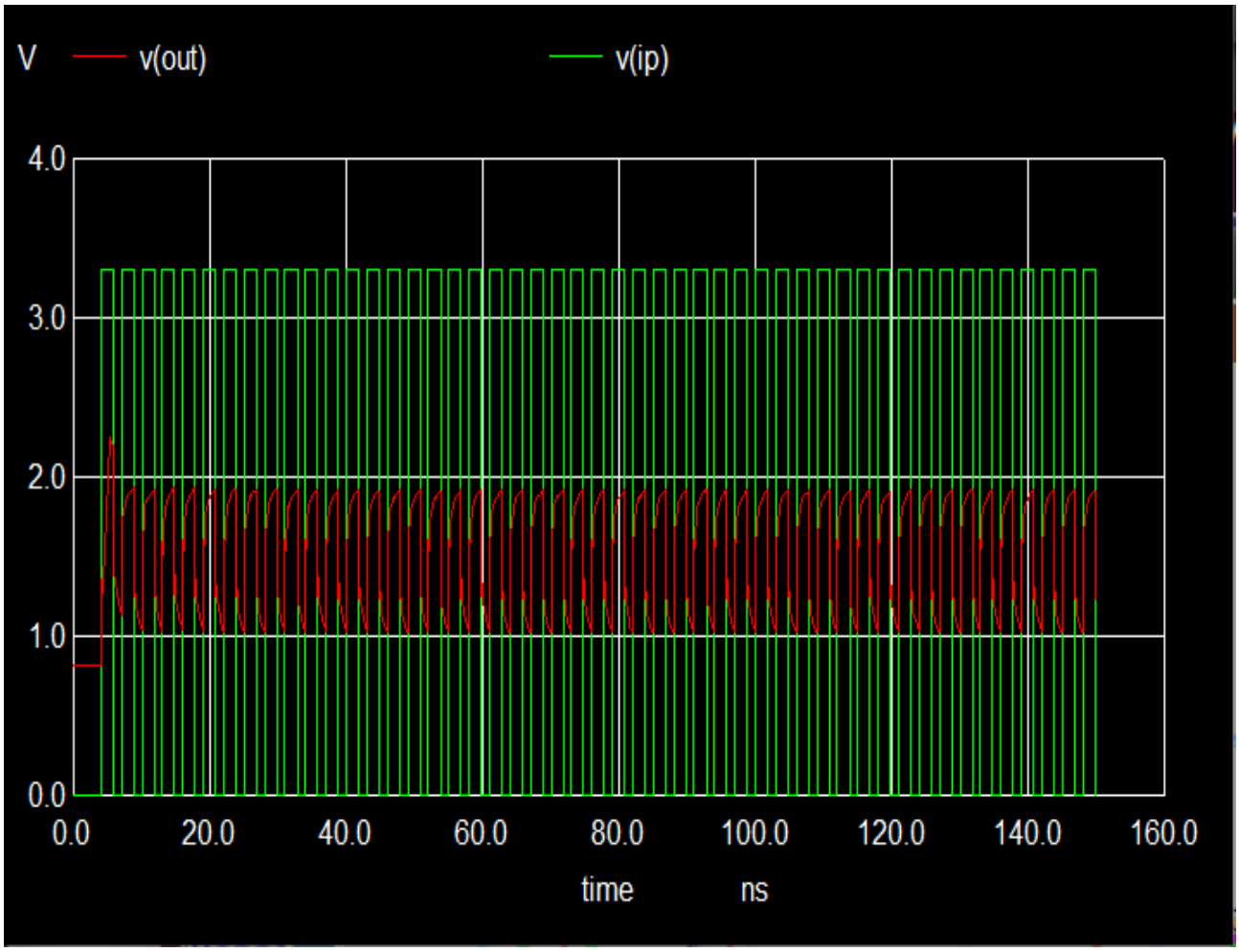
Firstly we need to draw stick diagram of the given circuit then we can start implementing in MAGIC. Here in Magic we need to keep a check for all DRC rules as they are very fundamental in nature. Once the layout is done then we need to convert into .spice file from .mag file. Here .spice file is for post layout simulation in NGSpice. We need to type "extract.all" and "ext2spice" command in MAGIC Terminal and the conversion will be over. Next step is to modify the length and Width of PMOS and NMOS as there might be in some mismatch in technology file used in MAGIC and NGSpice. So we need to make sure we modify .spice file according to our new model file. Once done we can do the analysis according to our own will. One such analysis is done in above picture.

Problem 2 Design the PLL(phase locked loop) circuit using the designed VCO circuits.

Solution The snippet of the designed layout is given below-



The snippet of the waveform is given below-



The snippet of the circuit-