COL216 Computer Architecture
Notes on Lab Assignment 5
Modules of the controller

This note gives a brief description of various modules that constitute the controller for multi-cycle processor design of Lab assignment 5 (reference Lectures 12 and 13).

Instruction decoder (combinational)

It looks at the relevant instruction bits and determines the class, such as (DP | DT | MUL | B), sub-class such as (arith | logic | test) or (ldr | str | ldrh | strh | ldrb | strb | ldrsh | ldrsb), and variant, such as (imm | reg_imm | reg_reg) for the current instruction. It also indicates whether the instruction is implemented or unimplemented or undefined.

The decoder needs to look at bits 27-20 and 11-4 of the instruction.

Flag check unit or Bctrl unit (combinational)

It looks the four flags (V, C, Z, N) to determine if the condition specified by the instruction bits 31-28 is true or not. Note that if the condition field is "1111", the instruction is undefined.

Main controller (sequential)

This module may be divided into two parts in order to keep each part simpler.

(i) Controller FSM (sequential)
This part includes control state register and the next state logic. A wide range of choices exists in defining the states. One extreme is to define enough states so the all control signals can be derived only from the control state in Moore style. The other extreme is to have only *m* states where *m* is the maximum number of cycles any instruction takes. Inputs to Controller FSM are those decoder outputs that influence state transitions. Output of the Controller FSM is the control state.

(ii) Control signal generator (combinational)
Outputs of this module are the control signals. The inputs are control state and some decoder outputs. Depending upon how states are defined, this module may need to look at all the decoder outputs in one extreme scenario and may not look at any decoder output in the other extreme scenario. Some of the control signals need to be ANDed with Bctrl output and the signal enabling flag setting needs to be further ANDed with S bit of instruction.

ALU control or Actrl (combinational)

This is adequately described by slides 4 and 5 of Lecture 13.