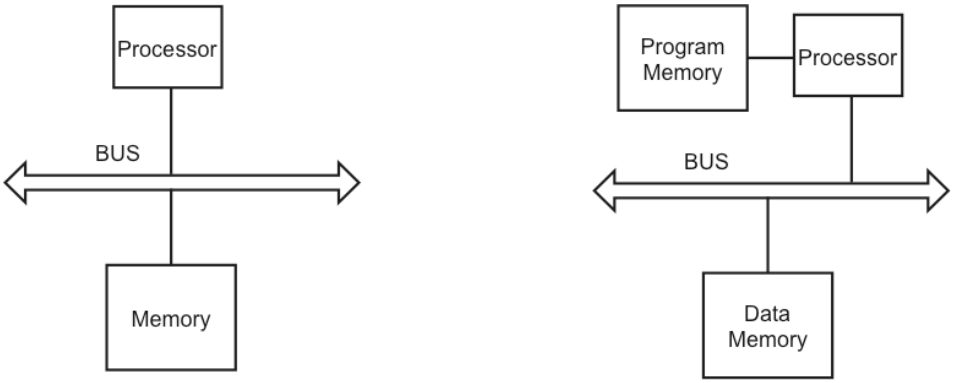
COL216 Computer Architecture

Lab Assignment 6
Part 1 (for week 10)

In the design of the assignment 5, introduce AHB-Lite bus to connect the processor (as the master) with the memory (as a slave). Any of the two configurations shown in the figure below may be used.



Use the following parameters/restrictions.

- Data width = 32 bits (4 bytes)
- Address = 16 bits
- Transfer Size = byte | half-word | word (HSIZE[2:0] = “000” | “001” | “010”)
- Burst Size = Single (HBURST[2:0] = “000”)
- Locked transfers Not used Ignore HMASTLOCK
- Protection control Not used Ignore HPROT[3:0]

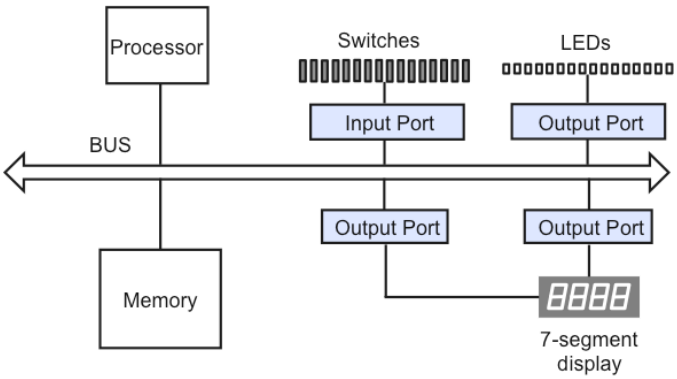
Artificially slow down the memory by introducing 3 wait cycles in every read/write transfer. In part 1, AHB-Lite bus is used only to connect the processor and the memory. In part 2, extend the bus to input/output ports as slaves.

Lab Assignment 6
Part 2 (for week 11)

This part involves adding the following input/output ports.

- a 16-bit input port for slide switches
- a 16-bit output port for LED display
- a 4-bit output port for anodes of 7-segment display
- an 8-bit output port for cathodes of 7-segment display

The enhanced system is shown in the figure below.



Here the 7-segment display is to driven completely by software. Assign suitable addresses to various ports. To test this system, write a program that takes a 16-bit binary number from the slide switches, displays it in binary on LEDs and its decimal equivalent on the 7-segment display,