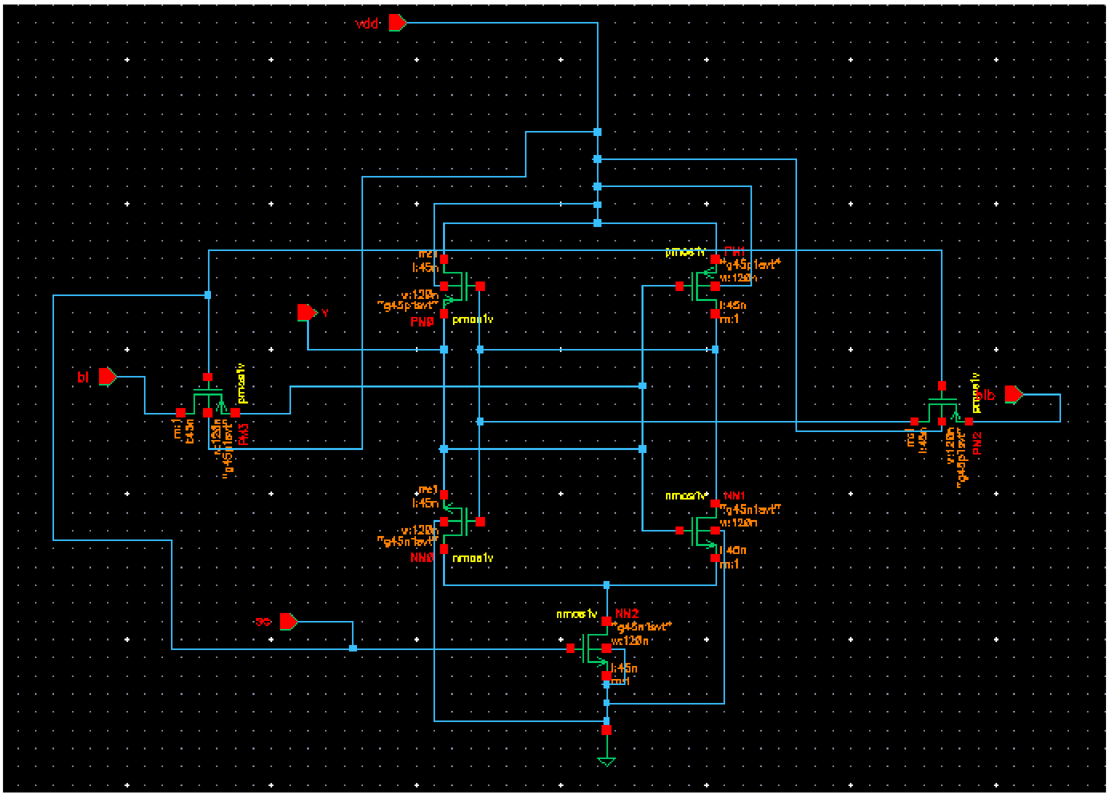
SENSE AMPLIFIER

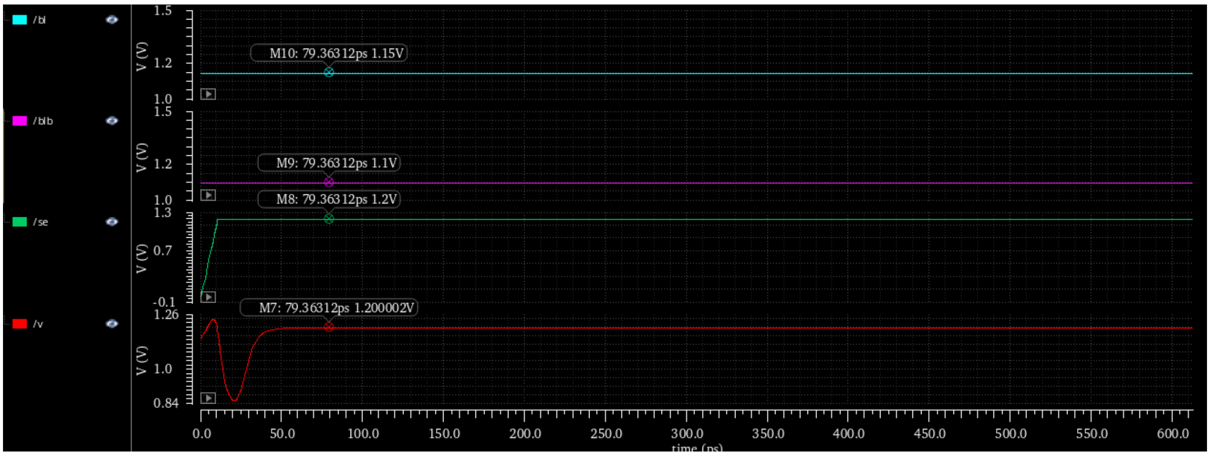
➢ <u>Schematic</u>



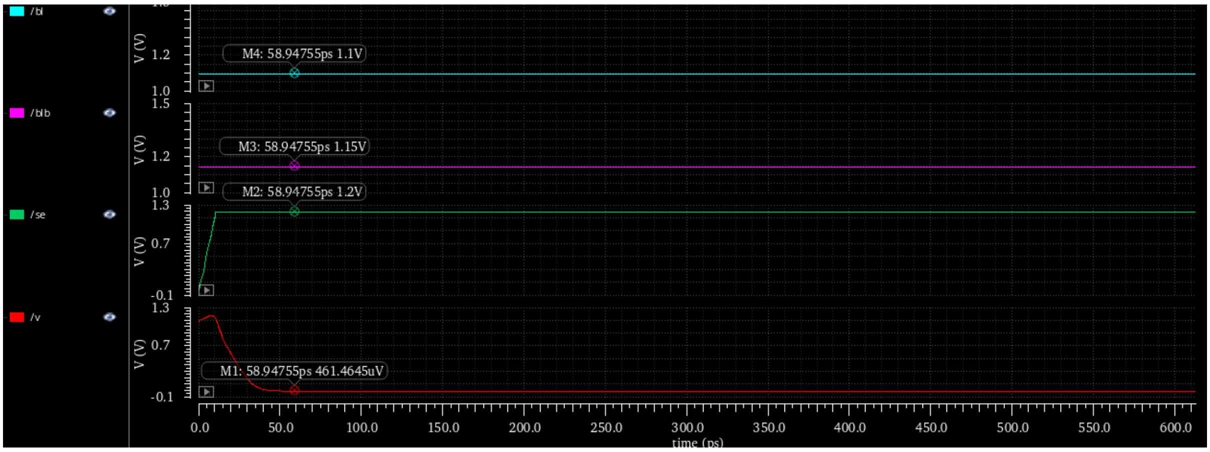
➢ <u>Test Cases</u>

Test Case	BL	BLB	SE	EXPECTED OUTCOME
1	1.15V	1.1V	HIGH	HIGH(1)
2	1.1V	1.15V	HIGH	LOW(0)
3	1.3V	0.7V	HIGH	HIGH(1)
4	0.7V	1.3V	HIGH	LOW(0)
5	Any	Any	Low	Undefined/Zero

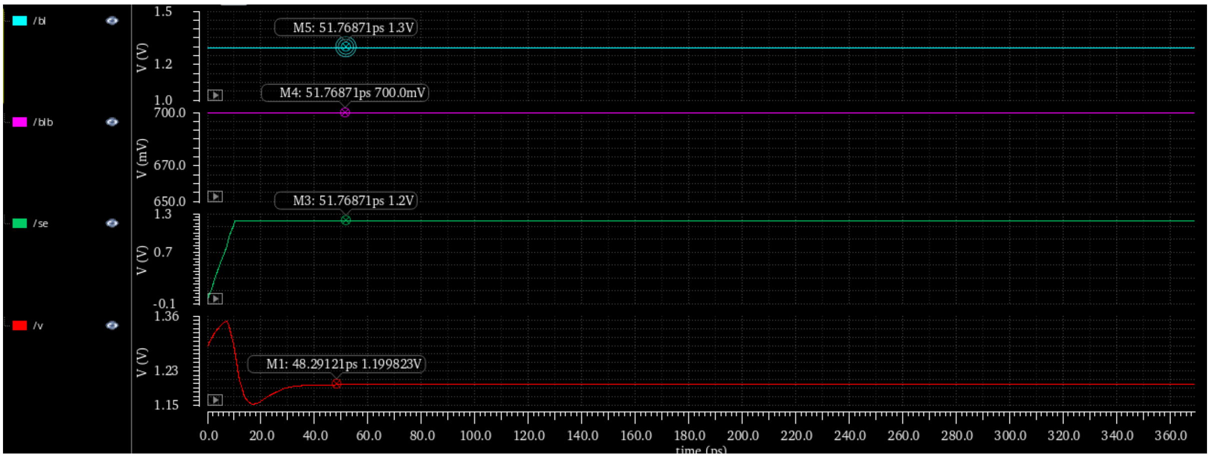
➢ Waveforms



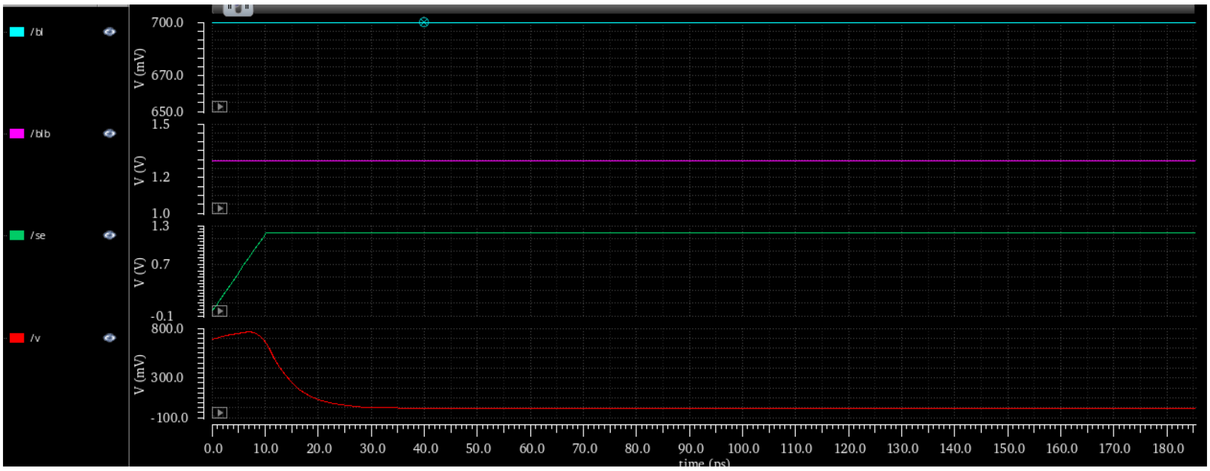
CASE 1



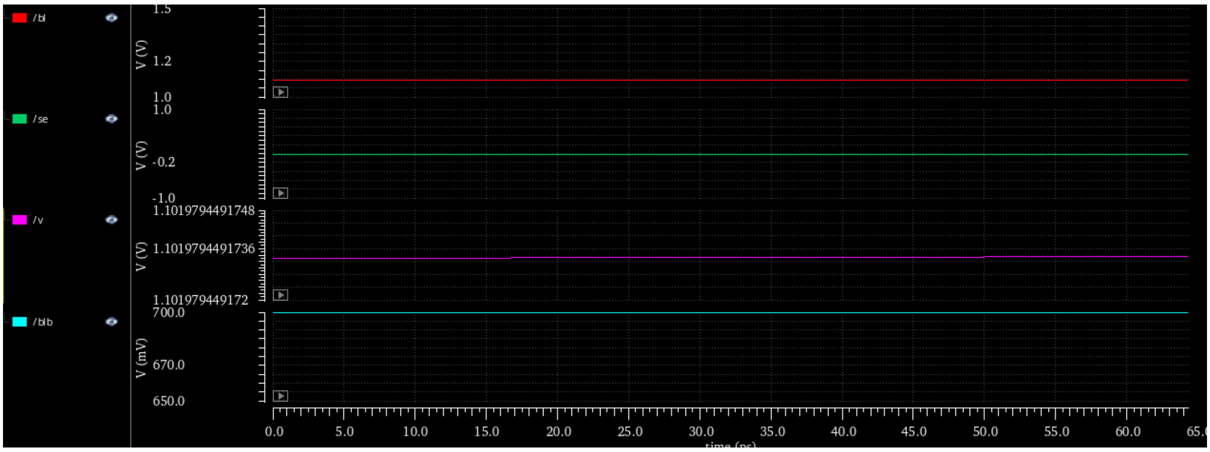
CASE 2



CASE 3



CASE 4



CASE 5

➢ Theory and Operation :

❖ What is a Sense Amplifier?

A sense amplifier is a specialized circuit used in memory devices like SRAM (Static Random Access Memory) to read the stored data. It detects and amplifies the small voltage differences on the bit lines (BL and BLB) caused by the stored data in the memory cells. The amplified signal is then used to determine whether the stored bit is a '0' or a '1'.

❖ Why is a Sense Amplifier Required?

1. Small Voltage Differences:
    - SRAM cells produce very small voltage differences on the bit lines during a read operation. These differences are often too small to be reliably detected directly by subsequent digital logic circuits.

2. Speed:
    - Sense amplifiers speed up the read operation by quickly amplifying the small voltage difference, allowing the memory system to operate at higher speeds.

3. Power Efficiency:
    - By amplifying small signals early, sense amplifiers help reduce the overall power consumption in the memory read path.

4. Signal Integrity:
    - Amplifying the signal helps in maintaining the integrity of the data, reducing the chances of errors during read operations.

❖ How Does the Sense Amplifier Work in Our Circuit?

The sense amplifier in our SRAM circuit consists of a combination of PMOS and NMOS transistors configured to detect and amplify the small voltage difference between the bit lines (BL and BLB). Here's a detailed step-by-step explanation of its operation:

1. Initial Setup:

   Precharge Phase:
    - Before a read operation, both BL and BLB are precharged to a midpoint voltage (typically VDD/2), equalizing their voltage levels.

2. Read Operation Initiation:

- When an SRAM cell is accessed, it creates a small voltage difference between BL and BLB. For example:
- If the stored bit is '1', BL might remain at VDD/2, and BLB might drop slightly below VDD/2.
- If the stored bit is '0', BL might drop slightly below VDD/2, and BLB might remain at VDD/2.

3. Sense Amplifier Enable (SE = 1):

Transistor Activation:

- When SE (Sense Enable) is high, it activates PM2, PM3, and NM2.
- PM2 and PM3: These transistors connect the bit lines (BL and BLB) to the gates of PM0/NM0 and PM1/NM1, respectively.
- NM2: Provides a path to ground for NM0 and NM1, enabling current flow through these transistors.

4. Voltage Difference Detection:

- Assume BL > BLB (small positive voltage difference):
- PM3 Conducts: Connecting BL to the gates of PM1 and NM1, raising their voltages.
- PM2 Conducts: Connecting BLB to the gates of PM0 and NM0, lowering their voltages.

5. Transistor Responses:

- NM1 Gate Voltage: Increased by BL, NM1 turns on more strongly, pulling its drain (node connecting NM0 and NM1) lower.
- NM0 Gate Voltage: Decreased by BLB, NM0 conducts less current.
- PM1: With a lower gate voltage (from NM1's action), PM1 turns on more strongly, pulling the output node high.
- PM0: With a higher gate voltage (from NM0's action), PM0 conducts less, contributing less to pulling the output node low.

6. Amplification and Output:

- The combined effect of PM0 conducting less and PM1 conducting more results in the output node (V) being pulled high. This amplified output reflects the small initial voltage difference between BL and BLB, representing the stored data.

➢ Case Study :

1) Case 1: Small Positive Differential (BL > BLB)

❖ **Inputs:**

- **BL = 1.15V**
- **BLB = 1.1V**
- **SE = 1.2V**

❖ **Explanation:**

- In this scenario, BL is slightly higher than BLB by a small differential voltage ($\Delta V = 50mV$).
- With SE high, the sense amplifier is enabled and detects the small positive difference.
- The sense amplifier amplifies this small difference, resulting in a high output (logic '1').

❖ **Expected Output:**

- High (logic '1'), as BL is greater than BLB.

2) Case 2: Small Negative Differential (BL < BLB)

❖ **Inputs:**

- **BL = 1.1V**
- **BLB = 1.15V**
- **SE = 1.2V**

❖ **Explanation:**

- In this scenario, BL is slightly lower than BLB by a small differential voltage ($\Delta V = 50mV$).
- The sense amplifier, with SE high, detects the small negative difference.

- The sense amplifier amplifies this small difference, resulting in a low output (logic '0').

❖ **Expected Output:**

- Low (logic '0'), as BL is less than BLB.

3) Case 3: Large Positive Differential (BL >> BLB)

❖ **Inputs:**

- **BL = 1.3V**
- **BLB = 0.7V**
- **SE = 1.1V**

❖ **Explanation:**

- In this case, BL is significantly higher than BLB by a larger differential voltage ($\Delta V = 200mV$).
- The sense enable signal (SE) is high, so the sense amplifier is active.
- The large positive difference between BL and BLB is detected and amplified quickly and strongly, producing a high output (logic '1').

❖ **Expected Output:**

- High (logic '1'), as BL is much greater than BLB.

4)Case 4: Large Negative Differential (BL << BLB)

❖ **Inputs:**

- **BL = 0.7V**
- **BLB = 1.3V**
- **SE = 1.2V**

❖ **Explanation:**

- In this scenario, BL is significantly lower than BLB by a larger differential voltage ($\Delta V = 200mV$).

- With SE high, the sense amplifier is enabled and detects the large negative difference.
- The sense amplifier amplifies this large difference, resulting in a low output (logic '0').

❖ **Expected Output:**

- Low (logic '0'), as BL is much less than BLB.

Case 5: Sense Enable is Low (SE = Low)

❖ **Inputs:**

- **BL = Any Value**
- **BLB = Any Value**
- **SE = 0V**

❖ **Explanation:**

- In this case, the sense enable signal (SE) is low, meaning the sense amplifier is disabled.
- Regardless of the values on BL and BLB, the sense amplifier should not be active.
- The output should be undefined or zero since the sense amplifier is not detecting any differential signal