

UNIT 2

DEVICE MODELING

D.C. MODELS, SMALL SIGNAL MODELS, MOS MODELS,
MOSFET MODELS IN HIGH FREQUENCY AND SMALL
SIGNAL, SHORT CHANNEL DEVICES, SUB THRESHOLD
OPERATIONS, MODELING NOISE SOURCES IN MOSFETs

Q.1. What do you mean by device modeling ? (R.G.P.V., June 2016)

Ans. The aim of device modeling is to get the functional relationship between the terminal electrical variables of the device which is to be modeled. These electrical characteristics based on a parameter set containing geometric variables and variables dependent upon the device physics. Design parameters or process are all variables which appear in the equations. The design parameters controlled by the circuit designer. The characteristic of the semiconductor process are process parameters itself and are not at the control of the circuit designer once the process has been specified. At best only a good approximation to the real relationship of the electrical variables can be found, for most physical electrical devices. There are tradeoffs between the quality of the approximation and its complexity. The factors that the engineer considers when making these tradeoffs are the needed accuracy and the intended use of model. A simple

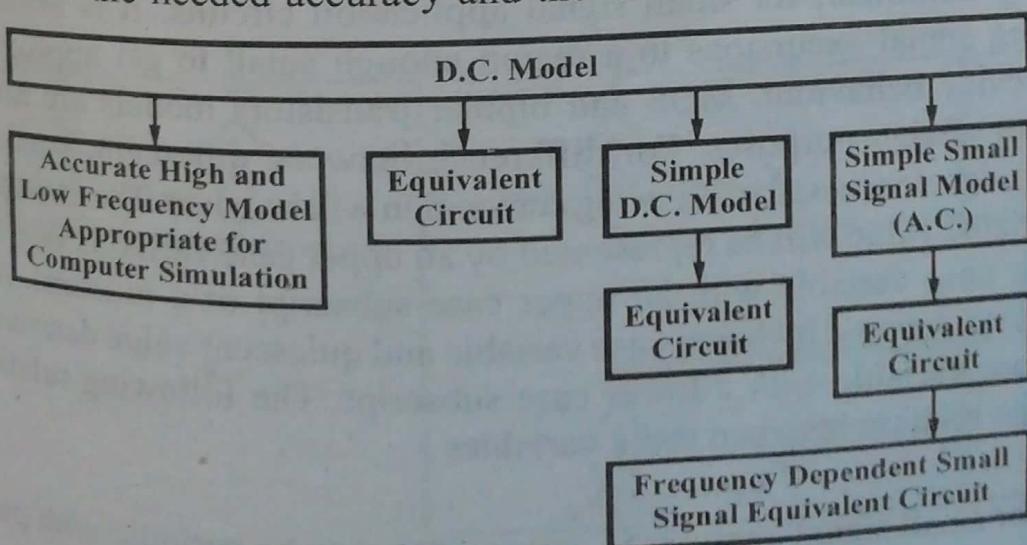


Fig. 2.1

model is normally required to give insight for design and facilitate hand manipulations where a more accurate and corresponding sophisticated model is normally preferred for computer simulation employing these devices. The beginning point for modeling the MOSFET discussed here will be a D.C. model. A linear small signal model equivalent simplified A.C. and D.C. circuit will be derived. The better agreement shown in fig. 2.1.

Q.2. What do you mean by modeling? Explain D.C. models.

Ans. Modeling – Refer to the ans. of Q.1.

(R.G.P.V., Dec. 2006)

D.C. Models – The D.C. model of a device is a mathematical relationship which relates the actual terminal voltages and currents at D.C. and low frequency. The D.C. model of a device must be valid over a large range of terminal voltages and currents. It is valid at frequencies in which the difference between the actual and D.C. solution is deemed negligible for the problem under investigation.

Q.3. Write short note on small signal model.

Ans. Circuits do the work for which they were designed over a limited excitation range. This range is particularly specified in terms of maximum input signal movement through an angle about some nominal point. These point internal to the circuit. In comparison to the supply voltages providing power to the circuit, these inputs are sinusoids of small amplitude. The process of small sinusoids propagation through the circuit is known as small signal analysis. Quiescent points or bias points are the points about which the circuit operates. BJTs and MOSFETs act as linear devices even though the devices are really nonlinear, for small signal application circuits. It is obtained by restricting signal excursions to a region enough small to get approximately linear device behaviour. MOS and bipolar transistors models are also very useful for design purposes. For difference between quiescent, small signal and large signal values, the following convention will be taken. The instantaneous total variable value will be represented by an upper case variable, or if require an upper case variable with an upper case subscript or a numeral. A small signal value denoted by lower case variable and quiescent value denoted by an upper case variable with a lower case subscript. The following relationship shows the relation between these variables –

$$V_C = v + V_c$$

where for small signal analysis V_c is considered to be periodic with period T and the quiescent value is explained by –

$$V_c = \frac{1}{T} \int_0^T V_C(t) dt$$

Hence, the small signal variable is the time varying component of V_c . Fig. 2.2 shows the relation between V_C , V_c and v .

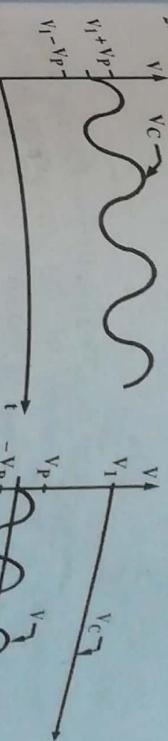
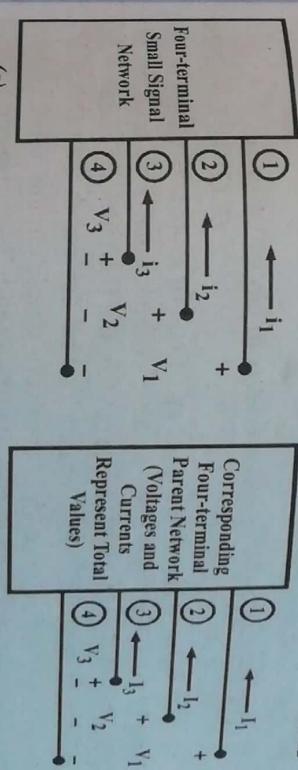


Fig. 2.2

In terms of h parameters, y parameters or g parameters, the electrical behaviour of linear multiple terminal networks can be modeled. Four terminal network for the linear small signal are shown in fig. 2.3 (a) in which terminal 4 is selected as a reference. With this reference and the consideration of linearity, it follows by definition that the y parameters relate the terminal currents and



(a)

(b)

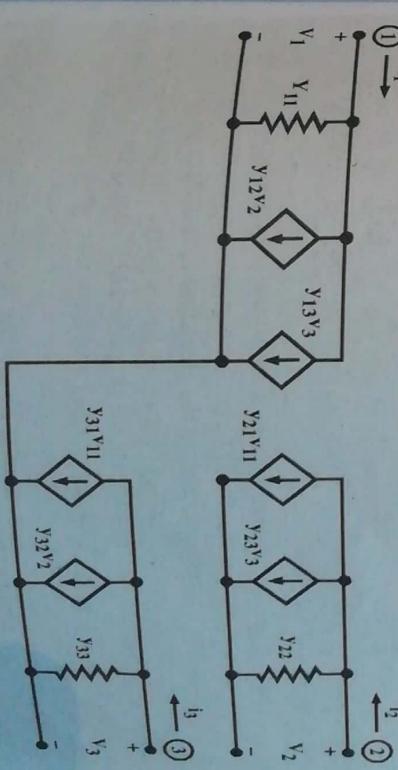


Fig. 2.3

voltages by the expressions as given below –

$$\begin{aligned} i_1 &= Y_{11}V_1 + Y_{12}V_2 + Y_{13}V_3 \\ i_2 &= Y_{21}V_1 + Y_{22}V_2 + Y_{23}V_3 \\ i_3 &= Y_{31}V_1 + Y_{32}V_2 + Y_{33}V_3 \end{aligned}$$

$$\text{Here } Y_{kj} = \left. \frac{i_k}{v_i} \right|_{v_m=0} \quad m \in \{1, 2, 3\}$$

The small signal voltage is the time varying part of the total terminal voltage and similarly the current variables are the time varying part of parent network relative to the Q-point as shown in fig. 2.3 (b). Hence it follows that y parameters can be determined from the large signal variables and hence from the D.C. model by the following expression –

$$Y_{kj} = \left. \frac{\partial I_k}{\partial V_j} \right|_{V_m=\text{quiescent value}, m \in \{1, 2, 3\}}$$

For circuit design and analysis a small signal equivalent circuit of the multiport network is found useful. Fig. 2.3 (c) shows the equivalent circuit for small signal networks.

Q.4. Explain the use of device models in circuit analysis.

(R.G.P.V., Dec. 2016)

Ans. Electrical circuits are made up of one or more active devices (i.e., BJTs or MOSFETs) and some passive components (i.e., resistors and capacitors). By using the D.C. device models, the D.C. transfer characteristics of a circuit can be achieved to characterize all devices in the network. It is observed that the D.C. analysis of even very simple circuits which comprise BJTs or MOSFETs is frequently unwieldy. Two points deserve mention, relating to the unwieldy nature of circuits analysis comprising non-linear devices.

- (i) Most existing practical circuits can be made up of very simple building blocks. The overall analysis are conveniently decomposed into the individual blocks analysis.

- (ii) It is often required to make simplifying assumptions on the device models to develop insight into the D.C. performance of even simple networks. The mathematical expressions relating the electrical parameters of interest are frequently so complicated that they obscure even the basic circuit functionality without these assumptions. In addition, the simplified D.C. analysis is sufficiently accurate to be useful for biasing purposes and may also give suitable insight into the small signal operation of a circuit.

There are two techniques used to obtain the low frequency small signal characteristics of circuit. The first technique involves replacing all devices and elements with a linear small signal equipment circuit where the parameter

are a function of the Q-point in the small signal modeling. The second technique is directly based upon the D.C. transfer characteristics. If the small signal input and output variables of interest are V_i and V_o , then these variables are related as follows –

$$\frac{V_o}{V_i} = \left. \frac{\partial V_o}{\partial V_i} \right|_{Q-\text{point}}$$

Q.5. Write short note on 'MOS models'?

Ans. While the ideal equations which describe the behaviour of MOS transistors incorporate some nonideal effects (channel-length modulation, threshold-voltage variation), they cannot accurately model a specific device in a particular process. It is especially true for devices which have very small dimensions (i.e., gate lengths, gate widths, oxide thickness) as the modeling process becomes increasingly 3D in nature. Various MOS models have been developed and refined in an effort to predict more precisely the performance of MOS devices before they are fabricated for varying design scenarios. As an example, D.C. currents might be predicted very precisely from raw process parameters, hence helping predict the behaviour of an yet untested device. But, it might not be suitable for a fast-execution-time model which might be required for digital simulation process, due to the complexity of the model. Therefore, a model formed by parameters measured from an actual process might be suitable.

Several MOS simulation models can be used, depending on the particular circuit level simulator which may be available. As an example, more than 10 models are possible in one commercial circuit simulator. The standardization of most CMOS digital foundry operations have been done on the LEVELS models in SPICE as the level of circuit modeling which is needed for CMOS digital system design.

Table 2.1 SPICE D.C. Parameters

Parameters	NMOS	PMOS	Units	Description
VTO	0.7	0.7	volt	Threshold voltage
KP	8×10^{-5}	2.5×10^{-5}	A/V ²	Transconductance coefficient
GAMMA	0.4	0.5	V ^{0.5}	Bulk threshold parameter
PHI	0.37	0.36	volt	Surface potential at strong inversion
LAMBDA	0.01	0.01	volt ⁻¹	Channel length modulation parameter
LD	0.1×10^{-6}	0.1×10^{-6}	meter	Lateral diffusion
TOX	2×10^{-8}	2×10^{-8}	meter	Oxide thickness
NSUB	2×10^{16}	4×10^{16}	1/cm ³	Substrate doping density

A summary of the main SPICE D.C. parameters which are used in Level 1, 2, and 3 with representative values for a 1μ n-well CMOS process is given in table 2.1. The process parameters are also included in the SPICE Level model parameters which are used to compute VTO, KP, GAMMA, PHI, and LAMBDA if they are not specified.

Q.6. Discuss the model of low frequency n-channel MOSFET.

(R.G.P.V., Dec. 2014) Clearly state the governing equations.

Or

(R.G.P.V., June 2015)

Explain D.C. MOSFET model in detail.

Ans. The experimentally obtained $I_D - V_{DS}$ characteristics as a function of V_{GS} for a typical MOSFET are shown in fig. 2.4. The starting point will be the D.C. model introduced by Sah in 1964 as follows –

$$I_D = \begin{cases} \frac{K'W}{L} \left[(V_{GS} - V_T) - \frac{V_{DS}}{2} \right] & V_{DS} < V_T \\ 0 & V_{GS} > V_T \end{cases} \quad \dots(i)$$

where L is the channel length, W is the channel width, K' is the transconductance parameter and V_T is the threshold voltage.

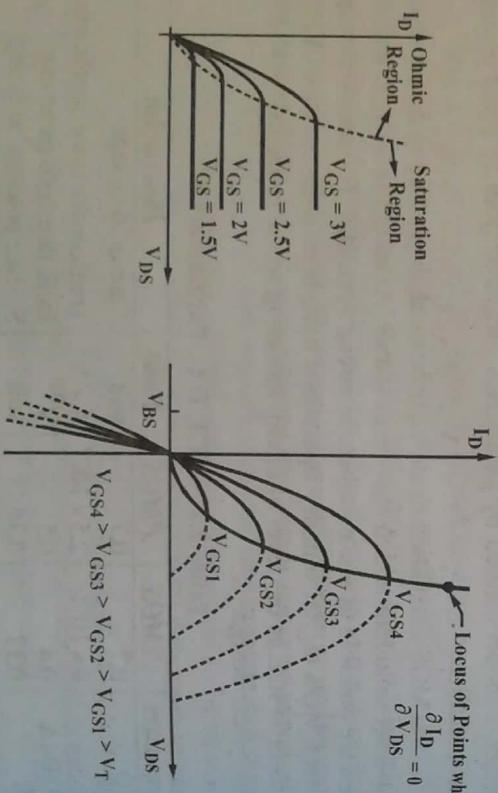


Fig. 2.4

Fig. 2.4 A plot of I_D versus V_{DS} for a MOSFET as given by equation (i) is represented in fig. 2.5 for several values of V_{GS} . The portions of the curves that have negative derivatives are dashed because Sah's model is good only when the derivatives are positive. The region in equation (i) is valid in the ohmic, linear, or active region. The point where the partial derivative of I_D

with respect to V_{DS} is zero is easily determined from equation (i) to be $V_{DS} = V_{GS} - V_T$... (iii)

This value of V_{DS} causes the channel to pinch off. For $V_{DS} > V_{GS} - V_T$, the current remains practically constant (not dependent of V_{DS}) at the value obtained when the channel first pinched off. Hence, this value is determined by evaluating equation (i) at $V_{DS} = V_{GS} - V_T$ to get

$$I_D = \frac{K'W}{2L} (V_{GS} - V_T)^2 \quad \dots(iv)$$

The drain current in the saturation region increases slightly in approximately a linear manner with V_{DS} . This is physically due to a slight shortening of the channel as V_{DS} is increased in the saturation region. Defining λ to be the coefficient which shows the linear dependence of I_D on V_{DS} , a more accurate expression for the drain current in the saturation region is obtained as –

$$I_D = \frac{K'W}{2L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \quad V_{DS} > V_T, V_{GS} > V_T \quad \dots(v)$$

The MOSFET model defined by equation (i) and equation (v), which differ from the model of Sah only through the parameter λ , is termed the Shichman-Hodges model. The discontinuity due to λ effects is shown in fig. 2.6. It should be noted that all projections from the saturation region into quadrant 2 intersect the V_{DS} axis at $-1/\lambda$.

The threshold voltage V_T is somewhat based on the bulk-source voltage. This dependence can be anticipated since the bulk-channel voltage will affect the carriers in the depletion region under the gate, which in turn affect the voltage that must be applied to the gate to form the inversion layer. This dependence is obtained as –

$$V_T = V_{T0} + \gamma(\sqrt{\phi - V_{BS}} - \sqrt{\phi})$$

where V_{BS} is the bulk-source voltage and V_{T0}, γ and ϕ are process parameters –

$$V_{T0} = \text{Threshold voltage for } V_{BS} = 0$$

$$\gamma = \text{Bulk threshold parameter}$$

$$\phi = \text{Strong inversion surface potential.}$$

The transconductance parameter K' is defined in terms of other physical process parameters by

$$K' = \mu C_{ox}$$

where C_{ox} = Capacitance density of the gate-channel capacitor, and μ Channel mobility.

A summary of the MOSFET model for n-channel devices which is enough for most D.C. hand calculations appears in table 2.2.

Table 2.2 Low Frequency n-channel MOSFET Model

$I_G = 0$	$V_{GS} < V_T$ (cutoff), $V_{DS} \geq 0$
$I_D = \begin{cases} 0 \\ \frac{K'W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \end{cases}$	$V_{GS} > V_T, 0 < V_{DS} < V_{GS} - V_T$ (ohmic)
$\frac{K'W}{2L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$	$V_{GS} > V_T, V_{DS} > V_{GS} - V_T$ (saturation)

$$\text{where } V_T = V_{T0} + \gamma(\sqrt{\phi} - V_{BS} - \sqrt{\phi})$$

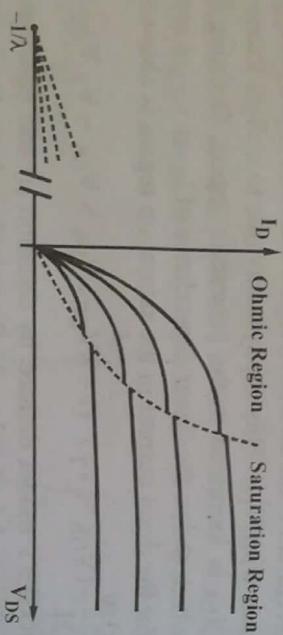


Fig. 2.6

Q. 7. Explain gradual channel approximation used to calculate the MOSFET current-voltage characteristics.

Ans. Gradual Channel Approximation – Gradual channel approximation (GCA) used to calculate the current-voltage characteristics of MOSFET. It was proposed by William Shockley. GCA is based on the assumption that the electric charge density related to the variation of the electric field in the channel in the direction parallel to the semiconductor-insulator interface is much smaller than the electric charge density related to the variation of the electric field in the direction perpendicular to the semiconductor insulator interface. Therefore, it is assumed that the channel potential is a gradually changing function of position and is varying very little over the distance of the order of the insulator thickness (t_{ox}) as shown in fig. 2.7. The two-dimensional Poisson's equation for the semiconductor is –

$$\frac{\partial F_x}{\partial x} + \frac{\partial F_y}{\partial y} = \frac{\rho}{\epsilon_s}$$

where, F_x and F_y are the x and y components of the electric field in the channel, ϵ_s is the dielectric permittivity of the semiconductor and ρ is the charge density in the channel. GCA is valid under the assumption

$$\frac{\partial F_x}{\partial x} \ll \frac{\partial F_y}{\partial y} \approx \frac{\rho}{\epsilon_s}$$

... (ii)

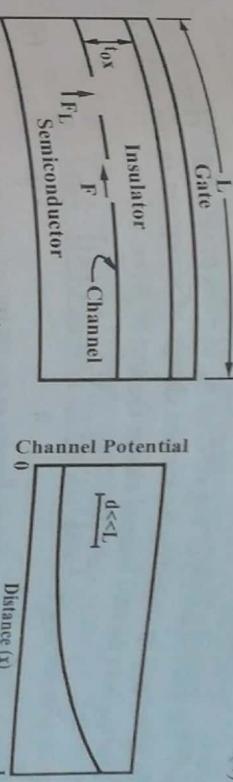


Fig. 2.7

The cross sectional view of an n-channel MOSFET is shown in fig. 2.8. At the surface end $x = 0$ and at the drain end $x = L$. The potential at the source i.e., the channel potential is represented by $V_C(x)$ and Q_s is the total surface charge density induced into the semiconductor layer considering a situation in which the device operates in the above threshold region and an inversion layer is present, the induced surface charge density Q_s is given by

$$Q_s = -C_{ox} [V_G - 2\phi_F - V_{FB} - V_C(x)] \quad \dots (iii)$$

$V_c(x)$ is the channel voltage and ϕ_F , V_{FB} will form the components of the threshold voltage later which is constant along the entire channel region. Equation (iii) can also be written as –

$$Q_s = -\frac{\epsilon_{ox}}{t_{ox}} [V_G - 2\phi_F - V_{FB} - V_C(x)] \quad \dots (iv)$$

Since the variation in $F_x \left(\frac{\partial F_x}{\partial x} \right)$ is very small as compared to the variation in $F_y \left(\frac{\partial F_y}{\partial y} \right)$, so F_x is dominant according to GCA. Our next assumptions lead to the boundary conditions for the channel voltage $V_C(x)$ (source grounded) ... (v)

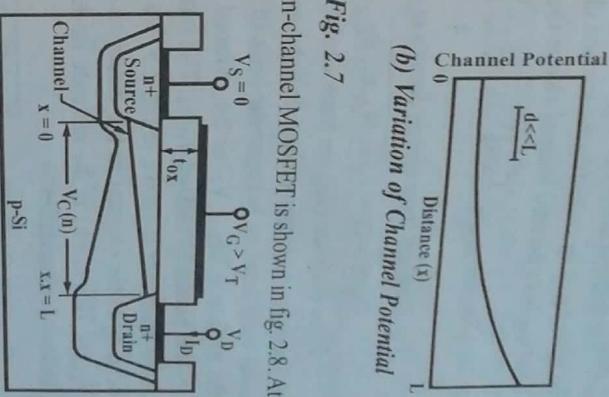


Fig. 2.8 Cross Sectional View of an n-channel MOSFET

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Also in the entire channel region $V_{GS} \geq V_T$.

The channel current I_D is due to the electrons in the channel region travelling from the source to drain under the influence of electric field F_x . Since the current flow is governed by the drift of electrons in the inversion layer, it is necessary to calculate accurately the total electron charge in this layer.

The induced density of free electron n_s , at each point of the channel can be determined by deducting the surface charge of acceptors in the depletion layer Q_B from the total induced charge Q_S and is given by,

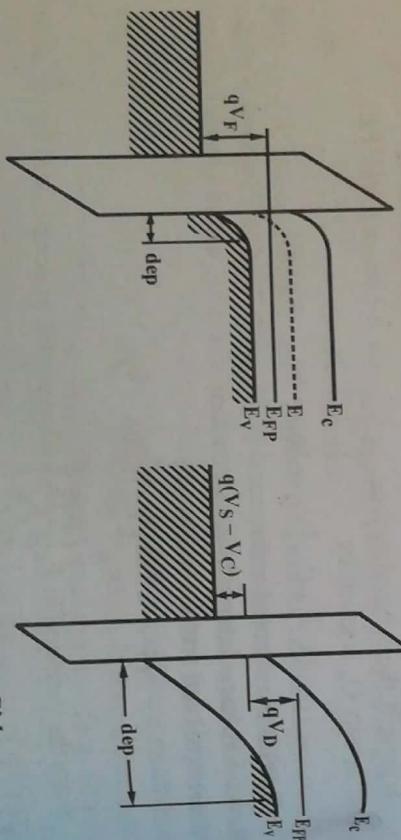
$$n_s = \frac{C_{ox}[V_{GS} - 2\phi_F - V_{FB} - V_C(x)]}{q} |Q_B| \quad \dots(vi)$$

The depletion layer charge density is given by,

$$Q_B(x=0) = -\sqrt{4qN_A\varepsilon_{si}\phi_F} \quad \dots(vii)$$

From equation (vii) we have already seen that the total band bending at the semiconductor surface is $2\phi_F$ and else where in the channel the total band bending between the bulk of the semiconductor substrate and the surface is $2\phi_F + V_C$ as the induced n-channel. Substrate junction is reverse biased by voltage $V_C(x)$. The band diagram at the source side and at the drain side is shown in fig. 2.9, we observe the increase of the band bending in the channel in the direction from the source to drain ($2\phi_F + V_C(x)$). This results in the increase in depletion layer charge density and equation (vii) modifies to,

$$Q_B(x=0) = -\sqrt{2\varepsilon_{si}qN_A(V_C(x) + 2\phi_F)} \quad \dots(viii)$$



(a) Source Side

Fig. 2.9 Energy Band Diagram of MOSFET

The channel potential $V_C(x)$ provides an additional reverse bias for the induced n-channel-p substrate junction.

The drain current I_D is written as

$$I_D = q\mu_n W n_s \frac{dV_C}{dx} \quad \dots(ix)$$

μ_n is the low field electron mobility, n_s is described by equation (vi) where, μ_n is the channel width. Consider a constant mobility model for the channel and W is the width, so that the electron velocity is proportional to the component of the electric field F_x in the channel parallel to the semiconductor-insulator interface as given by

$$V_n = \mu_n F_x$$

At high electric field, velocity saturation takes place and it strongly influence the electrical properties of the device at large values of drain to source bias.

Equation (ix) can be written as –

$$dx = \frac{q\mu_n n_s W}{I_D} dV_C \quad \dots(xi)$$

Integrating equation (xi) in the channel region i.e., from 0 (at source) to L (at drain), we get the expression for the drain current

$$\int_0^L dx = \int_0^{V_D} \frac{q\mu_n n_s W}{I_D} dV_C$$

$$I_D L = \int_0^{V_D} q \mu_n W \left[\frac{C_{ox}}{q} (V_{GS} - 2\phi_F - V_{FB} - V_C(x)) - \frac{Q_B}{q} \right] dV_C$$

$$I_D = \frac{\mu_n W C_{ox}}{L} \left\{ V_{GS} - 2\phi_F - V_{FB} - \frac{V_D}{2} \right\} \left[(V_D + 2\phi_F)^{3/2} - (2\phi_F)^{3/2} \right] \quad \dots(xii)$$

Equation (xii) shows the current-voltage characteristics as obtained by gradual channel approximation.

Fig. 2.10 shows the current-voltage characteristics of MOSFET as obtained by gradual channel app-

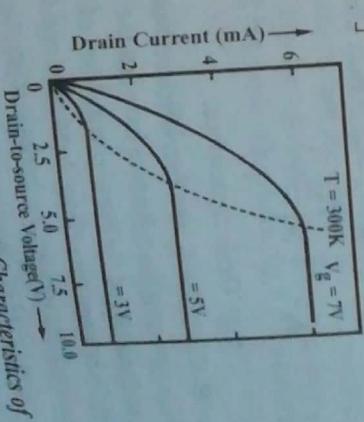


Fig. 2.10 Current-voltage Characteristics of MOSFET

Q.8 Explain threshold voltage with threshold voltage equations.

Ans. The voltage applied between the gate and the source of an MOS device below which the drain-to-source current I_{ds} effectively drops to zero is known as *the threshold voltage (V_t)* of an MOS transistor. Since the drain current never really is zero but drops to a very small value which can be deemed insignificant for the current application, the word 'effectively' is used.

Generally, the threshold voltage depends on the following parameters:

- (i) Gate insulation material
- (ii) Gate insulator thickness-channel doping
- (iii) Gate conductor material
- (iv) Voltage between the source and the substrate
- (v) Impurities at the silicon-insulator interface.

The absolute value of the threshold voltage also depends on the temperature. When temperature is increased, the absolute value of the threshold voltage decreases. This variation is $-2 \text{mV}^\circ\text{C}$ for low doping levels and $-4 \text{mV}^\circ\text{C}$ for high substrate doping levels.

The threshold voltage (V_t) is given by the expression as,

$$V_t = V_{t-\text{mos}} + V_{fb}$$

where, $V_{t-\text{mos}}$ = Ideal threshold voltage of an ideal MOS capacitor

V_{fb} = Flat-band voltage.

The MOS threshold voltage ($V_{t-\text{mos}}$) is the threshold where there is no work function difference between the gate and substrate materials. This is calculated by considering the MOS capacitor structure which makes the gate of the MOS transistor. Expression of the ideal threshold voltage is given as -

$$V_{t-\text{mos}} = 2\phi_b + \frac{Q_b}{C_{ox}}$$

where, $Q_b = \sqrt{2\varepsilon_{si}qN_A 2\phi_b}$ = Bulk charge term

$$\phi_b = \frac{kT}{q} \ln \left(\frac{N_A}{N_i} \right)$$

C_{ox} = Oxide capacitance.

Bulk potential (ϕ_b) is a term which accounts for the doping of the substrate which represents the difference between the Fermi energy level of the doped semiconductor and the Fermi energy level of the intrinsic semiconductor. The midway between the valence-band edge and the conduction-band edge of the semiconductor is called the intrinsic level.

In the case of a p-type semiconductor, the Fermi level is nearer to the valence band. On the other side, in an n-type semiconductor it is nearer to the

conduction band. N_p , which is equal to $1.45 \times 10^{10} \text{ cm}^{-3}$ at 300°K , is the carrier concentration in intrinsic (undoped) silicon and N_A is the density of carriers in the doped semiconductor substrate. The term C_{ox} is the density of capacitance, which is inversely proportional to the gate-oxide thickness (t_{ox}). The term ε_{si} is the permittivity of silicon ($1.06 \times 10^{-12} \text{ Farad/cm}$). The k is Boltzmann's constant ($1.380 \times 10^{-23} \text{ J/K}$) and T is the temperature (K). The term q is the electronic charge ($1.602 \times 10^{-19} \text{ Coulombs}$). Expression kT/q equals 0.02586 volts at 300°K . Threshold voltage ($V_{t-\text{mos}}$) is positive for n-transistors and negative for p-transistors.

Expression of the flatband voltage (V_{fb}) is given as -

$$V_{fb} = \phi_{ms} - \frac{Q_{fc}}{C_{ox}}$$

where, Q_{fc} = Fixed charge because of surface states which arise due to imperfections in the silicon oxide interface and doping.

ϕ_{ms} = Work function difference between the gate material and the silicon substrate ($\phi_{gate} - \phi_{si}$) which may be calculated for an n^+ gate over a p substrate, and is given by -

$$\phi_{ms} = -(E_g / 2 + \phi_b) \approx -0.9 \text{V} (N_A = 1 \times 10^{16} \text{ cm}^{-3})$$

where, E_g = Band gap energy of silicon.

$$= \left(1.16 - 0.704 \times 10^{-3} \frac{T^2}{T + 1108} \right)^5$$

T = Temperature in Kelvin.

For an n^+ polygate on an n-substrate -

$$\phi_{ms} = - \left(\frac{E_g}{2} - \phi_b \right) \approx -0.2 \text{V} (N_A = 1 \times 10^{16} \text{ cm}^{-3})$$

It is observed from these equations that for a given gate and substrate material, the threshold voltage can be varied by changing the doping concentration of the substrate (N_A), the oxide capacitance (C_{ox}) or the surface state charge (Q_{fc}).

Q.9. Explain different method to control threshold voltage of MOS device.

Ans. The value of threshold voltage (V_t) for the p-channel standard MOSFET is typically -4V , and it is common to use a power-supply voltage of -12V for the drain supply. This large voltage is incompatible with the power-supply voltage of typically 5V employed in bipolar integrated circuits. Hence, various manufacturing techniques have been developed to control V_t . Generally, a low threshold voltage permits - (i) the use of a small power-supply voltage.

(ii) compatible operation with bipolar devices, (iii) smaller switching time to the smaller voltage swing during switching and (iv) higher packing density.

To control the magnitude of threshold voltage, following three methods are used –

(i) High-threshold MOSFET described above uses a silicon crystal with $<111>$ orientation. When a crystal is utilized in the $<100>$ direction, it is observed that a value of V_t results which is about one half that found in $<111>$ orientation.

(ii) Silicon nitride approach makes use of a layer of Si_3N_4 and SiO_2 whose dielectric constant is about twice that of SiO_2 alone. A MOSFET built in this fashion (designated an NMOS device) reduces V_t to approximately 7V.

(iii) Instead of aluminum, polycrystalline silicon doped with boron is used as the gate electrode. This reduction in the difference in contact potential between the gate electrode and the gate dielectric reduces threshold voltage. Such devices are known as silicon gate MOS transistors.

All the three fabrication methods described above result in a low-threshold device with threshold voltage in the range 1.5 to 2.5V, whereas the standard high-threshold MOS has a threshold voltage of approximately 4 to 6V.

Q.10. Obtain an expression in terms of quiescent excess gate bias, V_p , that shows where the spectral density of the $1/f$ noise crosses over that of the thermal noise. Assume operation in the saturation region.

(R.G.P.V., Dec. 2011)

Ans. The thermal noise current is white noise, that has zero mean and is simply characterized by its spectral density as given below –

$$S_{\text{TW}} = \frac{4kT}{R_{\text{FET}}} ; \text{ For ohmic region}$$

$$S_{\text{TW}} = \frac{8kTg_m}{3} ; \text{ For saturation region}$$

In the ohmic and saturation regions, the flicker noise current is characterized by the spectral density as given below –

$$S_{\text{f}} = \frac{2K_f K' I_{\text{DQ}}}{C_{\text{ox}} L^2 f}$$

Equating equations (i) and (ii) for saturation region, we get

$$\frac{8kTg_m}{3} = \frac{2K_f K' I_{\text{DQ}}}{f C_{\text{ox}} L^2}$$

We know that,

$$I_D = \frac{K'W}{2L}(V_{\text{gs}} - V_t)^2$$

$$g_m = \sqrt{\frac{2K'W}{L} \sqrt{|I_{\text{DQ}}|}}$$

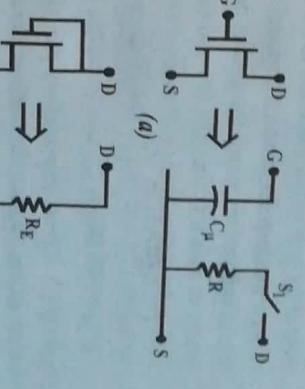
From equations (iv) and (v), equation (iii) simplifies to

$$f = \frac{3}{8kTC_{\text{ox}}} \left(\frac{V_{\text{gs}} - V_t}{L^2} \right) \text{ MHz}$$

It is seen that the relative impact of the thermal noise and flicker noise are strongly dependent on the quiescent operating point and the device size.

Q.11. Draw and explain all the MOSFET models for digital applications with the help of a suitable diagram. (R.G.P.V., Dec. 2015, 2017)

Ans. Many digital applications involve large numbers of gates and transistors which make hand analysis using the device models. This type of model will, of necessity, not provide highly accurate results. A very simple model that makes hand analysis tractable is needed for these applications. Models for the MOSFET used for simple analysis of digital circuits are shown in fig. 2.11.



In fig. 2.11 (a), the S_1 switch is open when $V_{\text{GS}} < V_H/2$ and closed when $V_{\text{GS}} > V_H/2$ here V_H is the logical high voltage in the digital logic family and where the logical low voltage is considered to be near zero. The values of R and C_μ are expressed as

$$C_\mu = C_{\text{ox}} WL \quad \dots(i)$$

$$R = \frac{L}{K'W(V_H - V_t)} \quad \dots(ii)$$

where V_t = Threshold voltage of MOSFET.

The two terminal enhancement and depletion configurations of fig. 2.11 (b) and (c) are characterized by

$$R_E = \frac{L}{K'W(V_H - V_{TE})}$$

$$R_D = \frac{L}{K'W|V_{TD}|}$$

where V_{TE} = Threshold voltage of the enhancement transistor

V_{TD} = Threshold voltage of the depletion transistor.

The model of fig. 2.11 (a) is motivated by the observation that in digital circuits, the inputs to the logic gates are typically inputs to the transistors, which swing between the high and low logic levels. It follows that the gate input port is capacitive with a value near $C_{ox}WL$ throughout the input signal swing. The output port looks nearly like an open circuit when the input is low and if the gate of the MOSFET is driven to V_H , where it is typically much larger than V_T , the output voltage is sufficiently low through most of the high to low transition to force operation in the ohmic region. In applications where the gate is permanently connected to the drain source as shown in fig. 2.11 (b) and (c), These models are used for simple D.C. and timing analysis with modest modifications of the resistances given in equations (iii) and (iv) to obtain closer agreement between theoretical and experimental results.

Q.12. Derive expressions for simple MOSFET models for digital applications. Explain derivations for the simple digital inverter.

(R.G.P.V., Dec. 2010)

Ans. Refer to the ans. of Q.11.

A simple digital inverter is shown in fig. 2.12.

A basic inverter circuit consists of a transistor with source connected to ground and load resistor of some short connected from drain to positive supply V_{DD} . The input is applied between gate and ground and output taken from the drain.

For $V_{gs} = 0$ all conditions are considered in the depletion mode transistor. It is also considered that in order to cascade inverters without degrading the levels. The following requirement is met i.e., $V_{in} = V_{out} = V_{inv}$.

The condition $V_{inv} = 0.5 V_{DD}$ is set for determining equal margin. At this point, both the transistors are in saturation. Then I_{ds} is given by

$$I_{ds} = K \frac{W(V_{gs} - V_t)^2}{L} \frac{2}{2}$$

Fig. 2.12 Simple Digital Invertor

$$\begin{aligned} & \text{In depletion mode (p.u. transistor, } V_{gs} = 0 \\ & I_{ds} = K \frac{W_{pd}}{L_{pu}} \frac{(-V_{id})^2}{2} \quad \dots(i) \\ & \text{and enhancement mode (p.d. transistor), } V_{gs} = V_{inv} \\ & I_{ds} = K \frac{W_{pd}}{L_{pd}} \frac{(V_{inv} - V_t)^2}{2} \quad \dots(ii) \end{aligned}$$

Equating equations (i) and (ii) because the currents in both transistors are equal, we obtain

$$K \frac{W_{pd}}{L_{pd}} \frac{(V_{inv} - V_t)^2}{2} = K \frac{W_{pu}}{L_{pu}} \frac{(-V_{id})^2}{2} \quad \dots(iii)$$

$$\text{If } Z_{p.d.} = L_{p.d.}/W_{p.d.} \text{ and } Z_{p.u.} = L_{p.u.}/W_{p.u.}, \text{ then the equation (iii) becomes}$$

$$\frac{1}{Z_{pd.}} \frac{(V_{inv} - V_t)^2}{2} = \frac{1}{Z_{pu.}} \frac{(-V_{id})^2}{2}$$

Thus,

$$V_{inv} = V_t - \frac{V_{id}}{\sqrt{Z_{p.u.}/Z_{pd.}}}$$

Q.13. Draw and explain small-signal MOSFET model.

(R.G.P.V., Dec. 2013, June 2017)

Ans. Although the MOS transistor is a nonlinear device, it can be approximated as linear for small changes around a bias point. This is useful for understanding the behaviour of amplifiers and other analog circuits. The currents and voltages can be written as

$$\begin{aligned} V_{gs} &= V_{GS} + v_{gs} \\ V_{ds} &= V_{DS} + v_{ds} \\ I_{ds} &= I_{DS} + i_{ds} \end{aligned} \quad \dots(i)$$

where the gate source voltage V_{gs} is expressed as a bias-point voltage V_{GS} plus a small-signal offset v_{gs} , as shown in fig. 2.13. The drain current also is expressed as a bias-point current I_{ds} plus a small-signal offset i_{ds} proportional to v_{gs} and v_{ds} .

MOS transistors are typically used in their saturation region in analog circuits. In saturation region in analog circuits. In

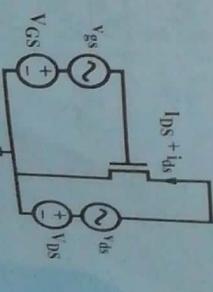


Fig. 2.13 Small-signal Variations Around Bias Point

$$= \frac{\beta}{2}(V_{GS} + v_{gs} - V_t)^2$$

$$= \frac{\beta}{2}[(V_{GS} - V_t)^2 + 2(V_{GS} - V_t)v_{gs} + v_{gs}^2]$$

$$= \frac{\beta}{2}\underbrace{(V_{GS} - V_t)^2}_{I_{DS}} + \underbrace{\beta(V_{GS} - V_t)v_{gs} + O(v_{gs}^2)}_{i_{ds}} \quad \text{...(ii)}$$

If v_{gs} is small enough, the $O(v_{gs}^2)$ term is negligible.

In general, we can find the sensitivity of current to small changes in voltage by taking the first-order Taylor series around the operating point,

$$I_{ds} \approx I_{DS} + \left. \frac{\partial I_{ds}}{\partial V_{gs}} \right|_{V_{gs}=V_{GS}} v_{gs} + \left. \frac{\partial I_{ds}}{\partial V_{ds}} \right|_{V_{ds}=V_{DS}} v_{ds} \quad \text{...(iii)}$$

we commonly write the sensitivities as

$$i_{ds} = g_m v_{gs} + g_{ds} v_{ds} \quad \text{...(iv)}$$

$$\text{where } g_m = \left. \frac{\partial I_{ds}}{\partial V_{gs}} \right|_{V_{gs}=V_{GS}}$$

$$= \beta(V_{GS} - V_t) \quad \text{...(v)}$$

and because the saturation current is ideally independent of V_{ds} ,

$$g_{ds} = \left. \frac{\partial I_{ds}}{\partial V_{ds}} \right|_{V_{ds}=V_{DS}} = 0 \quad \text{...(vi)}$$

This Taylor series approach gives the same results as the direct expansion in equation (ii).

In a real MOSFET, the output current does increase with V_{ds} because of channel length modulation.

$$I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2 (1 + \lambda V_{ds})$$

$$\therefore g_{ds} = \left. \frac{\partial I_{ds}}{\partial V_{ds}} \right|_{V_{ds}=V_{DS}} = \lambda \beta \frac{(V_{GS} - V_t)^2}{2} \quad \text{...(vii)}$$

$$= \lambda I_{DS} \quad \text{...(viii)}$$

g_m is called the transconductance because it reflects the dependence of the drain current on the gate voltage. g_{ds} is the output conductance, reflecting the dependence of the drain current on the drain voltage. Here λ is the channel length modulation coefficient, not the unit of distance. Recall that λ is inversely dependent on channel length. Current sources and high-gain analog amplifiers

require low output conductance and thus often use longer than minimum transistors. Often it is convenient to think about the reciprocal, output resistance,

$$r_o = r_{ds} = \frac{1}{g_{ds}} = \frac{1}{\lambda I_{DS}} \quad \text{...(viii)}$$

Fig. 2.14 shows the I-V characteristics of an n-MOS transistor annotated with the bias-point and small-signal parameters. The transistor is biased in saturation at $V_{GS} = 0.9$, $V_{DS} = 1.0$. The transconductance and output conductance are the slope of the I_{ds} curve with respect to small changes in V_{gs} and V_{ds} around the operating point.

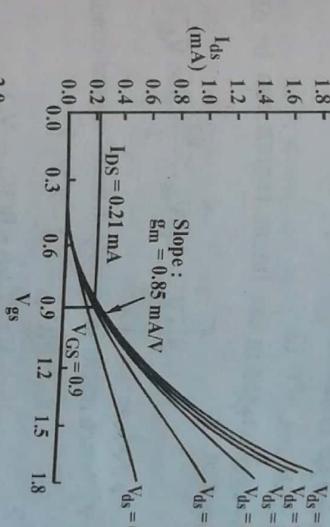


Fig. 2.14 Bias-point and Small-signal Behaviour

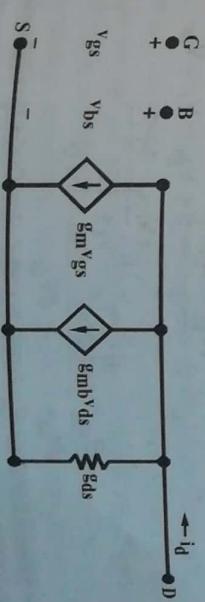


Fig. 2.15 Small-Signal Model Equivalent Circuit for MOS Transistor

Assuming the body is at the same potential as the source, we can model the transistor with the small-signal equivalent circuit of fig. 2.15 to relate

small-signal voltages and currents. The current source reflects the dependence of i_{ds} on V_{ds} . The capacitors of f_{ds} on V_{gs} and the resistor reflects the dependence of i_{ds} on V_{ds} . The capacitors can be considered for high-frequency operation or ignored for low-frequency operation. The results of the small-signal model are added to the results of the bias point to find the overall behaviour of the circuit.

Q.14. Explain the operating principle of MOS transistor at D.C. and low frequency.

Ans. Refer to the ans. of Q.6 and Q.13.

Q.15. Draw a low frequency small-signal model of MOS transistor g_m and derive the equation for its transconductance (g_m).

Ans. Refer to the ans. of Q.13.

The output conductance in the linear region can be obtained by differentiating equation

$$I_{ds} = \beta \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right] \quad 0 < V_{ds} < V_{gs} - V_t$$

with respect to V_{ds} , which results in an output drain source conductance of

$$\begin{aligned} g_{ds} &= \beta[(V_{gs} - V_t) - 2V_{ds}] \\ &= V_{ds} \lim_{V_{ds} \rightarrow 0} 0 \approx \beta(V_{gs} - V_t) \end{aligned} \quad \dots(i)$$

On rearrangement, the channel resistance R_c is approximated by

$$R_c(\text{linear}) = \frac{1}{\beta(V_{gs} - V_t)} \quad \dots(ii)$$

which indicates that it is controlled by the gate-to-source voltage. The relation defined by equation (ii) is valid for gate to source voltages that maintain constant mobility in the channel. In contrast, in saturation, the MOS device behaves like a current source, the current being almost independent of V_{ds} . This may be verified by

The saturation region

$$I_{ds} = \beta \frac{(V_{gs} - V_t)^2}{2} \quad 0 < V_{gs} - V_t < V_{ds}$$

$$\text{Since, } \frac{dI_{ds}}{dV_{ds}} = \frac{d}{dV_{ds}} \left[\frac{\beta}{2} (V_{gs} - V_t)^2 \right] = 0$$

The transconductance g_m expresses the relationship between output current I_{ds} and the input voltage V_{gs} and is defined by

$$g_m = \frac{di_{ds}}{dV_{gs}} |_{V_{ds}} = \text{Constant}$$

It is used to measure the gain of an MOS device. In the linear region g_m is given by

$$g_{m(\text{linear})} = \beta V_{ds}$$

 In the saturation region by,

$$g_{m(\text{sat})} = \beta(V_{gs} - V_t)$$

Q.16. Draw a high frequency model of MOS transistor and derive the equation for its transconductance (g_m) and transition frequency (f_T).

Or

Draw a high frequency model of MOS transistor and derive the equation for its transition frequency (f_T).

Or

Explain the high frequency MOSFET model.

(R.G.P.V., June 2015, Dec. 2015)

Ans. High Frequency for MOS Transistor – At high frequency, small signal models of the MOS transistor is generally considered inadequate. These limitations are to a large extent attributable to the unavoidable parasitic capacitances inherent in existing MOS structures. These parasitic capacitances can be divided into two groups. The first group is composed of those parasitic capacitors formed by sandwiching an insulating dielectric of fixed geometric dimensions between two conductive regions. The capacitances of these types of devices remains essentially constant for local changes in the voltage applied to the plates of the capacitor. Assuming the area of the normally projected intersection of the capacitor plates is A and that the distance between the plates is constant with thickness d , then this capacitance is given by the expression

$$C = \epsilon \frac{A}{d} \quad \dots(i)$$

where ϵ is the permittivity of the dielectric material separating the plates. Often it is more convenient to combine ϵ/d into a single parameter C_0 , called the capacitance density.

i.e., $C = C_0 A \quad \dots(ii)$

C_0 is thus a process parameter and A is a design parameter.

The second group is composed of the capacitors formed by the separation of charge associated with pn junction. The depletion region associated with the semiconductor junction serves as the dielectric. These junction capacitors are quite voltage dependent. They are typically expressed in terms of the process parameter C_{j0} , which denotes the junction capacitance density at zero volts bias. The capacitance of these devices can be approximated by

$$C = \frac{C_{j0} A}{(1 - V_F/\phi_B)^n} \quad \dots(iii)$$

where A is the junction area, V_F is the D.C. forward bias voltage junction, ϕ_B is the carrier potential, and n is a constant depending on the type of junction. This expression is reasonably good for $-\infty < V_F < \phi_B/2$.

Gate capacitance and the depletion capacitance play an important role in deciding the high frequency performance of the device. Fig. 2.16 shows the high frequency model for an MOS transistor.

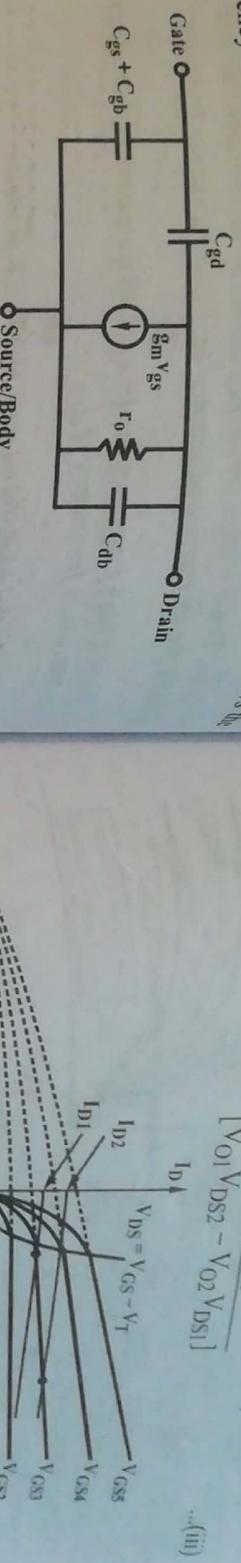


Fig. 2.16 High Frequency Model for MOS Transistor

The relation between the small signal parameter like transconductance (g_m) and the lower cut-off frequency can be given by

$$f_T = \frac{g_m}{2\pi C_g}$$

Q.17. Derive a relation for MOSFET models in high frequency for small signals.

Ans. Refer to the ans. of Q.16.

Q.18. Explain the method for measurement of λ and K' .

(R.G.P.V., Dec. 2013)

Ans. Measurement of λ – Consider the equation for the drain current of the MOSFET in the saturation region as follows –

$$I_D = \frac{K'W}{2L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

for $V_{GS} > V_T$, $V_{DS} > V_{GS} - V_T$... (i)

Equation (i) is drawn in fig. 2.17, for different values of $(V_{GS} - V_T)$ with constant V_{BS} . Projection of these curves into quadrant 2 represents that all curves intersect the V_{DS} axis at $V_{DS} = -1/\lambda$. Therefore, the parameter λ can be calculated by fixing V_{GS} and V_{BS} , thus fixing $(V_{GS} - V_T)$, and determining the $-V_{DS}$ axis intercept of I_D versus V_{DS} . If I_{D1} and I_{D2} are the currents corresponding to two distinct values of V_{DS} , V_{DS1} and V_{DS2} ; then, we get

$$\lambda = \frac{I_{D2} - I_{D1}}{I_{D1}V_{DS2} - I_{D2}V_{DS1}}$$

The circuit of fig. 2.18 with switch S_1 in position 1 is helpful for determining λ . The parameters V_{GS} and V_{BS} are fixed so that $V_{GS} > V_T$ for

operational amplifier is used to establish the relationship $V_O = -I_D R$ while maintaining a source voltage of nearly 0V. If $V_O = -I_D R$ while V_{DS1} and V_{DS2} are the two distinct output voltages for these inputs, then we get

$$\lambda = \frac{[V_O] V_{DS2} - V_O V_{DS1}}{V_{O2} - V_{O1}}$$

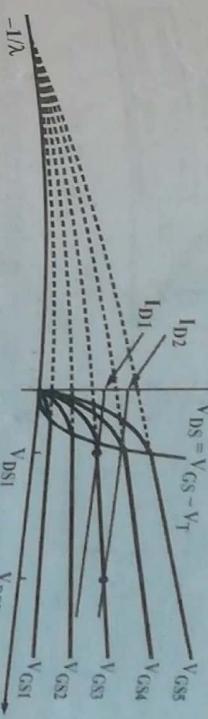


Fig. 2.17

Measurement of K' – It follows from equation (i) that K' can be calculated from a measurement of I_D for fixed values of V_{GS} and V_{DS} from the equation

$$K' = \frac{2L I_D}{W(V_{GS} - V_T)^2 (1 + \lambda V_{DS})}$$

The circuit of fig. 2.18 is again helpful for measuring K' .

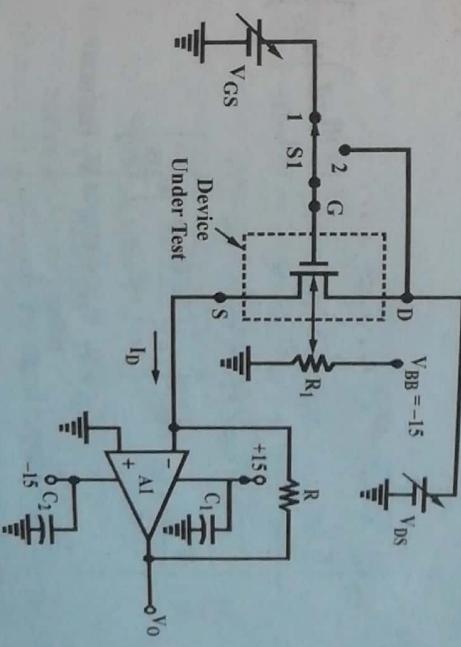


Fig. 2.18

Q.19. Explain short channel devices. Also mention its applications, advantages and limitations.

(R.G.P.V., Dec. 2013)

Ans. The minimum MOSFET device lengths has decreased from 10μ to 1μ range due to downward trends in device scaling. Device lengths in the 0.5μ range or below are projected by early 1990s. For shorter channel

lengths, the model is gradually deteriorate. Transistors with channel lengths less than 3 to 5 μ are referred to as short channel devices.

Geometrically, there is the change in the channel region from thin right rectangular region to irregular structure. Short channel transistors give some important advantages compared to larger transistors but have some limitations.

Improvements in speed and reduced area needs which are attainable with circuit employing short channel transistor are the important advantages. In the output impedance channel transistor characteristics is the major drawback. Better matching of short channel transistors but have some limitations.

A simple model of the MOSFET which is necessarily an extension of the long channel model is given by the following equations –

$$I_G = 0$$

$$I_D = \begin{cases} 0, & V_{GS} < V_T (\text{cut-off}) \\ \frac{K'W_{\text{eff}}}{L_{\text{eff}}} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \left[1 + \lambda \left(\frac{1 + \theta L_{\text{eff}}}{\theta L_{\text{eff}}} \right) V_{DS} \right], & V_{GS} > V_T, 0 < V_{DS} < V_{GS} - V_T \\ \frac{K'W_{\text{eff}}}{2L_{\text{eff}}} (V_{GS} - V_T)^2 \left[1 + \lambda \left(\frac{1 + \theta L_{\text{eff}}}{\theta L_{\text{eff}}} \right) V_{DS} \right] & V_{GS} > V_T, V_{DS} > V_{GS} - V_T (\text{saturation}) \end{cases} \quad \dots (iii)$$

where, L_{eff} = Effective channel length

W_{eff} = Effective channel width.

In digital logic, short channel devices are used, where a net improvement in speed and reduction in circuit area are readily obtainable in spite of performance limitations of the short channel MOSFET. If high output impedance and good matching characteristics are critical in analog application then short channel transistors find some uses in spite of the improvement frequency response.

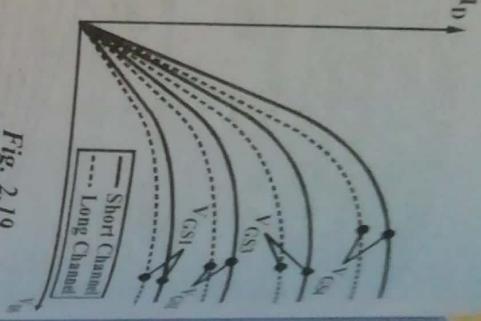


Fig. 2.19

Q.20. Explain in brief subthreshold operations with the help of suitable examples.

Or
(R.G.P.V., June 2016)

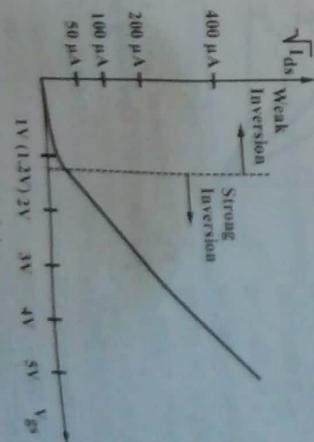
Ans. In the D.C. model of the MOSFET, the drain current for positive V_{DS} was assumed to be zero for $V_{GS} < V_t$ and nonzero for $V_{GS} > V_t$. In physical devices, such an abrupt transition is not anticipated and does not take place experimentally. However, the drain current is much smaller for $V_{GS} < V_t$ than for $V_{GS} > V_t$ and thus, in most applications, the assumption that $I_{ds} = 0$ for $V_{GS} < V_t$ is justifiable.

If $V_{GS} > V_t$, the devices are said to be operating in **strong inversion** or equivalently $V_{GS} < V_p$, the devices are said to be operating in **weak inversion** or equivalently in the subthreshold region. At room temperature, the transition between strong inversion and weak inversion actually takes place around $V_{GS} = V_t + 100$ mV. The following expression

$$V_{GS} = V_t + 2n V_T \quad \dots (i)$$

where n is a constant between 1 and 2, can be employed to predict the transition at other temperatures. Term V_T is equal to kT/q where k is a Boltzmann's constant ($k = 1.387 \times 10^{-23}$ V°C/K), T is the device temperature in degrees Kelvin and q is the charge of an electron ($q = 1.6 \times 10^{-19}$ C). At room temperature, $V_T = 26$ mV.

Fig. 2.20 shows a plot of I_{ds} versus V_{GS} for the MOSFET with $V_{DS} = V_{GS}$ for a wide range of V_{GS} values. From this figure, it is noted that the current in weak inversion is much smaller than the current in strong inversion. However, the behaviour is well characterized far into weak inversion and varies exponentially rather than quadratically with V_{GS} . The potential for very-low power dissipation should be apparent.



(a)

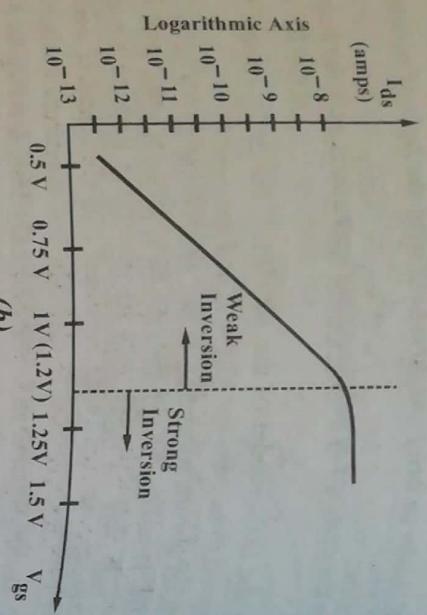


Fig. 2.20 Typical I_{ds} - V_{ds} Characteristics for MOSFET Operating in Weak Inversion, (a) Quadratic Vertical Axis, (b) Logarithmic Vertical Axis

$$(V_t = IV, V_{ds} = V_{gs})$$

A D.C. model for the MOSFET operating in weak inversion is required for both design and simulation. In weak inversion, the following model is useful –

$$\begin{aligned} I_g &= 0 \\ I_{ds} &= \frac{W}{L} I_{d0} e^{-V_{bs}[(1/nV_T) - (1/V_T)]} (1 - e^{-V_{ds}/V_T}) \\ &\quad \times e^{(V_{gs} - V_t)/(nV_T)} \end{aligned}$$

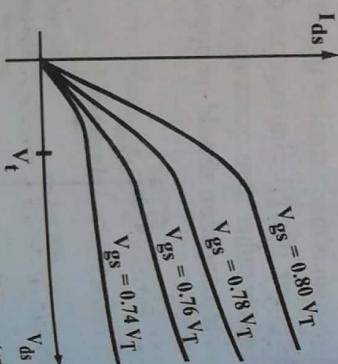
where V_t is the threshold voltage.

Constants I_{d0} and n are process parameters. Typical values of these parameters are $I_{d0} \approx 20$ nA and $n = 2$.

Fig. 2.21 depicts a typical plot of I_{ds} versus V_{ds} . It should be noted that for $V_{ds} > 3V_T$, the term e^{-V_{ds}/V_T} in equation (ii), and we find the equivalent of strong inversion saturation region of operation. Often $V_{bs} = 0$.

Under the assumption that $V_{bs} = 0$ and $V_{ds} > 3V_T$, equation (ii) becomes

$$\left. \begin{aligned} I_g &= 0 \\ I_{ds} &= \frac{W}{L} I_{d0} e^{(V_{gs} - V_t)/(nV_T)} \end{aligned} \right\}$$



Due to these practical limitations, it is often desirable to operate near the transition region between strong inversion and weak inversion, where some of the advantages of reduced power associated with weak inversion can be obtained but where these other limitations are not too problematic. Whereas diffusion current dominates weak inversion operation and drift current dominates strong inversion operation, both mechanisms interact in the transition region and hence complicate the modeling problem.

Q.21. Derive a relation for the subthreshold operations. How we can implement this operation on short channel devices?

(R.G.P.V., Dec. 2015, June 2017, Dec. 2017)

Ans. Refer to the ans. of Q.20 and Q.19.

Q.22. What do you mean by modeling noise sources for MOSFET?

(R.G.P.V., June 2015)

Explain in detail modeling noise sources in MOSFET.

(R.G.P.V., June 2017)

Ans. In MOSFETs, flicker noise and thermal noise are the primary contributors to the presence of noise. In the Si-SiO₂ interface region, flicker noise connected with the trapping and releasing of electrons. In the channel, thermal noise connected with the carriers. In either the small signal or large signal device model can be modeled as a current source between the source and drain because these noise sources contribute to the total drain current, as shown in fig. 2.22 (a).

However, it is often the case that power supply restrictions will need operation of subthreshold devices with smaller values of V_{ds} . Parameter I_{d0} is related to the transconductance parameter and is approximately given as –

$$I_{d0} = \frac{k'2(nV_T)^2}{e^2}$$

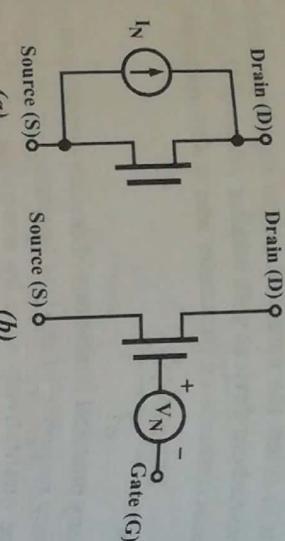


Fig. 2.22

The thermal noise current is white noise, which has zero mean. It is simply characterized by its spectral density as given below –

$$S_{IW} = \begin{cases} \frac{4kT}{R_{FET}} & \text{(ohmic region)} \\ \frac{8kTg_m}{3} & \text{(saturation region)} \end{cases}$$

where, R_{FET} = Equivalent FET resistance
 T = Temperature in °K

K = Boltzmann's constant
 g_m = Small signal transconductance.

In the ohmic region and saturation region, flicker noise current characterized by the spectral density –

$$S_{IF} = \frac{2K_f K' I_{DQ}}{C_{ox} L^2 f}$$

where I_{DQ} = Quiescent current

K_f = Flicker noise coefficient

f = Frequency

K' , C_{ox} , L = MOSFET model parameters.

The spectral current density of noise current source I_N can be determined by adding S_{If} and S_{IW} as given below –

$$S_N = S_{IW} + S_{IF}$$

In the frequency band $[f_1, f_2]$, RMS noise current source can be determined from the spectral density and is given by –

$$I_{NB} = \sqrt{\int_{f_1}^{f_2} S_N df}$$

It is noted that, if we define RMS flicker noise and white noise current by the square root of the integral of the spectral densities –

Hence,

Q.23. How noise sources are modeled? Illustrate with an example.

(R.G.P.V., Dec. 2014, June 2017)

Ans. Refer to the ans. of Q.22 and sol. of Prob.1.

NUMERICAL PROBLEMS

Prob.1. Fig. 2.23 shows a simple transconductance amplifier. Determine the output noise current spectral density, the input-referred voltage spectral density and the RMS output thermal noise current, the RMS output flicker noise current, the input-referred RMS noise current, and the input-referred RMS noise voltage in the flat frequency band from 100 Hz to 1 MHz if the small signal input voltage is zero. Suppose $W = 5 \mu$, $L = 5 \mu$, $V_{gg} = 2V$, $K_f = 3 \times 10^{-24} V^2 F$.

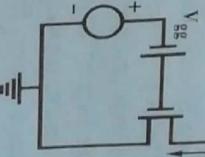


Fig. 2.23

Sol. Observe that the MOSFET is operating in the saturation region since $V_{DS} = V_{DD} > V_{GS} - V_T$. Then we get

$$I_{DQ} = \frac{K' W}{2L} (V_{GSQ} - V_T)^2 = 18.75 \mu\text{A}$$

$$g_m = \sqrt{\frac{2K' W}{L}} \sqrt{I_{DQ}} = 30.0 \mu\text{A/V}$$

Therefore, we get

$$S_{IW} = 3.3 \times 10^{-25} \text{ A}^2 \cdot \text{sec}$$

$$S_{IF} = \frac{1.54 \times 10^{-19}}{f} \text{ A}^2 \cdot \text{sec}$$

$$S_N = 3.3 \times 10^{-25} + \frac{1.54 \times 10^{-19}}{f} \text{ A}^2 \cdot \text{sec}$$

or

$$I_{WB} = \sqrt{\int_{10^2}^{10^6} S_{IW} df} = 0.489 \text{ nA(RMS)}$$

$$I_{FB} = \sqrt{\int_{I_0^2}^{10^6} S_I F dF} = 1.190 \text{ nA (RMS)}$$

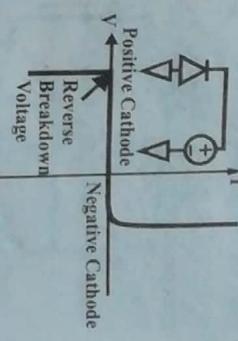
$$I_{NB} = \sqrt{I_{WB}^2 + I_{FB}^2} = 1.29 \text{ nA (RMS)}$$

$$V_N = \frac{I_N}{g_m} = 43 \mu\text{V (RMS)}$$

and

DIODE MODELS, BIPOLE MODELS, PASSIVE COMPONENTS MODELS

$$I_{\text{forward}} = I_s e^{\frac{qV}{kT}}$$



The current rapidly increases when the cathode-anode voltage is less than -0.6V as shown in fig. 2.25. The x-axis is reflected.

Q.26. Explain the following –

- (i) Small signal diode model
- (ii) High frequency diode model

Ans. (i) Small Signal Diode Model – In low frequency small signal applications diode is rarely used and like a small signal model requirement not be developed. Hence, the small signal model of diode is very simple. The low frequency small signal model is an open circuit for reverse bias. It is modeled by a single resistor of value calculated by –

$$r_V = \frac{nV_t}{I} \quad (\text{R.G.P.V., Dec. 2013})$$

Q.25. Explain the D.C. model for diode.

Ans. Fig. 2.25 shows the V/I characteristics of a diode. In a diode, the current is expressed as –

$$I = A_d I_s \left(e^{\frac{qV}{kmt}} - 1 \right) \quad \dots (i)$$

Here, I and V are the coordinates of the operating point. As a capacitor, the diode is sometimes used in high frequency small signal applications. The diode is often termed as varactor diode, if used as a capacitor.

(ii) High Frequency Diode Model – The capacitance made by the depletion region in the p-n junction becomes significant, at high frequencies. It is modeled by a capacitor connected between the terminals of the diode of value

$$C = \begin{cases} \frac{C_{j0}A}{\left(1 - \frac{V}{\phi_B}\right)^n} & V < \frac{\phi_B}{2} \\ 2^n C_{j0}A \left[\frac{2nV}{\phi_B} + (1 - n) \right] & V > \frac{\phi_B}{2} \end{cases}$$

where,

- k = Boltzmann's constant
- m = A constant between 1 and 2 to account for various nonlinearities
- t = Temperature, q = Electronic charge

Ans. Fig. 2.25 shows the V/I characteristics of a diode. In a diode, the current is given to the cathode with respect to the anode, then electrons are attracted to the supply and holes are repelled, leading to a "reverse-biased" condition which a very small reverse current flows, which results in a depletion region similar to that in the MOS transistor if it is in the depletion region before inversion. In the equation (i), the exponential term is reduced in importance.

and the current is approximated as ($A_d = 1$) –

$$I_{\text{reverse}} = -I_s \left(\sim 1 \times 10^{-15} \text{ A} \right) \quad \dots (ii)$$

This condition applies until the voltage exceeds the reverse breakdown voltage of the junction, at which point the current increases quickly owing to avalanche multiplication. This takes place when electrons accelerated by the high field across the junction impact silicon atoms, thereby generating electron hole pairs.

If a negative voltage is given to the cathode, then diode becomes forward biased. The current is approximated as ($A_d = 1$) –

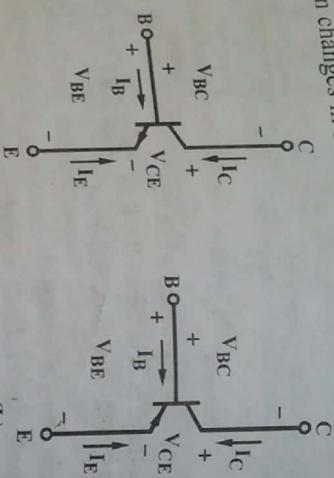
$$I_{\text{forward}} = I_s e^{\frac{qV}{kT}}$$

Fig. 2.25 *V/I Characteristics of Diode*

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Q.27. How the circuits and signals get affected by changing by changing the circuit from low frequency to high frequency? Explain. (R.G.P.V., Dec. 2013)

Ans. Refer to the ans. of Q.26.
Q.28. What is meant by bipolar model?

Ans. Fig. 2.26 shows the npn and pnp bipolar transistors and the convention for the electrical variables. The pnp development will be identical with the exception of sign changes in some of the equations.



(a) npn

(b) pnp

Fig. 2.26 Convention for Electrical Variables of BJT Transistors

Q.29. Explain the D.C. model for BJT. (R.G.P.V., Dec. 2013)

Ans. The relationship among the terminal variables in Ebers and Moll model is given by the following equations –

$$I_C = I_S \left(e^{(V_{BE}/V_t)} - 1 \right) - \frac{I_S}{\alpha_R} \left(e^{(V_{BC}/V_t)} - 1 \right) \quad \dots(i)$$

$$I_E = \frac{-I_S}{\alpha_F} \left(e^{(V_{BE}/V_t)} - 1 \right) + I_S \left(e^{(V_{BC}/V_t)} - 1 \right) \quad \dots(ii)$$

The device is characterized by I_S , α_R , α_F and V_t parameters.

Where,

α_R = Large signal reverse current gain of common base configuration
 α_F = Large signal forward current gain of common base configuration
 I_S = Transport saturation current

and
 $V_t = \frac{kT}{q}$

Here,
 T = Absolute temperature

k = Boltzmann's constant
 q = Charge of electron.

Following two equations along with KCL and KVL applied to the transistor itself –

$$I_B = -I_C - I_E \quad \dots(iii)$$

$$V_{CE} = V_{BE} - V_{BC} \quad \dots(iv)$$

The BJT is characterized by these four equations.

It is noted that there is complete functional symmetry in the device model with respect to the collector and emitter terminals.

Impurity concentrations and junction depths calculates the α_F and α_R parameters, and as such process parameters. The transport saturation current can be determined as –

$$I_S = J_S A$$

Here, A = Area of the emitter
 J_S = Transport saturation current density.

J_S parameter can be expressed as,

$$J_S = q \bar{D}_n n_i^2 / Q_B$$

Where,

\bar{D}_n = Average effective electron diffusion constant

Q_B = Number of doping atoms in the base per unit area
 n_i = Intrinsic carrier concentration in silicon.

The circuit of fig. 2.27 serves as an equivalent circuit where the currents in the two diodes satisfy the standard diode equations –

$$I_F = \frac{I_S}{\alpha_F} \left(e^{(V_{BE}/V_t)} - 1 \right)$$

$$I_R = \frac{I_S}{\alpha_R} \left(e^{(V_{BC}/V_t)} - 1 \right)$$

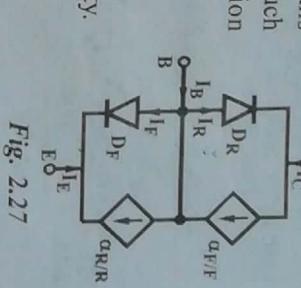


Fig. 2.27

Q.30. Explain in brief forward and reverse active regions of operation in BJT.

Ans. Mostly, in linear applications, BJT is operated in forward active region. When $V_{BE} > 0.5$ V and $V_{BC} < 0.3$ V, then the terminal variables simplify to

$$I_C = I_S e^{(V_{BE}/V_t)} \quad \dots(i)$$

$$I_E = -\frac{I_S}{\alpha_F} e^{(V_{BE}/V_t)} \quad \dots(ii)$$

It is convenient to use I_C and I_B rather than I_C and I_E as the dependent variables if modeling the BJT. β_F is given by

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F}$$

From equations (i) and (ii), I_C and I_B can be written as

$$I_C = I_S e^{(V_{BE}/V_t)}$$

$$I_B = \frac{I_S}{\beta_F} e^{(V_{BE}/V_t)}$$

BJT works as a good current amplifier in forward active region, from base to the collector with the gain relationship

$$I_C = \beta_F I_B$$

Similarly, if β_R is described as

$$\beta_R = \frac{\alpha_R}{1 - \alpha_R}$$

$$I_E = I_S e^{(V_{BC}/V_t)}$$

then,

$$I_B = \frac{I_S}{\beta_R} e^{(V_{BC}/V_t)}$$

Base-to-emitter current gain in the reverse active region is given as follows -

$$I_E = \beta_R I_B$$

Q.31. Explain the high frequency diode model which explain the bipolar model circuits for D.C. BJT model. (R.G.P.V, June 2016)

Ans. High Frequency Diode Model – At high frequencies, the parasitic junction capacitance of the diode plays an important role in the diode performance and also effects the transient response. The small signal parasitic capacitance can be expressed as follows –

$$C_D = \frac{dQ}{dV_D} \quad \text{...(i)}$$

The characterization of a junction capacitance under forward bias is different from the characterization under reverse bias. Under reverse bias ($V_D < FC \cdot \phi_B$), C_D is given by

$$C_D = \frac{C_{j0} A_n}{\left[1 - \left(\frac{V_D}{\phi_B}\right)\right]^m} + \frac{\tau I_S A_n e^{\left(\frac{V_D}{nV_t}\right)}}{nV_t} \underbrace{\left[1 - \left(\frac{V_D}{\phi_B}\right)\right]}_{\text{II}^{\text{nd}} \text{ Term}} \quad \text{...(ii)}$$

where,
 A_n = Normalized cross-sectional area of the function
 C_{j0} = Zero-bias junction capacitance

I_s = Saturation current
 ϕ_B = Capacitance barrier potential
 n = Emission coefficient
 FC = Coefficient for forward/reverse bias transition
 m = Coefficient of grading
 τ = Transit time

Therefore, I^{st} term of the equation (i) is essentially functionally equivalent to that used in the junction capacitance model for the MOSFET.

The II^{nd} term of the equation (i) increases from the charge stored in the junction because of minority carrier injection.

Under forward bias (for $V_D > FC \cdot \phi_B$), C_D is given by the equation

$$C_D = \frac{C_{j0} A_n}{[1 - FC(1+m)]} \underbrace{\left[1 - FC(1+m) + \frac{mV_D}{\phi_B}\right]}_{\text{I}^{\text{st}} \text{ Term}} + \frac{\tau I_S A_n}{nV_t} e^{\left(\frac{V_D}{nV_t}\right)} \underbrace{e^{-\left(\frac{V_D}{nV_t}\right)}}_{\text{II}^{\text{nd}} \text{ Term}} \quad \text{...(ii)}$$

The I^{st} term of the equation (ii) indicates a continuous and differentiable linear extension of the I^{st} term of equation (i) across the boundary $V_D = FC \cdot \phi_B$. The II^{nd} term of the equations (i) and (ii) are identical.

D.C. BJT Model – Refer to the ans. of Q.29.

Q.32. Write short note on small signal model for BJT.

Ans. The small signal model can be obtained directly from the D.C. model. For most small signal applications, the BJT is biased to operate in the forward active region and small signal model will be restricted to forward active region. In this region, the collector current I_C and base current I_B are given by the equations.

$$I_C = J_S A e^{(V_{BE}/V_t)} \left(1 + \frac{V_{CE}}{V_{AF}}\right) \quad \text{...(i)}$$

$$I_B = \frac{J_S A}{\beta_F} e^{(V_{BE}/V_t)} \quad \text{...(ii)}$$

Because the BJT is modeled as a three terminal device to obtain the small signal model for BJT. The base and collector nodes of the BJT are denoted by B and C and emitter node by E. The parameter y_{cb} is normally the dominant parameter in the model. This is given by

$$y_{cb} = g_m = \left. \frac{\partial I_C}{\partial V_{BE}} \right|_{V_{BE}=V_{BEO}, V_{CE}=V_{CEO}}$$

$$= \frac{\partial}{\partial V_{BEQ}} \left[J_S A e^{(V_{BEQ}/V_t)} \left(1 + \frac{V_{CEO}}{V_{AF}} \right) \right]$$

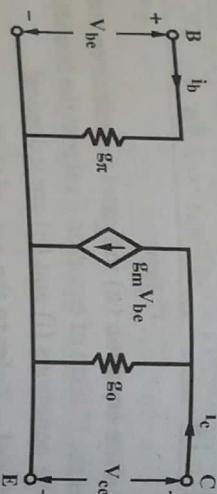
$$= \frac{J_S A}{V_t} e^{\left(\frac{V_{BEQ}}{V_t}\right)} \left(1 + \frac{V_{CEO}}{V_{AF}} \right)$$

Equation (iii) is evaluating at the Q-point and clearing that $\frac{V_{CEO}}{V_{AF}}$

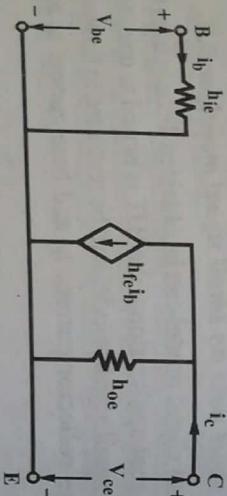
then

$$g_m = \frac{I_{CQ}}{V_t}$$

Fig. 2.28 shows the small signal model equivalent circuit and the small signal model parameters for BJT is given in table 2.3.



(a) *Y-parameter Model*



(b) *h-parameter Model*

Fig. 2.28 Small Signal Model for BJT

Table 2.3

S.No.	<i>h</i> -parameters	<i>Y</i> -parameters
(i)	$h_{fe} = \beta_F$	$y_{cb} = g_m = \frac{I_{CQ}}{V_t}$
(ii)	$h_{ie} = \frac{\beta_F V_t}{I_{CQ}}$	$y_{be} = g_\pi = \frac{g_m}{\beta_F}$
(iii)	$h_{re} = 0$	$y_{bc} = 0$
(iv)	$h_{oe} = \frac{I_{CQ}}{V_{AF}}$	$y_{CC} = g_o = \frac{g_m V_t}{V_{AF}} = \frac{I_{CQ}}{V_{AF}}$

Q.33. Write short note on passive component models.

Ans. Discrete passive elements are very simple to model. Ideal capacitors and registers can models capacitors and registers respectively. Temperature deviations and manufacturing tolerances are the major disadvantages, both of which can be reduced to acceptable levels in most applications via judicious component selection. Monolithic resistors and capacitors are temperature and voltage dependent. Area constraints limits the practical range of values. Large capacitor or resistors values are impractical. Figures of merit, which are used to characterize the passive components are given below –

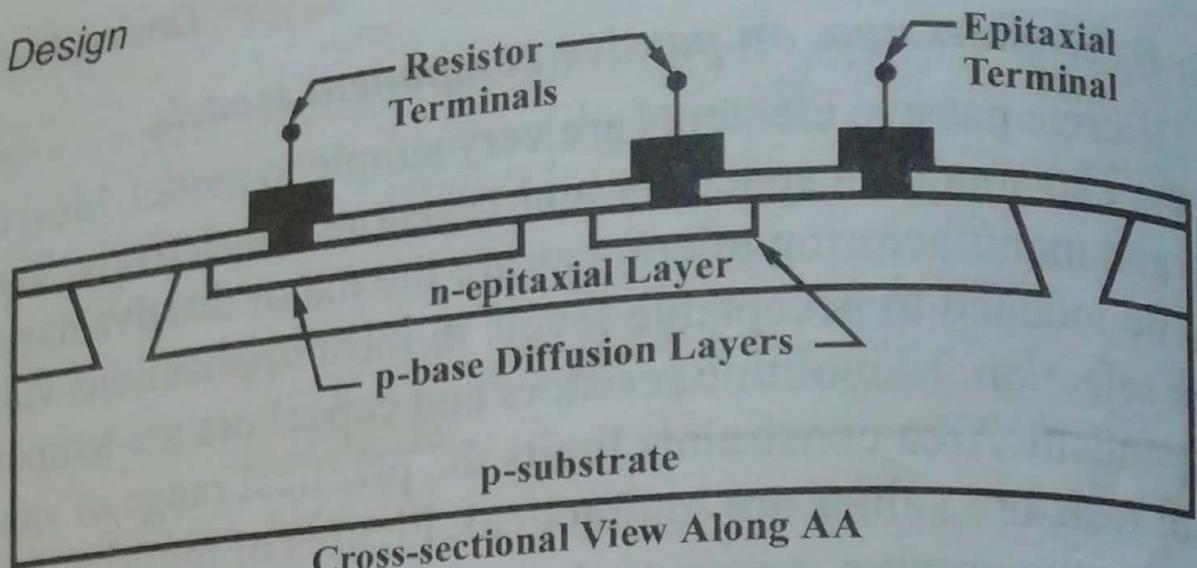
- (i) Sheet resistance
- (ii) Capacitance or resistance density
- (iii) Voltage coefficients of capacitance or resistance
- (iv) Temperature coefficients of capacitance or resistance
- (v) Relative accuracy of capacitance.
- (vi) Absolute accuracy of capacitance.

Q.34. Explain in brief the following –
 (i) *Monolithic capacitors* (ii) *Monolithic resistors*.

(R.G.P.V., June 2015)

Ans. (i) Monolithic Capacitors – A capacitor is a structure in which a voltage induced separation of charge generates. Common capacitors are made by sandwiching a thin oxide layer among two conductive polysilicon layers in a MOS process. These capacitors do not depend on applied voltage and can be modeled as ideal capacitors. Large parasitic capacitor which is always formed between the lower plate and the substrate is the main drawback. Metal-diffusion, poly-diffusion or metal-poly capacitors with an SiO_2 dielectric are used, if the luxury of the double polysilicon layers is absent in MOS processes. In comparison of double poly capacitors these capacitors have a lower capacitance density and/or increased voltage dependence and/or less conductive lower plate. Metal-diffusion capacitors with an SiO_2 dielectric are the common capacitors in the bipolar process. For the lower diffusion plate, heavily doped emitter diffusion is used.

(ii) Monolithic Resistors – Some monolithic resistors are passive devices and others are active devices. Generally ideal resistors are merely strips of polysilicon in standard MOS processes. Diffusion strips are also used for resistors although exhibit an nonlinear relationship between current and voltage. Diffusion strips or epitaxial strips are used for resistors in bipolar processes. These devices are quite linear. Mostly base diffusion is used due to its reasonably high sheet resistance. A contact is required to the epitaxial layer to stop forward biasing of the base collector junction. A base diffused resistor is shown in fig. 2.29.



Cross-sectional View Along AA

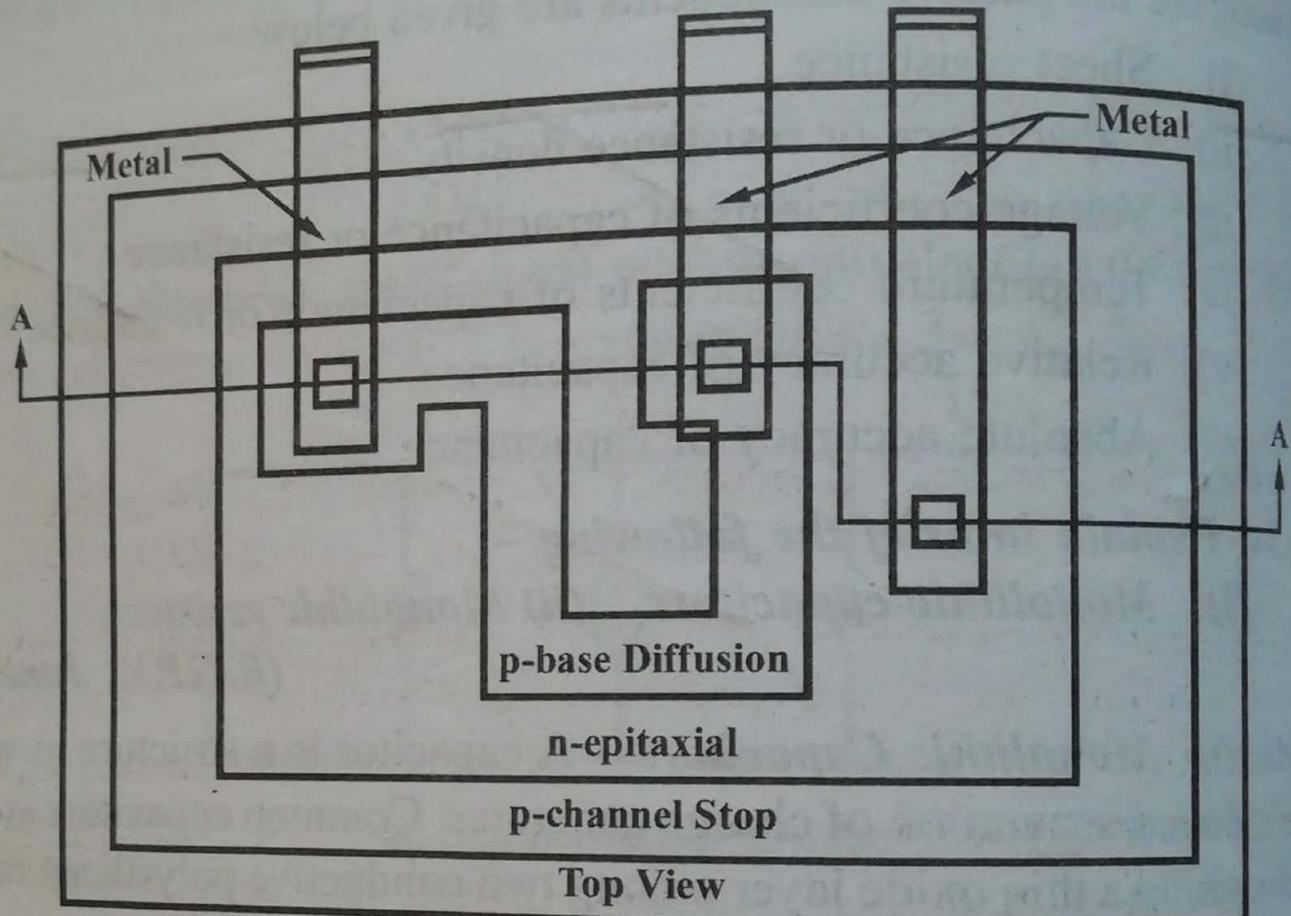


Fig. 2.29