

UNIT

1

PRACTICAL CONSIDERATION & TECHNOLOGY IN VLSI DESIGN

INTRODUCTION, SIZE AND COMPLEXITY OF INTEGRATED CIRCUITS, THE MICROELECTRONICS FIELD

Q.1. Write in brief historical overview of VLSI technology.

Or

Give a brief history of VLSI design explaining the effects of transistors in the discussion. *(R.G.P.V., Dec. 2016)*

Ans. The first integrated circuit is invented by Jack Kilby in 1958. The particular details of Kilby's circuit are inconsequential, although the impact of his approach has been phenomenal. Noyce and Kilby work, mark the starting of what has become the VLSI design field. In early days few devices used germanium as a semiconductor. Presently, for IC fabrication silicon is used as a semiconductor because one fourth part of the earth's crust is made of silicon. Some other materials like gallium arsenides are gaining acceptance in niche markets that can be very profitable. Many ICs have a large number of transistors, over one million in some designs. Traditional methods for design of circuit which involved iteration at the breadboard level proved impractical for designing integrated circuits. This is because of poor designer productivity and the high cost related with fabricating IC. The tools available now to the integrated circuit maker, are very powerful and dynamic. Most need the use of large computers or more presently powerful graphics-intense workstations. Integrated circuit fabrication needs the use of mechanical and optical equipments and materials capable of precisely maintaining close tolerances and small geometries.

Q.2. Define some important terms related to VLSI design.

Ans. (i) Integrated Circuit – The combination of interconnected circuit elements inseparably associated on or within a continuous substrate is known as integrated circuit.

(ii) Monolithic IC – An integrated circuit whose elements are formed in place upon or within a semiconductor substrate with atleast one of the elements formed within the substrate.

(iii) **Hybrid IC** – An IC with some discrete elements or a combination of two or more IC types is known as hybrid IC.

(iv) **Substrate** – An integrated circuit is fabricated upon or within the supporting materials that is known as substrate.

(v) **Chip** – One of the repeated ICs on a wafer is known as chip. According to complexity and size of the circuit, a typical production wafer may contain as few 20 or 30 ICs or as many as several hundred or even several thousand.

(vi) **Test Cell or Test Lead** – It is different from test plug. It is a special chip repeated only a few times on each wafer.

Q.3. Explain in brief the various steps for wafer processing.

(R.G.P.V., June 2015)

Ans. Wafers are cut from ingots of single-crystal silicon that have been pulled from a crucible melt of pure molten polycrystalline silicon. To provide the crystal with the needed electrical properties some amount of impurities are added to the melt. Seed crystal determines crystal orientation. This seed crystal dipped into the melt to start single crystal growth. Quartz crucible is used to keep the melt, quartz crucible also surrounded by a graphite radiator. Radio frequency induction heats the graphite and the temperature is maintained at a few degrees above the melting point of silicon. The seed is withdrawn vertically from the melt while simultaneously being rotated after the seed is dipped into the melt. The molten polycrystalline silicon melts the tip of the seed, and as it is withdrawn refreezing occurs. It considers the single crystal form of the seed as the melt freezes. This method is continued until the melt is consumed. With the help of seed rotation rate and seed withdrawal rate we can calculate the ingot diameter. Slicing into wafers are usually carried out using internal cutting edge diamond blades. Generally, wafers are between 0.25 mm and 1.0 mm thick, depending on their diameter. At least one face is polished to a flat, scratch free mirror finish following this operation.

Q.4. Define the test plug or process control bar.

Ans. A specific chip which is repeated only a few times on each wafer is known as test plug or process control bar. Process parameters of the technology are monitored by this chip. The validity of the process is verified after processing. If the determination of key parameters at the test plug level are not acceptable, the wafer is discarded.

Q.5. Write down the approaches of IC design.

Ans. Two approaches of IC design are given below –

(i) **Bottom-up Approach** – The designer begins at the transistor or gate level and designs subcircuits of increasing complexity, which are then interconnected to design the required functionality.

(ii) **Top-down Approach** – The designer repeatedly decomposes the system level specifications into groups and subgroups of simpler tasks. The task of lowest level are ultimately implemented in silicon, either with standard circuits and tested or with low-level circuits designed to obtain the required specifications. This method can be used for some digital designs and often results in a significant increase in designer productivity.

Q.6. Give a brief discussion about the size and complexity of integrated circuits.
 (R.G.P.V., Dec. 2015)

Or

Discuss about the size and complexity of integrated circuits.

(R.G.P.V., June 2016)

Or

Give a classification of integrated circuits by device count.

(R.G.P.V., Dec. 2016)

Ans. The classification of integrated circuits based on the number of devices or potential devices used in the design of the circuit and in terms of the feature size of the process. The device count is usually restricted to the number of active devices. Table 1.1 shows the classification of integrated circuit by device count.

Table 1.1

Name of Circuit	Active Device Count	Functions
SSI	1 to 10^2	Gates, op-amps, many linear applications
MSI	10^2 to 10^3	Registers, filters, etc.
LSI	10^3 to 10^5	Microprocessors, A/D, etc.
VLSI	10^5 to 10^6	Memories, computers, signal processors.

Based on feature size, classification is in terms of a usually minimum feature size or pitch. Minimum feature size is often nearly half of the pitch. In otherwords pitch is twice the minimum feature size. The minimum feature size was 7 micro to 10 micro in early 1970 and 5 micro were popular in late 1970 and early 1980. In the end 1980s the minimum feature size had shrunk to under 2 μ , with some groups producing 1 μ and $1\frac{1}{4}$ μ circuits. A sketch of FET is shown in fig. 1.1 for references purposes.

The FET is made of a conductive gate region, that is separated from the surface of the substrate by a very thin insulating layer. The minimum permissible value for L and W is the minimum feature size of this process. For instance, the minimum allowable value of L and W would be 5 micro for five micro

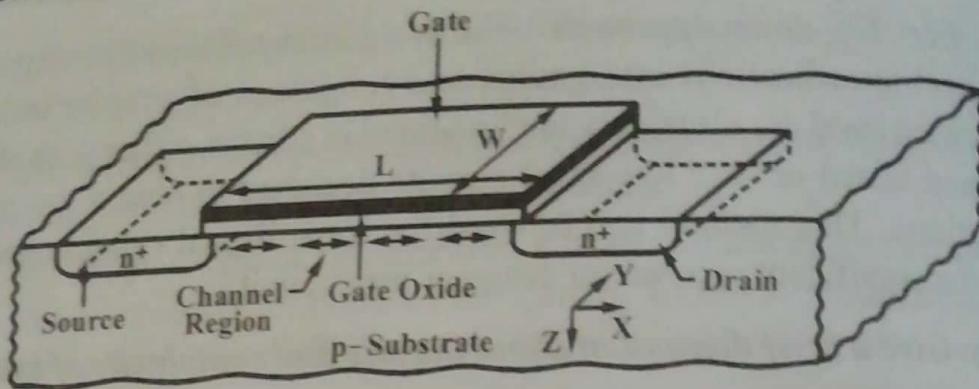


Fig. 1.1 Simplified Three Dimensional View of a FET

process. To get a realistic appreciation of the complexity of existing integrated circuits, an analogy among the features on an integrated circuit and the features on the map of a large city is often drawn. This is motivated by the fact that when a dense integrated circuit is observed under a high power microscope it resembles to a street map of a city and the interconnections corresponds to the city streets. Considering that the pitch of a process maps to one city block, that a city block is 200 metres on a side and the minimum feature size equals half of the pitch, it follows that the magnification factor is $10^8 : x$ where x is the minimum feature size of the process. Many integrated circuit needs a silicon area which is considerably less than the maximum practical chip size.

Q.7. Write short note on microelectronics field.

Or

"Microelectronics field plays a vital role in VLSI designing." Prove this statement with the help of a suitable example. (R.G.P.V., Dec. 2015)

Or

Give a brief introduction on microelectronics field. Give its classification also. (R.G.P.V., June 2016)

Ans. Various types of approaches and processes have found niches in the microelectronics market place. The field of microelectronics is very broad. Types of major processes used in IC fabrication is shown in fig. 1.2.

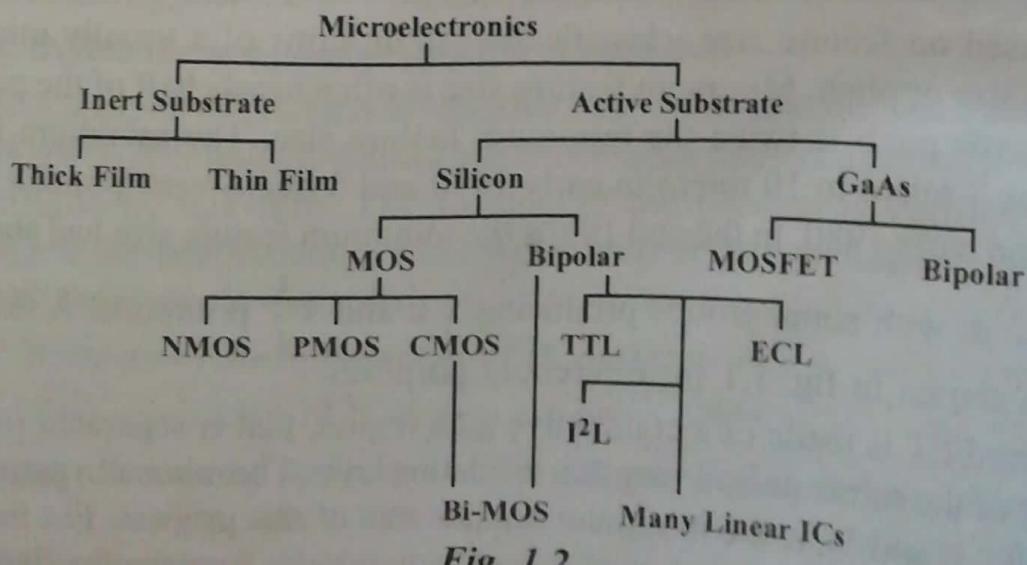


Fig. 1.2

In process types, the first division gets between active and inert substrates. Active substrates are utilized by the high volume integrated circuits. Some of the more demanding needs as well as specific low volume circuits use the inert substrates. Mostly hybrid ICs use inert substrates. Thick and thin film processes which utilize inert substrates are very important. Make good resistors with attractive temperature characteristics these processes are capable. This is hard to get with the standard active substrate processes.

Silicon or doped silicon is active substrate but significant research effort has been expended over the last decade in using GaAs. BJT is the basic active device for bipolar process and MOSFET is the basic active device for MOS processes. In 1960s and early 1970s, bipolar process was very popular. At very high frequency this process give potential for operation and some performance merits like large transconductances, that are of benefit in various linear applications. The types of bipolar process ICs are TTL logic family, I²L and ECL.

NMOS, PMOS and CMOS are the types of MOS process. p-channel and n-channel MOSFETs are the basic devices of MOS processes. MOS process which uses only p-channel FETs is known as PMOS process. The term NMOS refers to a MOS process using only n-channel FETs. Reasonable performance and excellent density, characterize the NMOS process. A MOS process which simultaneously gives both p-channel and n-channel devices is known as CMOS. The presence of both types of FETs offers the designer significant extra flexibility over that attainable with either an PMOS or NMOS process. For most VLSI scale circuits MOS processes are used. Applications include memories, microprocessors, interfacing, basic logic functions and a host of linear and mixed linear and digital applications.

Q.8. Discuss about the recent trends in VLSI Design. How VLSI design will be economical ? Give the major costs associated with wafer processing and fabrication.

(R.G.P.V., Dec. 2016)

Ans. In the production of VLSI circuits, various trends are readily identifiable. The continual shrinking of the minimum geometrical feature size is the most visible. Therefore, the rate at which the minimum feature size reduces is slowing, this trend will continue. In the photolithographic process, this slowing is partially attributable to inherent physical drawbacks and the gradually rising costs related with very fine equipment of resolution processing.

In digital circuits, a trend in increasing speed is readily identifiable. In some applications, GaAs material is attractive due to minimized sensitivity to radiation and due to higher electron mobility. Continual enhancement in the silicon circuits performance increases doubts, although, about if and when a transition to GaAs will take place. The increase in circuit complexity and increase in speed are direct results of the reduction in feature size.

The increasing circuit function complexity and device count on die is a third trend of VLSI design. For ICs, this trend is important for establishment of new markets.

A fourth trend is toward raised productivity of designer and an ever increasing dependence on the computer in the design process. In several current design projects, design techniques which were standard a ten year ago would be completely unworkable.

A fifth trend represents the continual shift of where design, production and markets are geographically located. In the United States and Western Europe, a 10 year ago most and innovative design efforts and a significant part of the production was performed with more mature technologies being moved to the far East. In country, production was normally most profitable in which labour costs were low. In recent years, an increasing shift in the design efforts to the more produced far Eastern countries has taken place in which labor costs remain low, with the mature production shifting more into the less produced far Eastern countries.

A sixth trend represents a increasing coupling of a specific process and its processing equipment. The process is becoming increasingly dependent on the specific performance pieces of equipment.

Other trends comprise the employ of more powerful CAD tools. This trend extends VLSI design to realm of the systems designer.

The field of VLSI design is challenging from both scientific and engineering point of views. Normally, both developmental and research efforts may be focused toward regions in which investments may be recoupled in the market place within a relatively short time. Hence, it is important that the designer is familiar with the IC production economics. The developmental costs will typically dominate on a product which is anticipated to have a relatively small total sales volume. The actual production costs dominate on a product with a large estimated sales volume over the life product life.

The developmental costs are projected once the engineering effort needed to bring a product into production is known. The developmental costs can become quite large for seemingly simple designs. The burden is quite large due to several expenses such as computer time charges, technician support, documentation preparation, applications engineering, equipment amortization, pilot production, test procedure development and mask generation. The burden factor changes from company to company and from project to project. Due to differing project requirements detailed estimates of the specific costs will usually be prepared. Information about design costs within a company is highly proprietary. The production costs of IC are simpler to projected. Major costs associated with wafer processing and fabrication are given in table 1.2. Typical value are given in table 1.3.

	Cost	
	Per Wafer	Per Die
Wafer fabrication		
Blank wafer	x_1 ✓	
Wafer processing	x_2 ✓	
Wafer sawing	x_3 ✓	
Die attach, bonding, and packaging	x_4 ✓	
Packaging	x_5 ✓	
Final test	x_6	✓
	x_7	✓

Table 1.3

Processing Costs		
	4" Process	5" Process
Wafer fabrication		
Blank wafer	$x_1 = \$10$	$x_1 = \$15$
Wafer processing	$x_2 = \$140$	$x_2 = \$150$
Wafer sawing (per wafer)	$x_3 = \$25$	$x_3 = \$40$
Die attach, and bonding (per wafer)	$x_4 = \$3$	$x_4 = \$3$
Packaging	$x_5 = \$3$	$x_5 = \$5$
Final test (per package)	x_6 (see below)	x_6 (see below)
	$x_7 = 30\phi/\text{cm}^2$	$x_7 = 30\phi/\text{cm}^2$
Package Costs		
Plastic DIP	8 pin	\$0.032
Plastic DIP	16 pin	0.048
Plastic DIP	24 pin	0.091
Ceramic side brazed	64 pin	0.70
Ceramic side brazed	16 pin	1.05
Ceramic CERDIP	24 pin	1.50
Ceramic CERDIP	64 pin	4.95
Ceramic pin grid array	16 pin	0.096
Ceramic pin grid array	24 pin	0.26
Ceramic pin grid array	40 pin	0.64
Ceramic pin grid array	68 pin	6.40
Ceramic pin grid array	84 pin	7.50
Ceramic pin grid array	132 pin	10.15
Ceramic pin grid array	224 pin	18.00

Q.9. Draw and explain a block diagram of conventional IC design process. (R.G.P.V., June 2016)

process.

Ans. Fig. 1.3 shows the block diagram of conventional IC design process. A set of design specifications is a starting point. A major effort is necessary to get a complete circuit set and system specifications on complicated designs.

Preliminary designs are based on simple models of devices or cells (subcircuits). These are typically at the component or device level for analog circuits and at the behavioural or logic level for digital circuits. A preliminary computer simulation using much more accurate models may be used to verify the preliminary performance design. Good device and cell (subcircuit) models are essential. If model accurately predicts experimental performance after fabrication, then it is good. During the simulation, a model is sufficiently easy to remove the requirement of excessive computer time. Assumable time is often invested in the preliminary design loop and initial computer simulation.

The actual layout occurs, once the preliminary design is deemed acceptable. The layout phase is commonly entered on cells prior to the completion of preliminary design phase. A good floorplan can be achieved early in the design after a good estimate of the overall architecture and cells size can be achieved. The floorplan contains all cells placement and major busing information as well as input-output pad designations.

After layout and ultimately on the entire circuit, additional computer simulation is undertaken on cells. These simulations are essential because parasitic effects related with the layout play an important role in both analog circuits and digital circuit. In digital circuits, the parasitics normally cause additional unwanted delays or potentially disastrous race conditions whereas in analog circuits, the parasitics tend to degrade performance specifications. If the effects of the parasitics cannot be

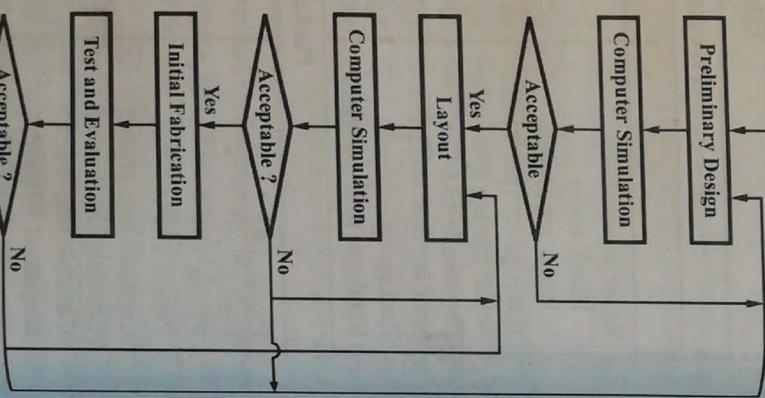


Fig. 1.3 Conventional IC Design Process

resolved with changes in the layout, then the results of the computer simulation commonly necessitate changes in the layout or changes in the design itself.

Following an acceptable computer simulation of the entire circuit, the circuit is committed to fabrication. For complicated designs or evolving processes, cells and test structures are commonly fabricated early in the process of design to give verify functionality and modeling information of cells. Either the circuit is released to production or the suitable step of the design process is re-entered based upon the experimental evaluation.

NUMERICAL PROBLEMS

Prob.1. Assume an op-amp requires an area $100 \text{ mil} \times 100 \text{ mil}$ and a microprocessor requires an area $1 \text{ cm} \times 1 \text{ cm}$. How many of each type of chip can be fabricated on a 5 inch wafer? (R.G.P.V., Dec. 2016)

Sol. Neglecting the area loss on the periphery of the wafer, the number of op-amps and microprocessors can be determined –

$$N_{\text{op-amp}} = \frac{\pi(2.5 \text{ in})^2}{(0.1 \text{ in})^2} = 1963.495 \approx 1963$$

Ans.

$$N_{\mu\text{p}} = \frac{\pi(2.5 \text{ in})^2}{(1 \text{ cm})^2} = 126$$

Ans.

Prob.2. If 1000 devices on a chip must have specific parameter within the specified design process window, determine the soft yield if the process has been characterized by a capability index of –

- (i) $C_p = 0.5$ (ii) $C_p = 1.0$ (iii) $C_p = 1.5$ (iv) $C_p = 2.0$.

(R.G.P.V., Dec. 2016)

$$\text{Sol. (i)} \quad C_p = 0.5$$

The design specification window is given by

$$P = \frac{1}{\sqrt{2\pi}} \int_{-3C_p}^{3C_p} e^{-(x^2/2)} dx = \frac{1}{\sqrt{2\pi}} \int_{-1.5}^{1.5} e^{-(x^2/2)} dx = 0.8664$$

Therefore, the probability that all 1000 devices have a parameter within the design specification window is

$$P_{1000} = (0.8664)^{1000} \\ = 5.229 \times 10^{-63} \approx 0$$

(ii) $C_p = 1.0$

The design specification window is given by

$$P = \frac{1}{\sqrt{2\pi}} \int_{-3\times 1}^{3\times 1} e^{-(x^2/2)} dx = 0.9973$$

Thus, the probability that all 1000 devices have a parameter within the design specification window is

$$P_{1000} = (0.9973)^{1000} = 0.067$$

This represents about a 6.7% yield.

$$(iii) C_p = 1.5$$

The design specification window is given by

$$P = \frac{1}{\sqrt{2\pi}} \int_{-3\times 1.5}^{3\times 1.5} e^{-(x^2/2)} dx = 0.999993$$

and

$$P_{1000} = (0.999993)^{1000} = 0.993$$

This represents about 99.3% yield.

$$(iv) C_p = 2.0$$

$$P = \frac{1}{\sqrt{2\pi}} \int_{-3\times 2}^{3\times 2} e^{-(x^2/2)} dx = 0.99999998$$

and

This representing essentially a 100% yield.

IC PRODUCTION PROCESS, PROCESSING STEPS, PACKAGING AND TESTING

Q.10. Write the major steps involved in producing ICs from qualitative point of view.

Or

Write down all the steps of IC production process. (R.G.P.V., Dec. 2015)

Ans. Major steps involved in producing ICs from qualitative point of view are given below –

- (i) Crystal preparation (ii) Masking
- (iii) Photolithographic process (iv) Deposition
- (v) Etching (vi) Diffusion
- (vii) Conductors and resistors (viii) Oxidation
- (ix) Epitaxy

Q.11. What do you mean by crystal preparation ?

Or

Write down all the steps of crystal preparation of bipolar substrate and MOS integrated circuits.

(R.G.P.V., June 2016)

Ans. A single crystal of silicon which is lightly doped with either p or n type impurities is known as substrate of bipolar and MOS ICs. These crystals are cut from large right circular cylinders of crystalline silicon that are grown upto 2 m and that lies in diameter from 1 to several inches. The thickness of

these slices are 250μ to 400μ . The size of wafers has been growing rapidly with time to permit for both large chips and a larger number of chips per wafer. Four inch wafers are used in older processing lines but in newer lines 5 and 6 inch wafers are used.

Q.12. What is meant by masking ?

Ans. Integrated circuit masks are high-contrast photographic negatives or positives. During the photolithographic process these are used to stop light from striking a photosensitized wafer. The masks are constructed of glass covered with a thin film of opaque metal, but low costly and less durable emulsion masks are sometimes used. Digitized description of the desired mask geometries are responsible for generating masks. There are many methods of producing the masks. Some methods are given below –

- (i) First method uses a laser beam as a pattern generator in a raster scan mode.

Generally, these two methods also need a high resolution step and repeat and/or reduction camera to produce the last masks which will be used.

- (ii) Second method contains photographically reducing large copies of the desired patterns which have been produced with a computer controlled drafting machine.
- (iii) To produce the real patterns directly onto the final masks, electron beam is used in third method. The best quality masks produced by this method but it needs more time and expensive equipment.

Q.13. Discuss the photolithographic process.

Or

Explain the photolithographic process with masking used.

(R.G.P.V., June 2016)

Ans. Viscous liquid is applied in a thin, uniform layer to the whole surface of a wafer following cleaning. Regions of dopants, polysilicon metal and contacts are defined using masks. For instance, in places covered by the mask, ion implantation might not occur or the dielectric or metal layer might be left intact. In areas where the mask is absent, the implantation can occur, or dielectric or metal could be etched away. The patterning is achieved by a process called photolithography, from the Greek photo (light), lithos (stone) and graph (picture), which literally means ‘carving pictures in stone using light’. The primary method for defining areas where we want material to be present or absent on a wafer is by the use of photoresists. The wafer is coated with the photoresist and subjected to selective illumination through the photomask. After the initial patterning of photoresists, other barriers layers such as polycrystalline silicon, silicon dioxide, or silicon nitride can be used as physical masks on the chip.

Q.14. What do you mean by deposition ?

Ans. For most existing semiconductor processes films of different materials should be applied to the wafer during processing. Mostly these films are very thin. Insulators, resistive films, dielectric, n- and p-type semiconductor materials, conductive films and dopants are included in film that are deposited. Deposition methods contain chemical vapour deposition, physical vapour deposition and screen printing.

Evaporating the material is known as evaporation which is to be deposited by controlling the temperature and pressure of the host material environment. If the material condenses then film is formed.

Sputtering contains bombardment of the host material with greater energy ions to dislodge molecules, that will reconnect themselves to the surface of the water.

Chemical vapour deposition is obtained in two ways –

- By pyrolytic decomposition of a single gas, which also frees the desired molecules for reattachment.
- By causing a reaction of two gases near the substrate, a reaction gets that creates solid molecules, that subsequently adhere to the substrate surface.

Q.15. What is meant by etching ?

Ans. Selectively dismissing unnecessary material from the surface of the substrate is known as etching. Masks and photoresist are used to selectively pattern the surface of the substrate. Wet and dry types of etches used in generation. Wet etches is also known as chemical etches. Dry etching, also termed ion etching, is directional and thus much less susceptible to the undesirable horizontal undercutting.

Q.16. Discuss the diffusion process.

Or
Clearly explain various diffusion effects in silicon with emphasis on VLSI application.
(R.G.P.V., Dec. 2017)

Ans. Diffusion is the process of introducing controlled amounts of dopants into semiconductors. Using diffusion, conductivity of silicon is being altered by producing either n-type or p-type region. Selectively producing n-type and p-type regions require that diffusion to be carried out at an elevated temperature and by placing the dopant atoms on the surface of the semiconductor. So we have a high concentration of the dopant at the surface and it gradually decreases as one move inside the semiconductor.

Diffusion is generally carried out in a furnace similar to that used in thermal oxidation, placing the wafers inside it and passing an inert gas that

contains the desired dopant through it at an increased temperature in the range of $800 - 1200^{\circ}\text{C}$.

p-type semiconductor is usually obtained by diffusion of solid, liquid or gaseous source of boron into silicon and n-type semiconductor by diffusion of solid, liquid or gaseous source of arsenic or phosphorous into silicon.

Q.17. What do you mean by conductors and resistors ?

Ans. For interconnection of components on an integrated circuit, aluminium or other metals used as a conductors. If current flow is small then nonmetallic films are mostly used for conductors and interconnections. Example of nonmetallic conductor is polysilicon. This is mostly used for gates of MOSFETs. These polysilicon materials find limited applications as resistors.

Q.18. With neat sketches explain oxidation process in IC fabrication.

(R.G.P.V., Dec. 2017)

Ans. Several structures and manufacturing techniques used to make silicon integrated circuits rely on the properties of the oxide of silicon, which is named silicon dioxide (SiO_2). Hence, the reliable manufacture of SiO_2 is extremely significant.

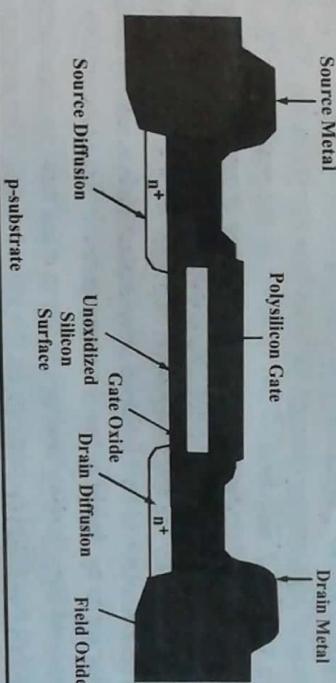


Fig. 1.4 An NMOS Transistor Showing the Growth of Field Oxide below the Silicon Surface

Oxidation of silicon is obtained by heating silicon wafers in an oxidizing atmosphere like oxygen or water vapour. Two common methods are as follows –

(i) Wet Oxidation – This takes place when the oxidizing atmosphere contains water vapour. The temperature is normally between 900°C and 1000°C . This is a quick process.

(ii) Dry Oxidation – This occurs when the oxidizing atmosphere is pure oxygen. Temperatures are in the region of 1200°C , to obtain an acceptable growth rate.

In the oxidation process, silicon is consumed. Because SiO_2 has approximately twice the volume of silicon, the SiO_2 layer grows almost equally

in both vertical directions. This effect is shown in fig. 1.4 for an n-channel MOS device in which the SiO_2 (field oxide) projects above and below the unoxidized silicon surface.

Q.19. Explain the following terms –

- (i) Oxidation
- (ii) Lithography
- (iii) Ion-implantation
- (iv) Epitaxy.

(R.G.P.V., Dec. 2013)

Ans. (i) Oxidation – Refer the ans. of Q.18.

(ii) Lithography – Lithography is the process of transferring patterns of geometric shapes on a mask to a thin layer of radiation sensitive material called resist covering the whole surface of the semiconductor substrate. The patterns define the regions of the integrated circuits that have to be fabricated.

This includes the implantation regions, contact regions, bonding pads etc. These resist patterns are the replicas of circuit elements. These resist patterns are also transferred into the underlying layers where the device is. After transferring the pattern etching is done to remove unmasked portions of the layers.

(iii) Ion-implantation – Ion-implantation is the process of introduction of high energy charged particles into the substrate. The dopant atoms are vaporized, accelerated and targeted at the substrate. The atoms enter the crystal lattice, collide with the substrate atoms, lose energy and come to rest. The distance to which the dopant atoms penetrate depend on their speed. Typically the ion energies lie between 30 and 300 KeV and ion densities between 10^{11} to 10^{16} ions/cm². Ion-implantation is mainly used when small areas are to be doped at lower temperatures.

A beam of ions, having desired charge to mass ratio are accelerated by a voltage and permitted to impinge on the silicon wafer. The surface of the wafer is selectively coated with a beam resist such that the beam energy is adequate to penetrate the target lattice only in the selected regions. The beam is highly directional and little lateral penetration occurs only at the resist edges and which is very low. The dopant dose can be controlled by monitoring the ion current during implantation. The damaged caused to the silicon lattice can be removed by following heat treatment steps called annealing.

(iv) Epitaxy – The word epitaxy is made from two Greek words epi + taxis, i.e., epi means upon and taxis means ordered. Thus growth of thin ordered crystalline layer on a crystalline substrate is called epitaxy. During epitaxy the substrate act as the seed crystal and the crystal can be grown below the melting point. Epitaxy is generally used to enhance the performance of bipolar transistor and other CMOS ICs also.

Q.20. What do you mean by packaging and testing ? Or

(R.G.P.V., June 2015)

Write short note on VLSI testing. because packages vary widely in cost and thermal impedance. Usually the more expensive package for a given number of pins is thermal impedance. The thermal impedance is a measurement which can conduct heat away from

package which can conduct heat away from package selection may be very important because packages vary the die. Processed wafers are sliced into dice (chips) and packaged. Fig. 1.5 shows a 1.5 × 1.5 mm chip in a 40 pin dual-inline package.

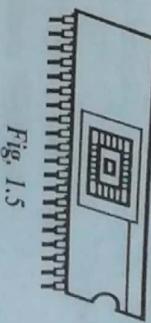


Fig. 1.5

This wire bonded package uses thin gold wires to connect the pads on the die to the lead frame in the center cavity of the package. More advanced packages offer different tradeoff's between cost, pin count, pin bandwidth, power handling, and reliability. Flip-chip technology places small solder balls directly onto the die, eliminating the bond wire inductance and allowing contacts over the entire chip area rather than just at the periphery.

Even tiny defects in a wafer or dust particles can cause a chip to fail. Chips are tested before being sold. Testers capable of handling high speed chips cost millions of dollars, so many chips use built-in self test features to reduce the tester time required.

Q.21. Explain IC production process and what are the methods of testing in detail.

(R.G.P.V., June 2017)

Ans. Refer to the ans. of Q.10, Q.11, Q.12, Q.13, Q.14, Q.15, Q.16, Q.17, Q.18 and Q.20.

Q.22. What is the need of testability in a VLSI design ? Define design for testability.

(R.G.P.V., Dec. 2014)

Ans. Testability – Developed chips are eventually inserted into printed circuit boards or multichip modules for system uses. The correct functionality of the system hinges upon the correct functionality of the chips used. Thus, the fabricated chips must be completely testable to ensure that all the chips passing the specified chip test may be inserted into the system without causing failures, either in packaged or in bare die form. Such a aim requires –

- (i) Generation of good test vectors.
- (ii) Availability of reliable test fixture at speed.
- (iii) Design of testable chip.

Design for Testability – As the number of transistors integrated into a single chip raises, the task of chip testing to ensure correct functionality becomes increasingly more complex. Thus, many chips must be tested within a short

time for timely delivery to consumers in a production environment. Design for testability has become ever more critical to overcome such difficult issues.

The key to designing circuits which are testable are the two concepts that we have introduced known as controllability and observability. Controllability is the ability to set (to 1) and reset (to 0) every node internal to the circuit. Observability is the ability to observe either directly or indirectly the state of any node in the circuit.

Three main techniques are used for design for testability. These are given below –

- Ad-hoc testable design techniques
- Scan based techniques
- Self-test and built-in techniques.

MOS PROCESSES, NMOS PROCESS, CMOS PROCESS, BIOPOLAR TECHNOLOGY, HYBRID TECHNOLOGY, DESIGN RULES AND PROCESS PARAMETERS

Q.23. What are the various bipolar devices ?

Ans. In isolation, the MOS transistor is treated as the device of interest. But, there are other semiconductor devices which are fabricated either parasitically or deliberately in a CMOS process. Particularly, the junction diode and bipolar transistor are important. The former is used primarily in digital circuits as a protection device in I/O structures and the latter can be constructed to improve the speed of CMOS in BiCMOS processes. However, of concern to all CMOS designers are the parasitic bipolar transistors constructed as a by-product of building the basic NMOS/PMOS structures in CMOS, which can lead to a circuit debilitating condition known as latchup.

Q.24. Sketch the schematic symbol for n-channel and p-channel depletion MOSFET and enhancement MOSFET. What is the significant difference between the construction of an enhancement type MOSFET and depletion type MOSFET ?

Ans. Commonly used symbols for n-channel and p-channel depletion MOSFET and enhancement MOSFET are shown in fig. 1.6.

The constructional difference between enhancement type MOSFET and depletion type MOSFET as

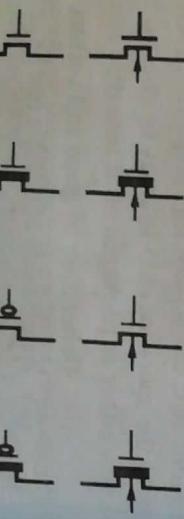
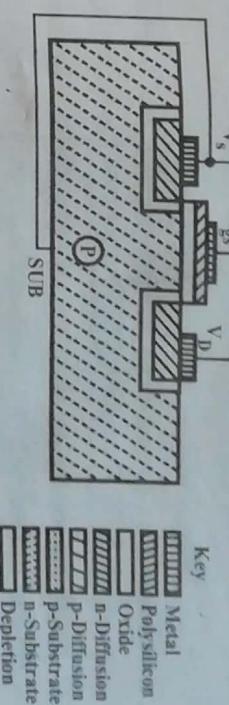


Fig. 1.6 MOS Transistor Circuit Symbols

shown in fig. 1.7, is a non-conducting condition with $V_D = V_S = V_{GS} = 0$. If the gate is connected to a positive voltage with respect to the source, the electric field is established between the gate and the substrate, which induces inversion region in the substrate under the gate insulation and a conduction path or channel is formed between source and drain.



(a) NMOS Enhancement Mode Transistor
(b) NMOS Depletion Mode Transistor

In depletion mode device, the channel is present under the condition $V_{GS} = 0$ by implanting suitable impurities in the region between source and drain during manufacture and prior to depositing the insulation and the gate. In this, source and drain are connected by a conducting channel, but the channel may be closed by applying a suitable negative voltage to the gate.

The conduction characteristics for enhancement and depletion mode MOS transistors are shown in fig. 1.8. The devices that are normally cut-off (i.e. nonconducting) with zero gate bias are called *enhancement mode devices*, whereas those devices that conduct with zero gate bias are called *depletion mode devices*.

n-Channel Enhancement n-Channel Depletion

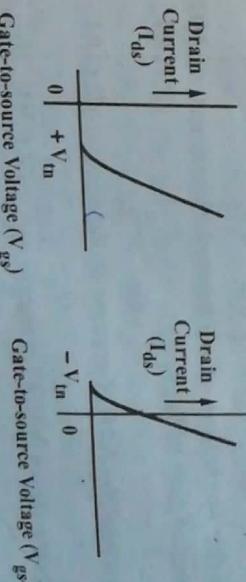


Fig. 1.8 MOS Transistor Characteristics

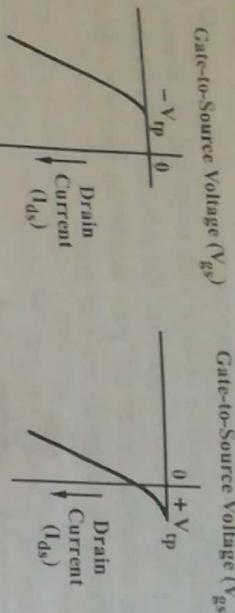


Fig. 1.8 Conduction Characteristics for Enhancement and Depletion Mode MOS Transistors (Assuming Fixed V_{ds})

Q.25. Briefly discuss the physical structure of a PMOS transistor.

Ans. Physical structure of a PMOS transistor is shown in fig. 1.9. A reversal of n-type and p-type regions of NMOS yields a p-channel MOS transistor.

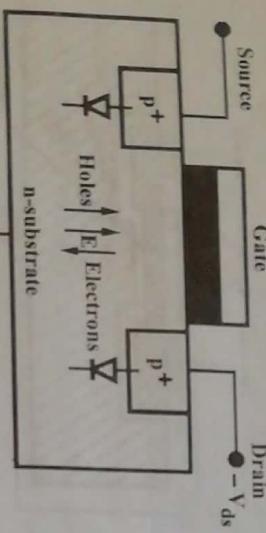


Fig. 1.9 Physical Structure of PMOS Transistor

When a negative gate voltage is applied (with respect to source), it draws holes into the region below the gate, resulting in the channel changing from n-type to p-type. Hence, a conduction path between the source and the drain is formed. However, in this instance, conduction results due to the movement of holes (versus electrons) in the channel. A negative drain voltage sweeps holes from the source through the channel to the drain.

Q.26. Explain the physical structure and operation of an NMOS enhancement transistor.

Or

Explain the operation of n-channel enhancement MOSFET with different values of gate voltage.

(R.G.P.V., Dec. 2013)

Explain about the NMOS process in details.

Or

(R.G.P.V., Dec. 2015)

Write short note on NMOS process.

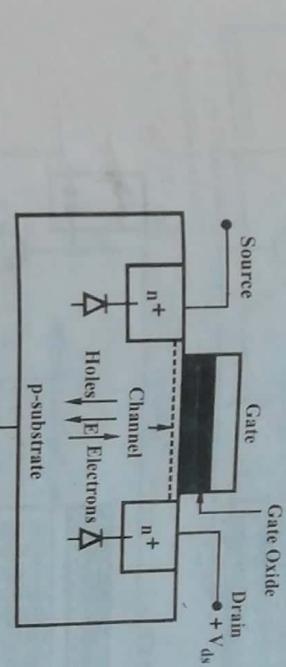


Fig. 1.10 Physical Structure of an NMOS Enhancement Transistor

The D.C. current from the gate to channel is essentially zero, because the oxide layer is an insulator. There is no physical distinction between the drain and source regions due to the inherent symmetry of the structure. The application of high gate fields is possible because SiO_2 has relatively low loss and high dielectric strength.

In operation, a positive gate voltage is given between the source and the drain (V_{ds}). When gate bias is zero (i.e., $V_{gs} = 0$), current does not flow from source to drain since they are effectively insulated from each other by the two reversed biased pn-junctions illustrated in fig. 1.10. But, when a voltage, which is positive with respect to the source and the substrate, is applied to the gate then it generates an electric field E across the substrate which attracts electrons toward the gate and repels holes. In case when gate voltage is sufficiently large, the region under the gate alters from p-type to n-type and gives a conductive path between the source and the drain. Under such a condition, the surface of the underlying p-type silicon is called inverted.

Fig. 1.11 shows the initial distribution of mobile positive holes in a p-type silicon substrate of an MOS structure for a voltage, V_{gs} , much less than a threshold voltage, V_t , that is the threshold voltage. This mode is referred to as accumulation mode. When V_{gs} becomes greater than V_t , the holes are repelled causing a depletion region under the gate. This is termed as depletion mode as shown in fig. 1.11 (b). If V_{gs} is further increased above V_t , this results in electrons being attracted to the region of the substrate under the gate. A

Ans. Fig. 1.10 shows the physical structure of an NMOS enhancement transistor, which consists of a moderately doped p-type silicon substrate into which two heavily doped n⁺ regions, the source and drain, are diffused. A narrow region of p-type substrate exists between these two regions, which is known as channel. This channel is covered by a thin insulating layer of silicon dioxide (SiO_2) called gate oxide. There is a polycrystalline silicon electrode over this oxide layer, which is referred to as gate.

conductive layer of electrons gives rise to the name inversion mode in the p-substrate, as shown in fig. 1.11 (c).

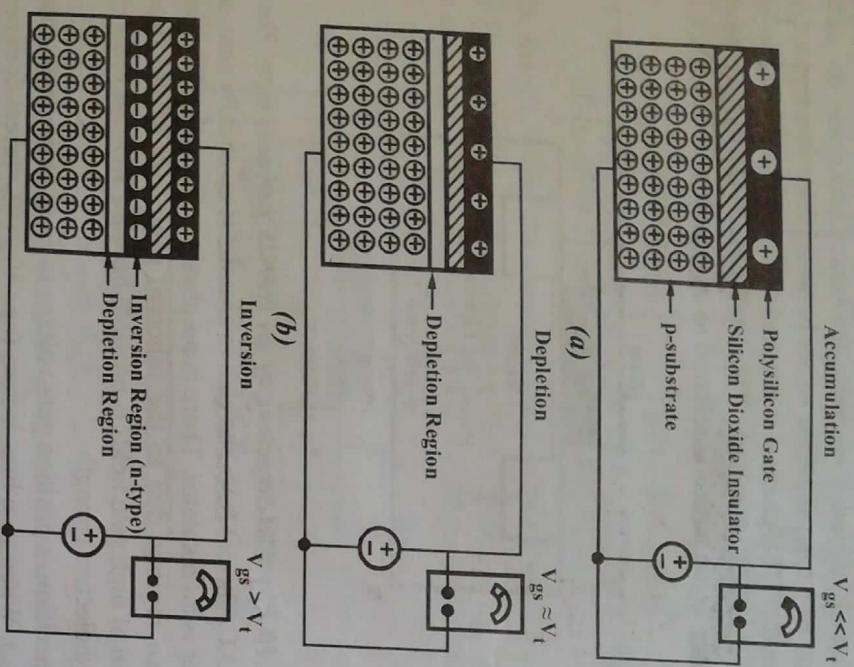


Fig. 1.11 Accumulation, Depletion and Inversion Modes in NMOS Structure

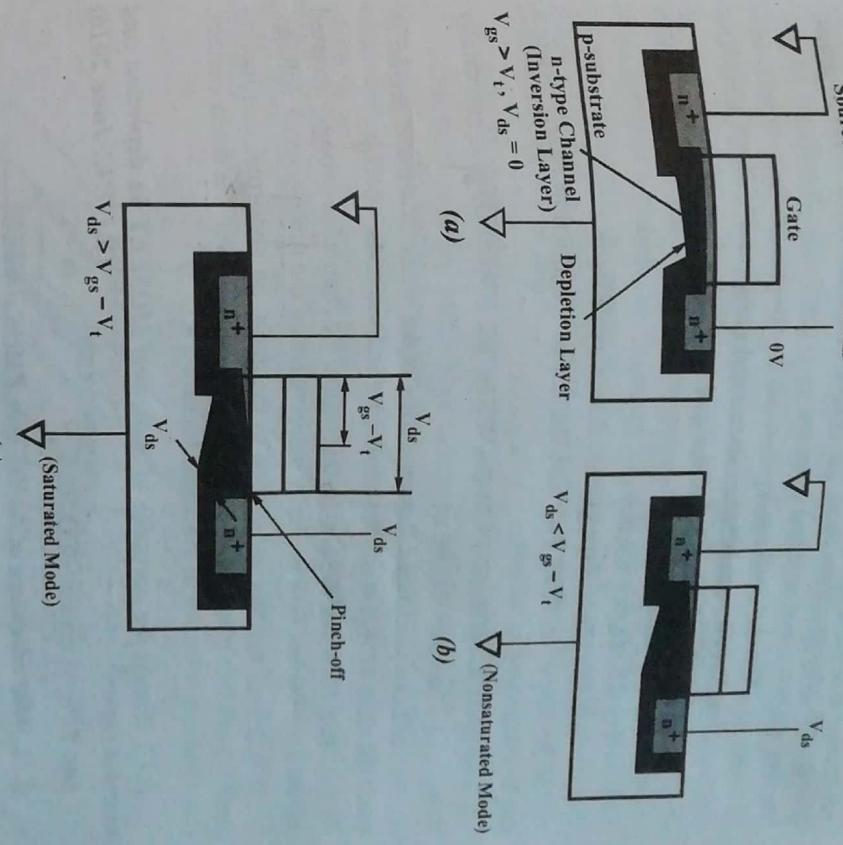
An MOS device acts like a voltage-controlled switch which conducts initially if the gate-to-source voltage, V_{gs} is equal to the threshold voltage, V_T . If a voltage V_{ds} is given between source and drain, with $V_{gs} = V_b$, the horizontal and vertical components of the electrical field because of the source-drain voltage and gate-to-substrate voltage interact, leading conduction to take place along the channel. Sweeping of the electrons in the channel from the source toward the drain is the responsibility of the horizontal component of the electric field associated with the drain-to-source voltage (that is, $V_{ds} > 0$).

When voltage from drain to source is raised, the resistive drop along the channel starts to change the shape of the channel characteristic. This is shown in fig. 1.12. The full gate voltage is effective in inverting the channel at the source end of the channel. But, at the drain end of the channel, only the difference between the gate and drain voltages is effective.

Fig. 1.12 NMOS Device Behaviour affecting by the Different Terminal Voltages

If the effective gate voltage ($V_{gs} - V$) is larger as compared to the drain voltage, then channel becomes deeper as V_{gs} is increased. This is referred to as the linear, resistive, non-saturated or unsaturated region, in which the channel current I_{ds} is a function of both gate and drain voltages. When V_{ds} is greater than effective gate voltage, $V_{gd} < V_t$, and the channel becomes pinched-off, i.e., channel no longer reaches the drain. This is shown in fig. 1.12 (c).

In such a case, conduction is brought about by a drift mechanism of electron under the effect of the positive drain voltage. When electrons leave the channel, they are injected into the drain depletion region and are subsequently accelerated toward the drain. As a result, the voltage across the pinched-off channel tends to stay fixed at $(V_{gs} - V_t)$. In this condition, the channel current is controlled by the gate voltage and is almost independent of the drain voltage. This condition is termed as saturated state. In the case when drain-to-source



voltage and gate voltage are fixed, the factors which affect the level of drain current flowing between source and drain are –

- Threshold voltage V_t
- The distance between source and drain
- Dielectric constant of the gate insulator
- The channel width
- The carrier mobility μ
- Thickness of the gate-insulating oxide layer.

In the case of an MOS transistor, the normal conduction characteristics can be categorized as follows –

- Cut-off Region** – In this region, the current flow is essentially zero.
- Non-saturated Region** – This is the weak inversion region in which the drain current is dependent on gate and the drain voltage.

(iii) Saturated Region

In this region, the channel is strongly inverted and the drain current flow is ideally independent of the drain-source voltage. If very high voltages are applied to the drain, an abnormal conduction condition can take place in which gate has no control over the drain current. This condition is known as avalanche breakdown.

Q.27. Discuss the operation of n-channel MOSFET in depletion and inversion region.

Ans. Refer to the ans. of Q.26.

Q.28. Write advantage of NMOS over PMOS devices.

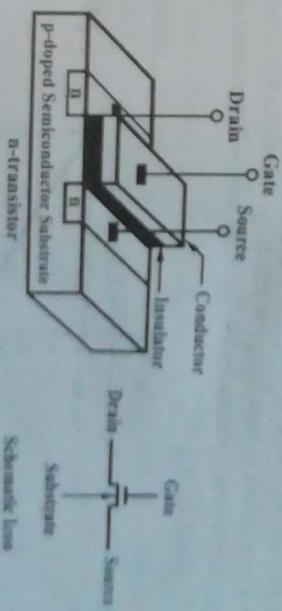
Ans. The p-channel enhancement FET is very popular in MOS systems because its production is much easier as compared to the n-channel device. In MOS fabrication, most of the contaminants are mobile ions that are positively charged and are trapped in the oxide layer between gate and substrate. In an n-channel enhancement device, the gate is generally positive with respect to the substrate and thus, the positively charged contaminants collect along the interface between the SiO_2 and the silicon substrate. The positive charge from this layer of ions attracts free electrons in the channel that tends to make the transistor turn on prematurely. In p-channel devices, the positive contaminant ions are pulled to the opposite side of the oxide layer (to the aluminium- SiO_2 interface) by the negative gate voltage and therefore they cannot influence the channel.

In silicon, at normal field intensities, the hole mobility is approximately $500 \text{ cm}^2/\text{V}\cdot\text{s}$ while electron mobility is about $1300 \text{ cm}^2/\text{V}\cdot\text{s}$. Hence, the p-channel device will have more than twice the ON resistance of an equivalent n-channel of the same geometry and under the same operating conditions. It

means that the p-channel device must have more than twice the area of the n-channel device to obtain the same resistance more than twice than area of the n-channel device to obtain the same resistance. Hence, n-channel MOS circuits can be smaller for the same complexity as compared to p-channel MOS circuits. The higher packing density of the n-channel MOS also makes it faster in switching applications owing to the smaller junction areas. The operating speed is limited primarily by the internal RC time constants and the capacitance is directly proportional to the junction cross-sections. Due to all the above reasons, it is clear that n-channel MOS circuits are more advantageous than p-channel circuits. However, the more extensive process control required for p-channel fabrication makes them expensive and unable to compete economically with p-channel devices at this time.

Q.29. Describe the two types of MOS transistors used in CMOS technology.

Ans. In the CMOS technology, two types of transistors are used – an n-type transistor (n-MOS) and a p-type transistor (p-MOS). Fabrication of these which is rich in holes. When fabrication steps have been performed, a typical MOS structure includes distinct layers called diffusion, polysilicon and aluminium separated by insulating layers.



(R.G.P.V., June 2016)

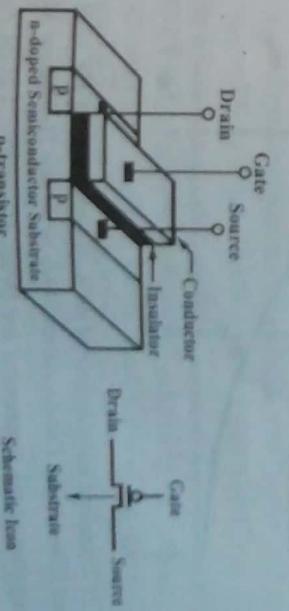


Fig. 1.13 Architecture of MOS Transistors and their Schematic Icons

Fig. 1.13 shows the physical structures for the two types of MOS transistors. The structure of n-transistor has a section of p-type silicon (called

the substrate) separating two areas of n-type silicon. This structure is formed by using a chemical process which changes selected areas in the positive substrate into negative regions rich in electrons. The area which separates the n regions, is capped with a sandwich consisting of silicon dioxide and a conducting electrode, known as the gate. In the same way, the structure of the p-transistor consists of a section of n-type silicon separating two p-type areas. The p-transistor also has a gate electrode in common with the n-transistor.

The transistors have two additional connections, designated the source and the drain, these being formed by the n diffused regions. Gate is a control input, which affects the flow of electrical current between the source and the drain. Actually, the drain and source can be seen as two switched terminals which are interchangeable.

Q.30. Draw and explain ideal I-V characteristics of MOS transistor.

Or
Draw the transfer characteristics of MOSFET and derive the expression for drain current.

Ans. Fig. 1.14 shows the transfer characteristics of n-channel MOSFET. The depletion and enhancement regions, corresponding to V_{gs} negative and positive, respectively, should be noted. The manufacturer sometimes indicates the gate-source cut-off voltage $V_{gs,off}$ at which I_{ds} is reduced to some specified negligible value at a recommended V_{ds} . This gate voltage corresponds to pinch-off voltage V_p of a JFET.

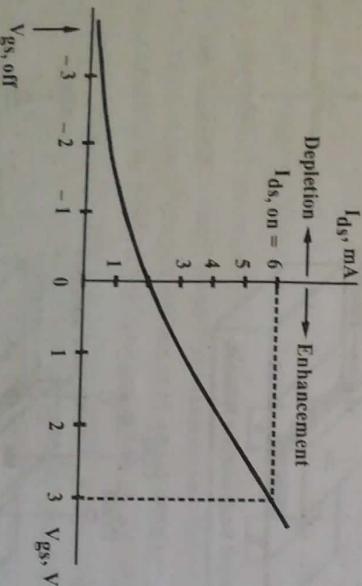


Fig. 1.14 Transfer Characteristic of an n-channel MOSFET that can be

Used Either in the Enhancement Mode or in the Depletion Mode

Derivation of the Expression for Drain Current – Let us consider a voltage V_{gs} which is applied between gate and source with $V_{gs} > V_t$ to induce a channel. In addition, we assume that a voltage V_{ds} is applied between drain and source. First we consider operation in the triode region, for which the

channel must be continuous and hence V_{gd} must be greater than V_t or

equivalently, $V_{ds} < V_{gs} - V_t$. In such a case, the channel will have the tapered shape depicted in fig. 1.15.

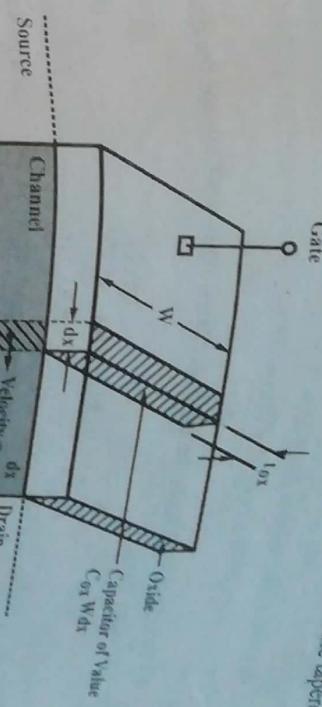


Fig. 1.15 Derivation of the I_{ds} – V_{ds} Characteristic of the NMOS Transistor

We know that in the MOSFET, the gate and the channel region form a parallel-plate capacitor for which the oxide layer acts as a dielectric. If the capacitance per unit gate area is represented by C_{ox} and the thickness of the oxide layer is t_{ox} , then we obtain,

$$C_{ox} = \frac{\epsilon_0}{t_{ox}} \quad \dots(i)$$

where, ϵ_0 = Permittivity of the silicon dioxide
 $\epsilon_0 = 3.9 \times 8.854 \times 10^{-12} = 3.45 \times 10^{-11} \text{ F/m}$.

Oxide thickness t_{ox} is obtained by the process technology used to fabricate the MOSFET. Now, refer to fig. 1.15 and consider the infinitesimal strip of the gate at distance x from the source. Capacitance of this strip is $C_{ox} W dx$. To determine the charge stored on this infinitesimal strip of the gate capacitance, we multiply the capacitance by the effective voltage between the gate and the channel at point x , where the effective voltage is the voltage which is responsible for inducing the channel at point x and is hence $[V_{gs} - V(x) - V_t]$ where $V(x)$ is the voltage in the channel at point x . It follows that the electron charge dq in the infinitesimal part of the channel at point x is obtained as,

$$dq = -C_{ox} (W dx) [V_{gs} - V(x) - V_t] \quad \dots(ii)$$

where the leading negative sign indicates that dq is a negative charge.

Voltage V_{ds} generates an electric field along the channel in the negative x direction.

At point x , this field is given as,

$$E(x) = -\frac{dV(x)}{dx}$$

Electric field $E(x)$ leads the electron charge dq to drift toward the drain with a velocity dx/dt ,

$$\frac{dx}{dt} = -\mu_n E(x) = \mu_n \frac{dV(x)}{dx} \quad \dots(iii)$$

where, μ_n , called the surface mobility, is the mobility of electrons in the channel. It is a physical parameter whose value is dependent upon the fabrication process technology. The resulting drift current I can be given as follows –

$$I = \frac{dq}{dt} = \frac{dq}{dx} \cdot \frac{dx}{dt}$$

Substituting for the charge-per-unit-length dq/dx from equation (ii) and for the electron drift velocity dx/dt from equation (iii) yields,

$$I = -\mu_n C_{ox} W [V_{gs} - V(x) - V_t] \frac{dV(x)}{dx}$$

Although evaluated at a particular point in the channel, the current I must be constant at all points along the channel. Hence, I must be equal to the source-to-drain current. The drain-to-source current is given as,

$$I_{ds} = -I = \mu_n C_{ox} W [V_{gs} - V(x) - V_t] \frac{dV(x)}{dx}$$

that can be arranged in the form,

$$I_{ds} dx = \mu_n C_{ox} W [V_{gs} - V_t - V(x)] dV(x)$$

Integrating both sides of this equation from $x = 0$ to $x = L$ and correspondingly, for $V(0) = 0$ to $V(L) = V_{ds}$, we obtain,

$$\int_0^L I_{ds} dx = \int_0^{V_{ds}} \mu_n C_{ox} W [V_{gs} - V_t - V(x)] dV(x)$$

$$I_{ds} = (\mu_n C_{ox}) \left(\frac{W}{L} \right) \left[(V_{gs} - V_t) V_{ds} - \frac{1}{2} V_{ds}^2 \right] \dots(iv)$$

This is the expression for the drain current in the triode region. The value of the current at the edge of the triode region, or equivalently, at the starting of the saturation region can be found by substituting, $V_{ds} = V_{gs} - V_t$,

$$I_{ds} = \frac{1}{2} (\mu_n C_{ox}) \left(\frac{W}{L} \right) (V_{gs} - V_t)^2 \quad \dots(v)$$

This is the expression of drain current in the saturation region.

In the expressions in equations (iv) and (v), $\mu_n C_{ox}$ is a constant obtained by the process technology used to fabricate the n-channel MOSFET. It is called the process transconductance parameter. It determines the value of the MOSFET transconductance, denoted by k'_n , and has the dimensions of A/V^2 .

$$k'_n = \mu_n C_{ox}$$

In fact, the equations (iv) and (v) can be written in terms of k'_n as follows –

$$I_{ds} = k'_n \frac{W}{L} \left[(V_{gs} - V_t) V_{ds} - \frac{1}{2} V_{ds}^2 \right] \quad (\text{Triode Region})$$

$$I_{ds} = \frac{1}{2} k'_n \frac{W}{L} (V_{gs} - V_t)^2 \quad (\text{Saturation Region})$$

Thus, the drain current is proportional to the ratio of the channel width W and the channel length L , called the aspect ratio of the MOSFET.

Q.31. Discuss about the bipolar process in detail. (R.G.R.V, Dec 2013)

Chemically and polished treated wafers ready for use in the manufacturing process are provided to design engineer by industries. By using the batch processing technique, we have to fabricate in this wafer transistors of the structure shown in the fig. 1.16.

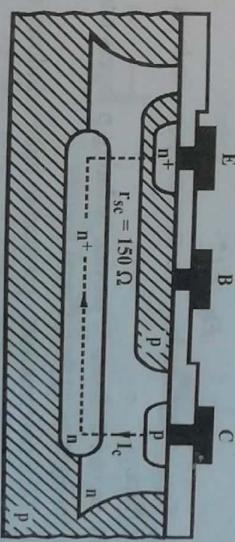


Fig. 1.16

The sequence of steps is given below –

- Total oxidation of the wafer.
- First photomasking operation to define windows in the oxide for the diffusion of buried n⁺ layers.
- First diffusion to grow buried n⁺ layers as shown in fig. 1.17 (a), using the diffusant arsenic or antimony.
- Etching of the oxide from the entire surface.
- Growing of an n epitaxial layer, in which process the buried n⁺ layer diffuses a little both into the substrate and into the epilayer.
- Total oxidation.

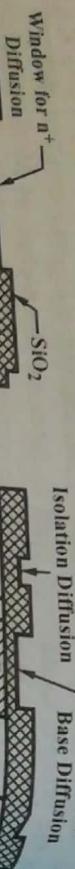


Fig. 1.17

(vii) Second photomasking operation to open windows in the oxide for isolation diffusions.

(viii) Second diffusion to provide isolating p layers and isolated n islands in the epi-layer, using the diffusant boron.

(ix) Third photomasking operation to open windows in the oxide for base diffusion.

(x) Third diffusion to grow base p layers [see fig. 1.17 (b)], using the diffusant boron. The diffusion involves two stages predeposition and drive-in.

(xi) Fourth photomasking operation to open windows in the oxide for emitter diffusion and ohmic contacts of the collectors.

(xii) Fourth diffusion to grow n⁺ layers, using the diffusant phosphorous. The diffusion here is sometimes of the two stage type too. Emitter diffusion is shown in fig. 1.17 (c).

(xiii) Fifth photomasking operation to define windows in the oxide for ohmic contacts.

(xiv) Total deposition of aluminium film onto the wafer as shown in fig. 1.17 (d).

(xv) Sixth photomasking operation to open windows in the photoresist for the interconnection pattern.

(xvi) Etching of the aluminium film through the photoresist mask and removal of the remaining photoresist. Fig. 1.17 (e) shows the etching step.

(xvii) Thermal treatment for firing of aluminium into silicon.

Q.32. Explain the structure and V/I characteristics of an npn bipolar transistor and write expressions for the collector current, emitter current, base current and gain.

Ans. An npn bipolar transistor can be constructed by building an npn diffusion sandwich as shown in fig. 1.18 (a). Likewise, a pnp transistor can be constructed by sandwiching an n diffusion between the two p diffusions. The terminals of a bipolar transistor are known as collector, base and emitter. For an npn transistor, the behaviour of the transistor can be modeled by the structure shown in fig. 1.18 (b).

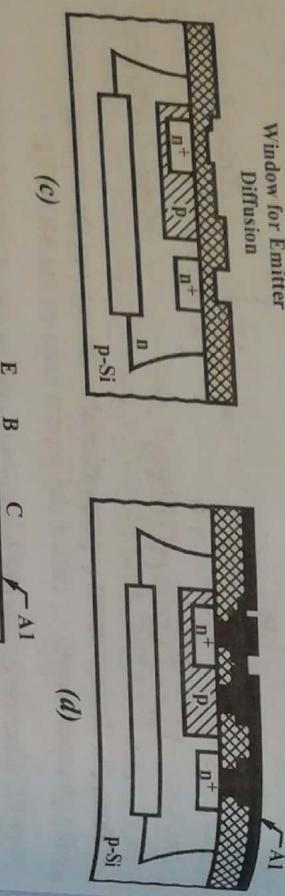


Fig. 1.18 Structure and Model of an npn Bipolar Transistor

By using the Ebers-Moll model, the collector current can be given as -

$$I_c = I_s \left(e^{\frac{qV_{be}}{mkt}} - 1 \right) \left(1 + \frac{V_{ce}}{V_A} \right)$$

While the emitter current is expressed as -

$$I_e = I_c \left(1 + \frac{1}{\beta \left(1 + \frac{V_{ce}}{V_A} \right)} \right)$$

where, $kT/q = 0.026$ (at 300°K)
 $V_{ce} =$ The collector-emitter voltage
 $V_{be} =$ The base-emitter voltage
 $m =$ A constant between 1 and 2
 $V_A =$ The early voltage (an approximation to permit for non-ideal phenomena which result in finite output conductance)

$\beta =$ Forward current gain
 $I_s =$ The junction saturation current.

Forward current gain, β , typically ranges from 20-500.
 $I_b = \frac{V_{in} - V_{be}}{R_b}$

where, $V_{in} =$ Input voltage
 $V_{be} =$ Base emitter voltage ($\sim 0.7\text{ V}$).
 $I_c = \beta I_b$

Thus, the collector voltage is given as -

$$V_{out} = V_{DD} - I_c R_c = V_{DD} - \beta \left[\frac{V_{in} - V_{be}}{R_b} \right] R_c$$

Gain A , is expressed as -

$$\frac{dV_{out}}{dV_{in}} = \frac{\beta R_c}{R_b}$$

An n-well CMOS process inherently has a pnp transistor which is generated between the substrate (collector), well (base), and source/drain diffusions (emitter). This pnp transistor is not that useful except for application as a current reference. Since the transistor is formed by the vertical stacking of junctions, this transistor is a vertical pnp.

To construct more useful npn transistors, extra processing steps must be added to CMOS processes. These steps result in what is termed a BiCMOS process (for bipolar and CMOS). Similar to the case of p-and n-channel transistors in CMOS, npn bipolar transistors have much higher gain and better frequency as compared to pnp transistors. Hence, BiCMOS processes concentrate on adding a high-performance npn transistor.

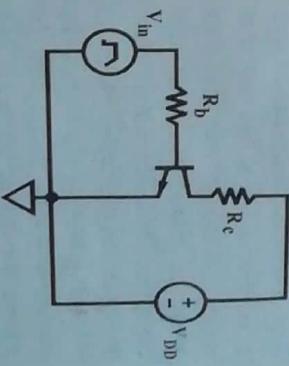


Fig. 1.19 Inverter Using an NPN Transistor

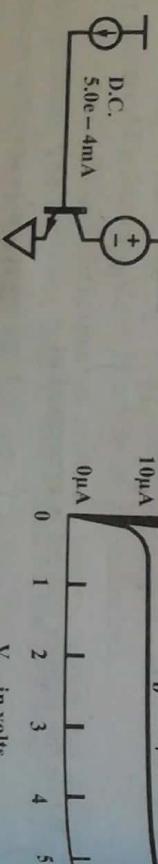


Fig. 1.19 Inverter Using an NPN Transistor

Fig. 1.18 shows the V/I characteristics of a typical npn transistor. The basic design equations for use with digital bipolar circuits are described in

association with the inverter shown in fig. 1.19, in which the collector of an npn transistor is connected to a positive supply via resistor R_c . Base is connected via resistor R_b to an input voltage V_{in} . The base current I_b is expressed as -

$$I_b = \frac{V_{in} - V_{be}}{R_b}$$

where, $V_{in} =$ Input voltage
 $V_{be} =$ Base emitter voltage ($\sim 0.7\text{ V}$).
 $I_c = \beta I_b$

The collector current is expressed as -

Thus, the collector voltage is given as -

$$V_{out} = V_{DD} - I_c R_c = V_{DD} - \beta \left[\frac{V_{in} - V_{be}}{R_b} \right] R_c$$

Gain A , is expressed as -

$$\frac{dV_{out}}{dV_{in}} = \frac{\beta R_c}{R_b}$$

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To construct more useful npn transistors, extra processing steps must be added to CMOS processes. These steps result in what is termed a BiCMOS process (for bipolar and CMOS). Similar to the case of p-and n-channel transistors in CMOS, npn bipolar transistors have much higher gain and better frequency as compared to pnp transistors. Hence, BiCMOS processes concentrate on adding a high-performance npn transistor.

Q.3.3. What do you mean by hybrid technology? Describe the thick film and thin film circuits.
(R.G.P.V., Dec. 2013)

Ans. The combination of two or more integrated circuit dies, along with few discrete components in some cases, in a single package to form what is called a hybrid integrated circuit. Monolithic structures are cheaper than hybrid integrated circuit. The passive components thin film and thick film have reasonable tolerances, are simply trimmable, have acceptable temperature

coefficients which can be tailored to tracking, and give reasonable tradeoff between area needed and component values. The technology of thick film thin film is given below.

The film and hybrid ICs are divided into thick film and thin film depending on the technology of manufacturing. The fabrication of thick film hybrid ICs is simple. Different layers of various inks are deposited on insulating substrate of size of few square centimetres. In thick film IC, desired thickness of film is obtained at once. Conductive pastes provide interconnections, capacitor plates and contact pads for connection of elements to case leads, or pins. Resistive paste resistors and dielectric pastes ensure insulation between capacitor plates and protection in general of the surface of the ready HIC. Every layer of paste should be fixed configuration or pattern. The paste is applied to insulating substrate via the windows of a stencil screen or mask for depositing every layer of film, which defines the pattern for the desired film. The local deposition method of paste on substrate is shown in fig. 1.21.

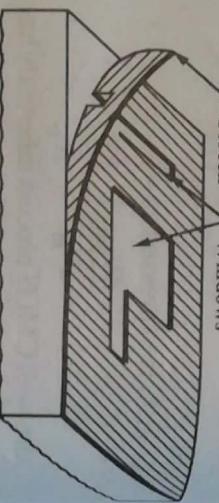


Fig. 1.21

After the passive circuit on the substrate is completed the next step follows that contains bonding of discrete components to the reserved areas or to the protective dielectric layer and connection of their leads to contact pads formed in conductive layers. On the other hand, thin film HICs necessitate more complex technology than thick film hybrid integrated circuits. The thin film deposition process needs particular tooling and equipment, that are rather expensive. Thick-film ICs are cheaper than thin film ICs. In comparison to the deposition of thick-films the growth of thin films to the final thickness proceeds gradually, one monomolecular layer over the other. The next film follows, now from the gaseous phase of different chemical composition to achieve the desired electrical and physical properties. The procedure of depositing film in this fashion ensures the consecutive growth of conductive, resistive and dielectric layers. A metal mask placed on substrate defines the pattern for each film layer. Fig. 1.22 shows the deposition of thin film layers.

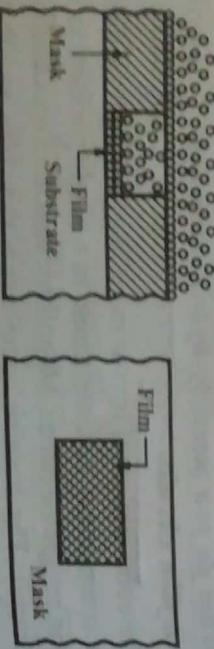


Fig. 1.22

Q.34. Write down the features of thick film ICs.

- (i) The mechanical method of deposition has small tolerances on the ratings of resistors and capacitors, i.e. cannot produce precision elements.

(ii) The deposition process in this method is done mechanically, that does not allow fabrication of films less than 10 to 20 μm in thickness, that this, it is named thick film technology and thick film hybrid integrated circuits.

(iii) Since, the thick film technology is simpler, so the thick film HICs are easily available and are cheaper.

Q.35. Write down the features of thin film ICs.

Ans. The various features of thin film ICs are as follows –

- (i) The capacitors and resistors of high precision values are formed in thin film integrated circuits.
- (ii) The deposition of film over one micrometre in thickness, requires much time, since the rate of deposition of thin film is very less. Also, the deposited films over 1 or 2 μm thick is easily peeled off.
- (iii) A low rate of film growth permits easy control of film thickness, ensuring close tolerances on the values of resistors and capacitors.

Q.36. Write any five differences between the bipolar technology and hybrid technology.

(R.G.P.V., Dec. 2015, June 2017)

Ans. An npn transistor is the basic element of a bipolar IC; the whole production cycle is tailored to make this element. The other elements are made where ever possible at the same time as the transistor. Resistors are formed at the same time as the base region and hence grown to same depth as base. Class of bipolar ICs depends on alternate doping of a semiconductor substrate with donor and acceptor impurities to form within the body of the substrate.

An IC with some discrete elements or a combination of two or more IC types is known as hybrid IC. In hybrid ICs various layers of various inks are deposited on an insulating substrate of size of few square centimetres.

Q.37. What do you understand by layout design rules? Explain their function.

Ans. Layout rules are also known as design rules. These rules can be considered as a prescription for preparing the photomasks used in the fabrication of integrated circuits. The rules provide an essential communication link between circuit designer and process engineer during the manufacturing phase. The main objective associated with layout rules is to achieve a circuit with optimum yield in small area as possible without compromising reliability of the circuit.

Design rules represent the best possible compromise between performance and yield. The more conservative the rules are, the more likely it is that the circuit will function. But, the more aggressive the rules are, the greater the probability of improvements in circuit performance. This improvement can be at the cost of yield.

Design rules specify to the designer certain geometric constraints on the layout artwork so that the patterns on the processed wafer will preserve the topology and geometry of the designs. Design rules do not denote some hard boundary between correct and incorrect fabrication. Rather, they denote a tolerance which ensures very high probability of correct fabrication and subsequent operation.

In a process, two sets of design-rule constraints relate to line widths and interlayer registration. When the line widths are made too small, it is possible for the line to become discontinuous, hence leading to an open circuit wire. If the wires are placed too close to one another, it is possible for them to merge together; that is, shorts can take place between two independent circuit nets. In addition, the spacing between two independent layers may be influenced by the vertical topology of a process.

Design rules primarily address two issues –

- The geometrical reproduction of features that can be reproduced by the mask-making and lithographical process.
- The interactions between different layers.

Several approaches can be taken in describing the design rules, which include 'micron' rules stated at some micron resolution and lambda(λ)-based rules. Micron design rules are usually given as a list of minimum feature sizes and spacings for all the masks required in a given process. The lambda-based design rules popularized by Mead and Conway are based on a single parameter, λ . It characterizes the linear feature – the resolution of the complete wafer implementation process – and allows first-order scaling. As a rule, they can be represented on a single page.

There is some minimum grid dimension in terms of which the design rules are expressed. This is a result of the economic reality that eventually the mask has to be built and the higher the lithographic tolerance, the higher the cost of the mask.

Q.38. Write briefly the layout design rules followed in fabrication of CMOS devices.

Q.

(R.G.P.V., June 2017)

Explain the various CMOS design rules.

(R.G.P.V., June 2015)

Ans. A version of n-well rules are described based on the MOSIS CMOS Scalable rules and compare those with the rules for a hypothetical (but

realistic) commercial 1μ CMOS process. These are given in table 1.4. The MOSIS rules are expressed in terms of λ . These rules permit some degree of scaling between processes as, in principle, we only require to minimise the value of λ and the designs will be valid in the next process down in size. Industry usually uses the actual micron-design rules down in size terms of these dimensions, or uses symbolic layout systems to target the design rules exactly.

Table 1.4 CMOS Layout Rules

A. N-well layer		λ Rule	λ/μ Rule (0.5μ)	μ Rule
A.1	Minimum size	10λ	5μ	2μ
A.2	Minimum spacing (wells at same potential)	6λ	3μ	2μ
A.3	Minimum spacing (wells at different potentials)	8λ	4μ	2μ
B. Active Area				
B.1	Minimum size	3λ	1.5μ	1μ
B.2	Minimum spacing	3λ	1.5μ	1μ
B.3	N-well overlap of p ⁺	5λ	2.5μ	1μ
B.4	N-well overlap of n ⁺	3λ	1.5μ	1μ
B.5	N-well space to n ⁺	5λ	2.5μ	5μ
B.6	N-well space to p ⁺	3λ	1.5μ	3μ
C. Poly 1				
C.1	Minimum size	2λ	1μ	1μ
C.2	Minimum spacing	2λ	1μ	1μ
C.3	Spacing to Active	1λ	0.5μ	0.5μ
C.4	Gate Extension	2λ	1μ	1μ
D. p-plus/n-plus (p ⁺ , n ⁺ for short)				
D.1	Minimum overlap of Active	2λ	1μ	1μ
D.2	Minimum size	7λ	3.5μ	3μ
D.3	Minimum overlap of Active in abutting contact	1λ	0.5μ	2μ
D.4	Spacing of p ⁺ /n ⁺ to n ⁺ /p ⁺ gate	3λ	1.5μ	1.5μ

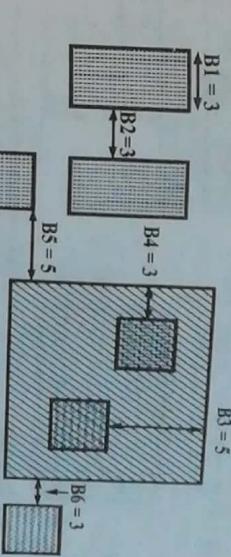
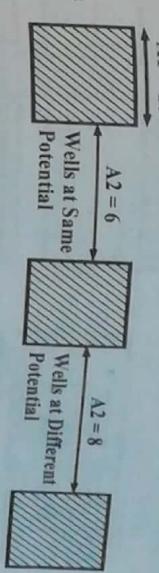
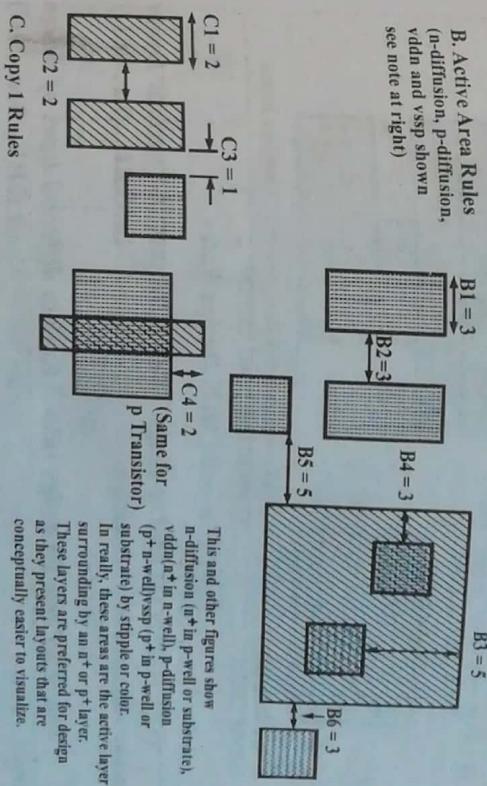
For each mask needed in a process one requires to know whether it is "light field" or "dark field", whether light will pass through the mask to expose a photolithographic pattern or whether light will be blocked by the mask. Furthermore, biases are added or subtracted from the drawn dimensions of the mask to allow for varying types of processing. Contacts might be shrunk as etching tends to make them larger during processing. The rules in table I.4 are illustrated in fig. 1.23 (and in Plate 2).

E. Contact		2λ	1μ	0.75μ
E.1 Minimum size		2λ	1μ	1μ
E.2 Minimum spacing (Poly)		2λ	1μ	0.75μ
E.3 Minimum spacing (Active)		2λ	1μ	0.5μ
E.4 Minimum overlap of Active		2λ	1μ	0.5μ
E.5 Minimum overlap of Poly		1λ	0.5μ	0.5μ
E.6 Minimum overlap of Metal 1		2λ	1μ	1μ
E.7 Minimum spacing to Gate		2λ	1μ	1μ
F. Metal 1		3λ	1.5μ	1μ
F.1 Minimum size		3λ	1.5μ	1μ
F.2 Minimum spacing		3λ	1.5μ	1μ
G. Via		2λ	1μ	0.75μ
G.1 Minimum size		3λ	1.5μ	1.5μ
G.2 Minimum spacing		1λ	0.5μ	0.5μ
G.3 Minimum Metal overlap		1λ	0.5μ	0.5μ
G.4 Minimum Metal2 overlap		1λ	0.5μ	0.5μ
H. Metal 2		3λ	1.5μ	1μ
H.1 Minimum size		4λ	2μ	1μ
H.2 Minimum spacing		3λ	1.5μ	1.5μ
I. Via 2		2λ	1μ	1μ
I.1 Minimum size		2λ	1μ	1μ
I.2 Minimum spacing		3λ	1.5μ	1.5μ
J. Metal 3		8λ	4μ	4μ
J.1 Minimum size		5λ	2.5μ	2.5μ
J.2 Minimum spacing		2λ	1μ	1μ
J.3 Minimum Metal 2 overlap		1μ	1μ	1μ
J.4 Minimum Metal 3 overlap		1μ	1μ	1μ
K. Passivation		100μ	100μ	150μ
K.1 Minimum opening		150μ	150μ	
K.2 Minimum spacing				

The rules are defined in terms of -

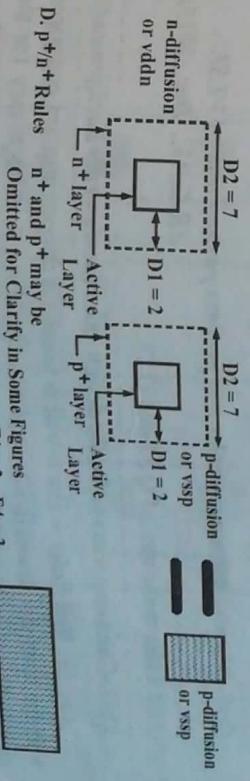
- (i) Feature sizes
- (ii) Separations and overlaps.

In addition to the rules stated above, there are various spacing rules for the periphery of the chip which frequently depend on the vendor (e.g., spacing of all layers to die boundary is 20-50μ).



D. p⁺/n⁺ Rules
n⁺ and p⁺ may be omitted for clarity in some figures

E1 = 2 E2 = 2 E3 = 2 E4 = 2 E5 = 2 E6 = 2 E7 = 2 E8 = 2



boundary. It is necessary to thoroughly ground the well, because the n-well sheet resistance can be several k Ω s per square. This will prevent excessive voltage drops due to substrate currents.

(ii) Transistor Rules –

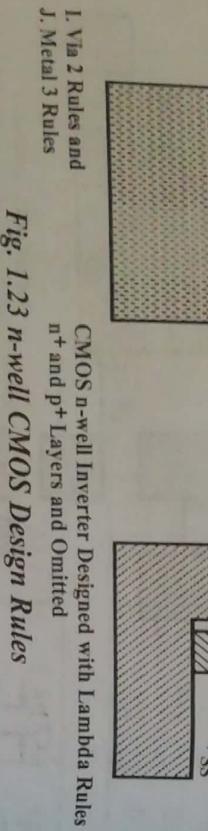
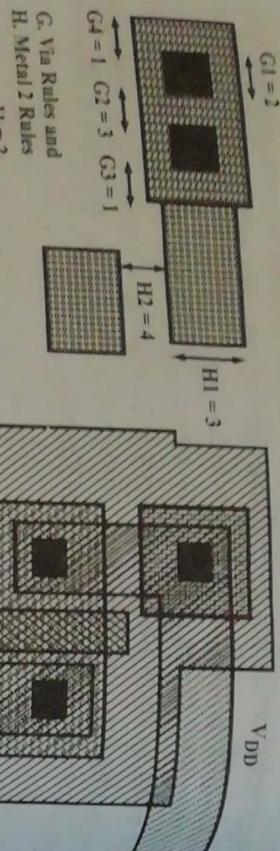


Fig. 1.23 n-well CMOS Design Rules

Q.39. What is the need of design rules? Discuss the various layout design rules for CMOS IC design.

Or

What is the need for design rules? Explain different types of design rules.

Ans. Refer to the ans. of Q.37 and Q.38.

Q.40. Describe the various rules and process parameters of VLSI.
(R.G.P.V., Dec. 2015)

Ans. Refer to the ans. of Q.37 and Q.38.

Q.41. Give some reasons for the design rules (design rule background).

Ans. (i) Well Rules – The n-well is usually a deeper implant compared with the transistor source/drain implants, therefore it is necessary for the outside dimension to provide sufficient clearance between the n-well edges and the adjacent n⁺ diffusions.

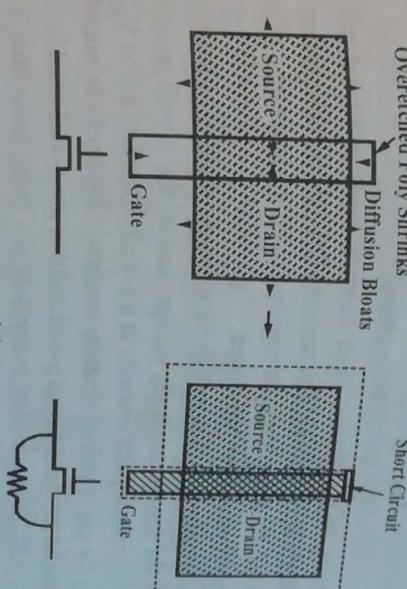
The inside clearance is determined by the transition of the field oxide across the well boundary. Some processes that use STI may permit zero inside clearance, but problems such as the 'birds-beak' effect usually prevent this. To avoid a shorted condition, active is not permitted to cross a well

drain diffusion is masked by the poly region. The source, drain and channel cross active, otherwise the transistor that has been created will be shorted by a diffused path between source and drain. To ensure this condition is satisfied, often termed the "gate extension". This effect is shown in fig. 1.24 (a) where the diffusion has increased in size and the poly has been overetched, resulting in a short. The thin oxide must extend beyond the poly gate so that diffused

As Drawn

As Processed

Short Circuit



Mask Misalignment
Drastically Changes Width of Device and Sometimes Completely Eliminates it

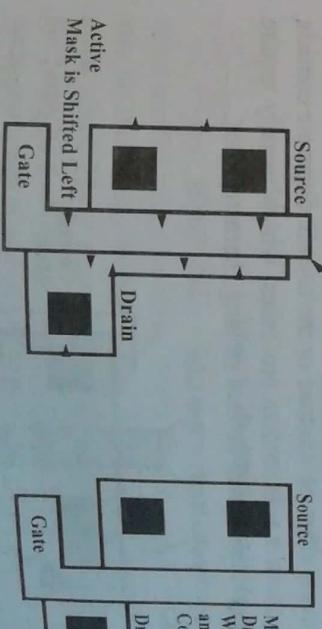


Fig. 1.24 Effects of Insufficient Gate Extension and Source-drain Extension

regions exist to carry charge into and out of channel [fig. 1.24 (b)]. Poly active regions that do not meet intentionally to form a transistor should be kept separated. Both types of transistors have an active region (diffusion or implant) and a poly-silicon region. A p-device has an n-well region surrounding it. Thin oxide areas that are not covered by n are p⁺ and hence are p-devices or wires (within the n-well). Therefore a transistor is n-channel if it is inside an n⁺ region; otherwise it is a p-channel device.

(iii) Contact Rules – There are several generally available contacts.

- (a) Metal to p-active (p-diffusion)
- (b) Metal to n-active (n-diffusion)
- (c) Metal to polysilicon
- (d) V_{DD} and V_{SS} substrate contacts
- (e) Split (substrate contacts).

Depending on the process, other contacts such as buried polysilicon, active contacts may be allowed. This contact allows direct connection between polysilicon and the active transistor region. Sometimes this type of contact is allowed to only one type of active area.

Since the substrate is divided into "well" regions, each isolated well must be "tied" to the appropriate supply voltage; that is, the n-well must be tied to V_{DD} and the substrate (what amounts to a p-well) must be tied to V_{SS}. This is achieved by the use of well or substrate contacts. One needs to note that every p-device must be surrounded by an n-well and that the n-well must be connected to V_{DD} via a V_{DD} contact. Also, every n-device must have access to a V_{SS} contact. The split or merged contact is equivalent to two separate metal-diffusion contacts that are strapped together with metal (fig. 1.25). This structure is used to tie transistor sources to either the substrate or the n-well. Separate contacts are shown; this is consistent with modern processes, which usually require uniform contact sizes to achieve well-defined etching characteristics.

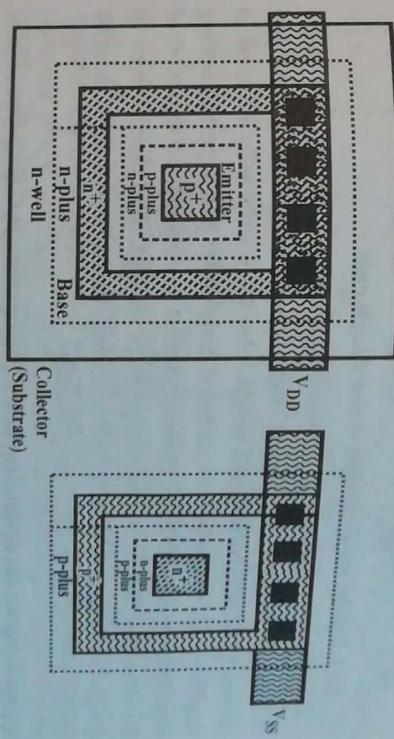


Fig. 1.26 Guard Rings

(v) Metal Rules – Metal spacings may vary with the width of the metal line (so-called fat-metal rules). That is, at some width, the metal spacing may be increased. This is due to etch characteristics of small versus large metal wires. There may also be maximum-metal-width rules. Additionally, there may be rules that are applied to long closely spaced parallel metal lines.

Some processes require a certain portion of the chip area to be covered with metal, and in such cases metal might have to be added to chip "white space". These rules usually relate to constraints imposed by manufacturability requirements.

Merged contact structures in older processes may have used an elongated contact rectangle (fig. 1.25). The V_{SS} or V_{DD} merged contacts may have been used to collect injected minority carriers. If they are implemented in a structure, then n⁺ guard rings must be tied to V_{DD}, while p⁺ guard rings must be tied to V_{SS}. A p⁺ diffusion with n⁺ guard ring is shown in fig. 1.26 (a), while an n⁺ diffusion with p⁺ guard ring is shown in fig. 1.26 (b).

Different well-enclosure rules may apply for guard-ring structures. The structure shown in fig. 1.26 (a) is also that for a pnp transistor if one was required. The transistor terminals have been marked. The area of the center p⁺ region is the area of the emitter. The base is the n-well and is connected via the n⁺ ring. The collector is substrate.

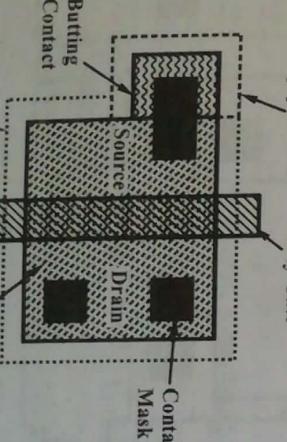
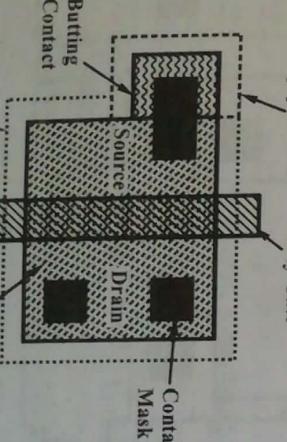
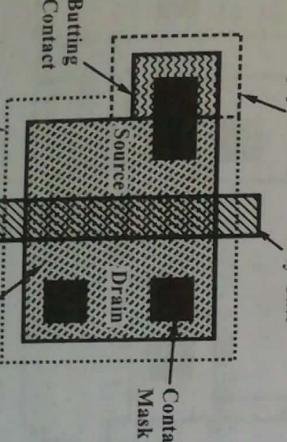
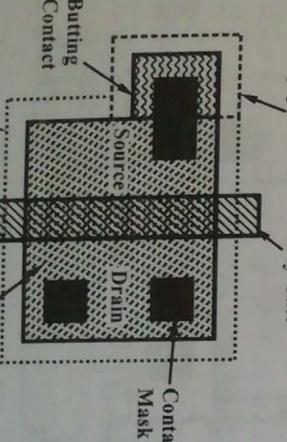
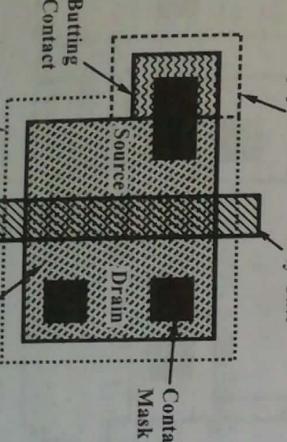
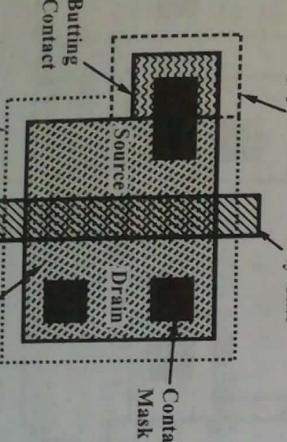
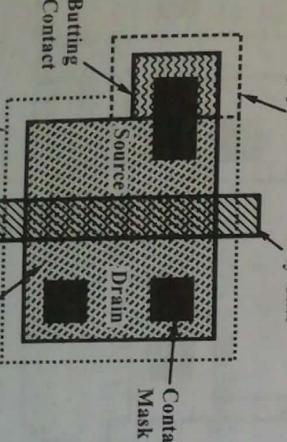
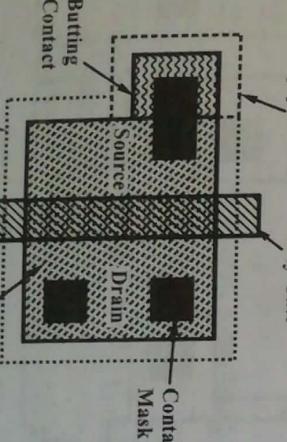
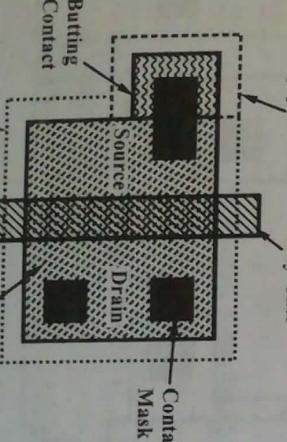
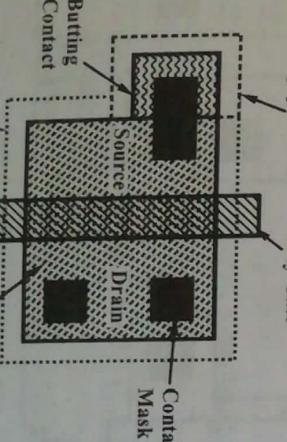
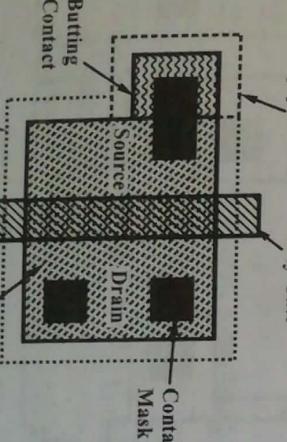
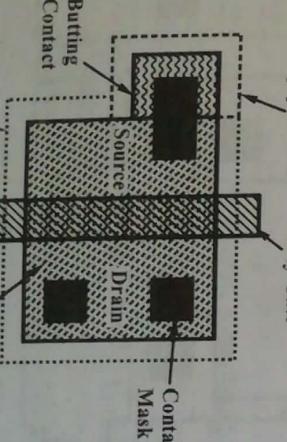
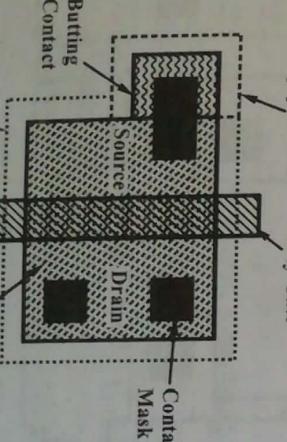
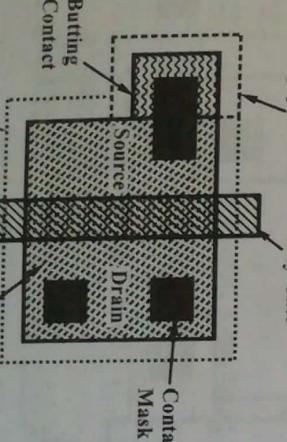
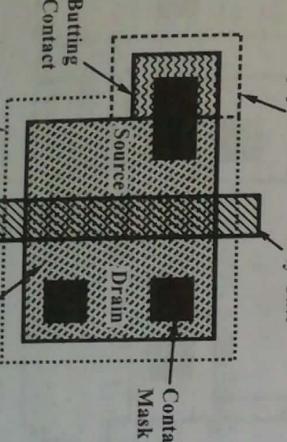
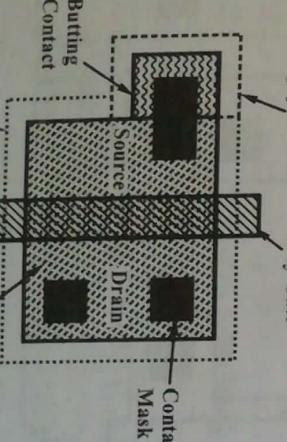
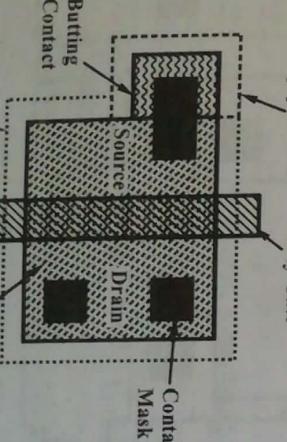
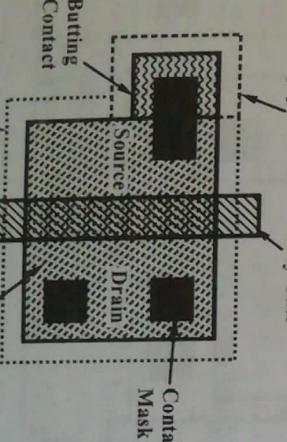
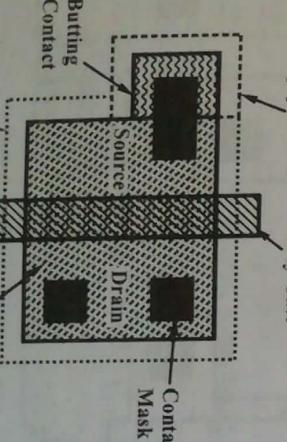
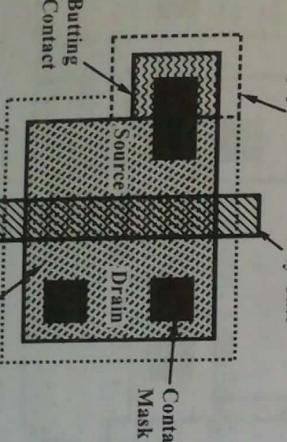
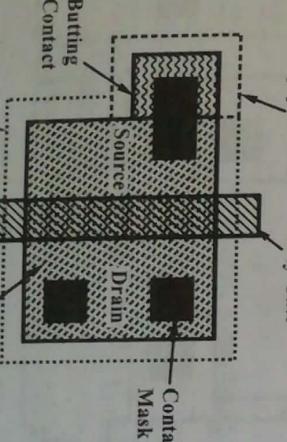
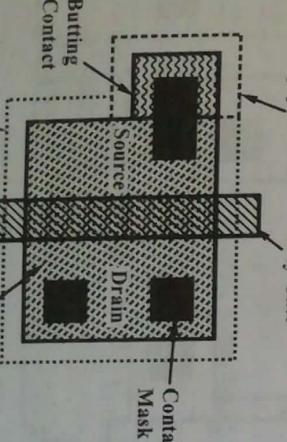
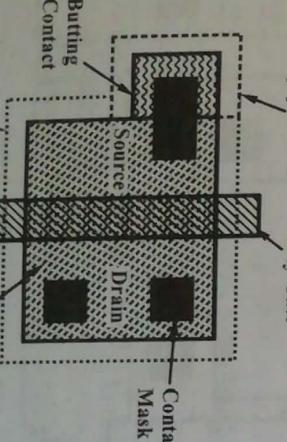
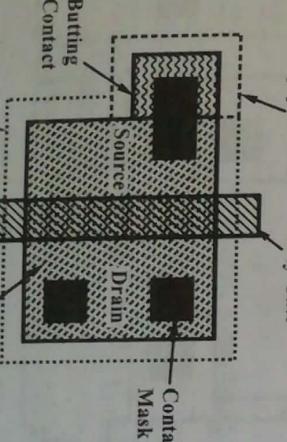
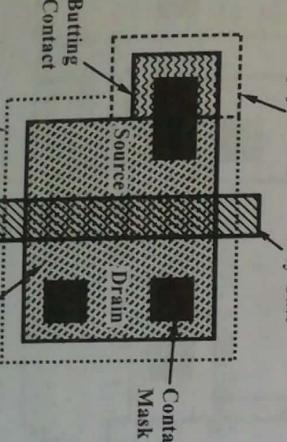
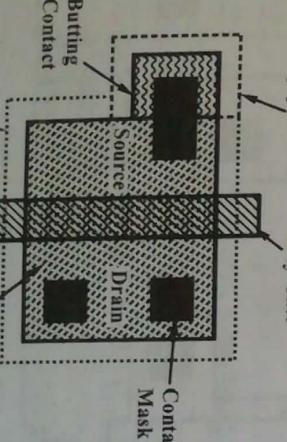
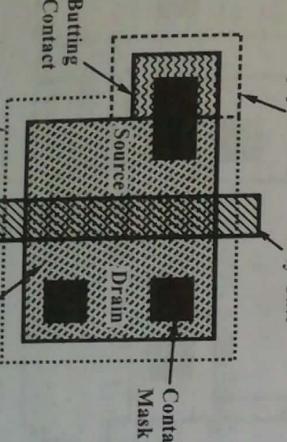
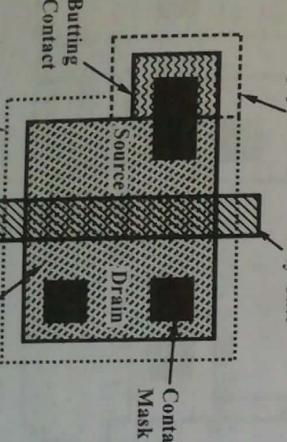
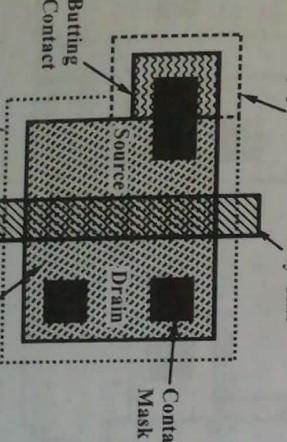
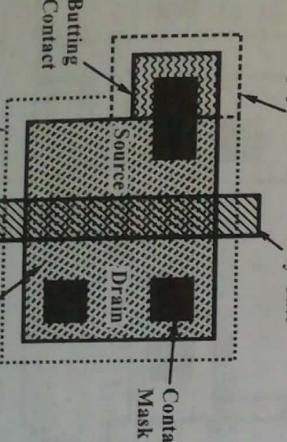
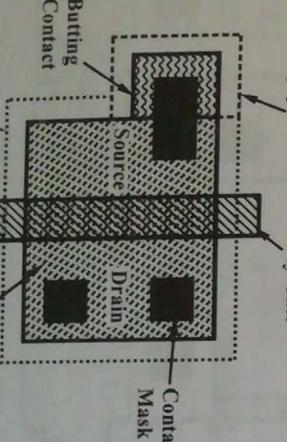
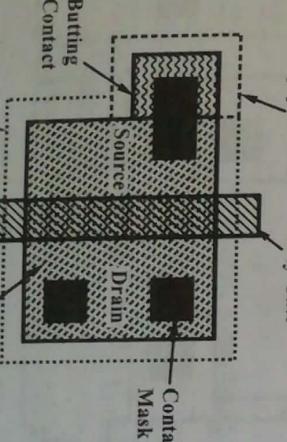
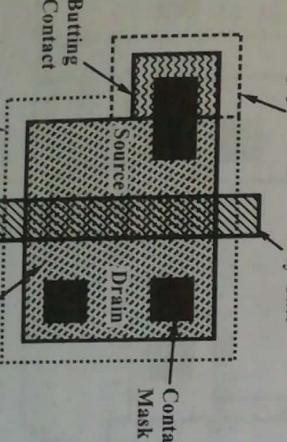
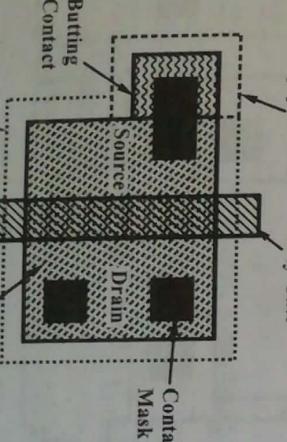
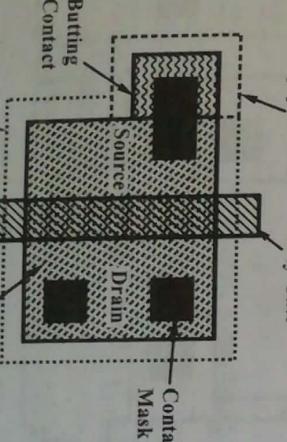
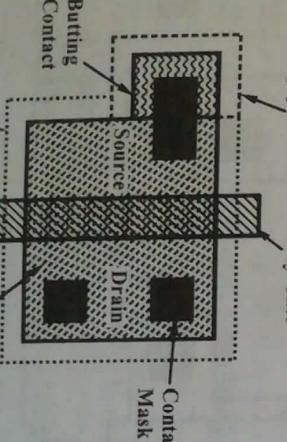
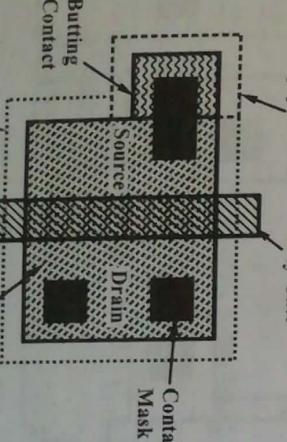
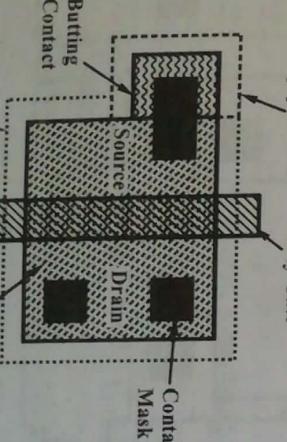
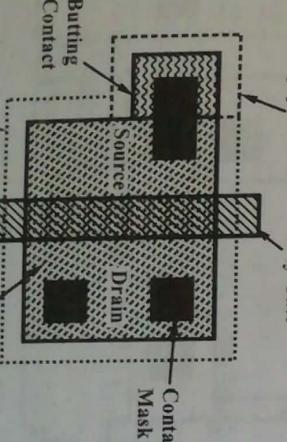
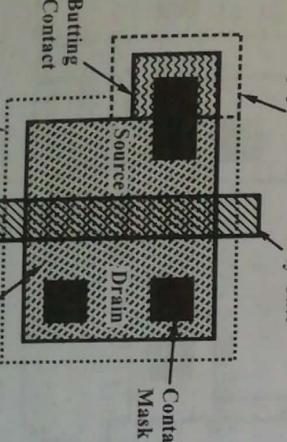
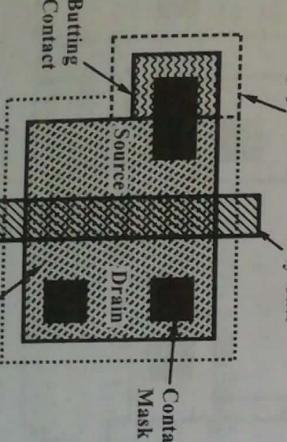
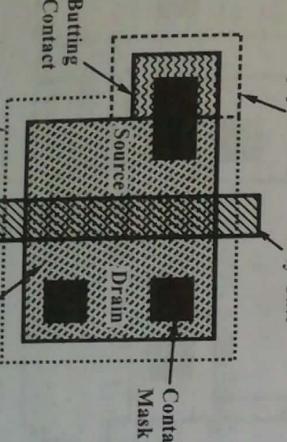
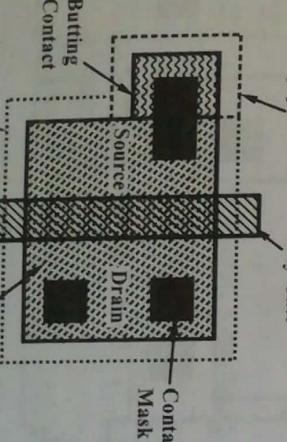
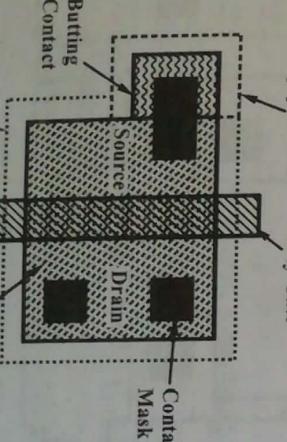
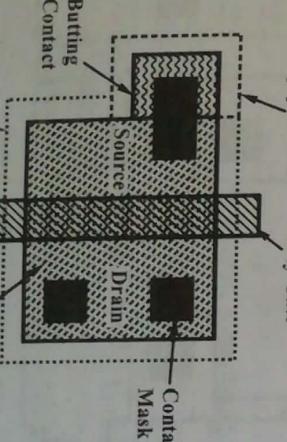
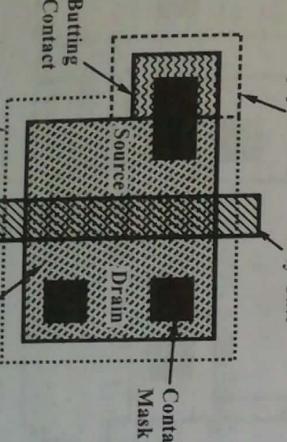
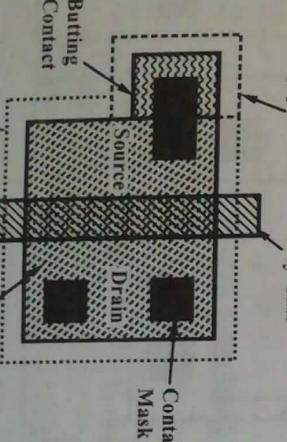
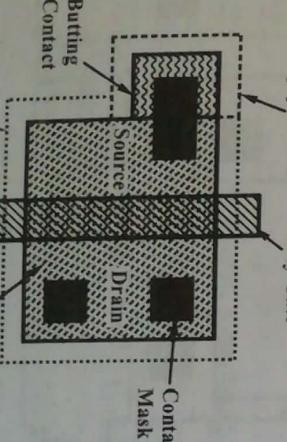
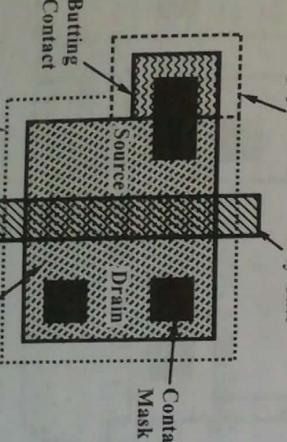
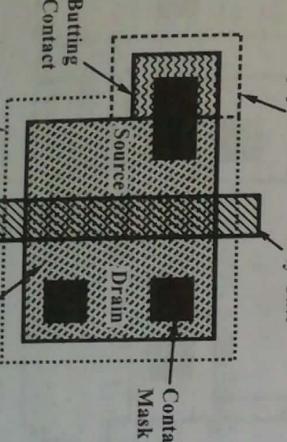
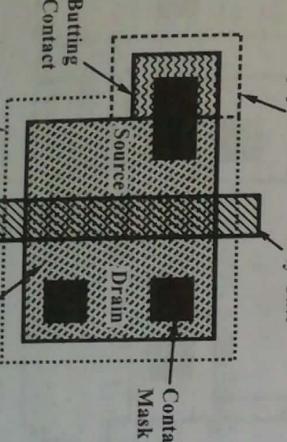
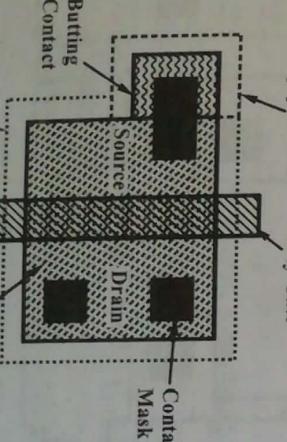
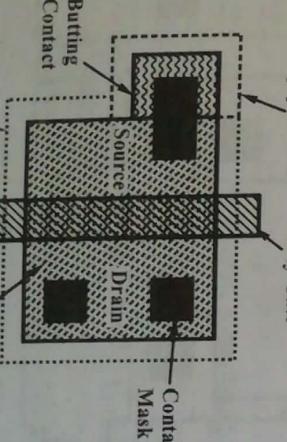
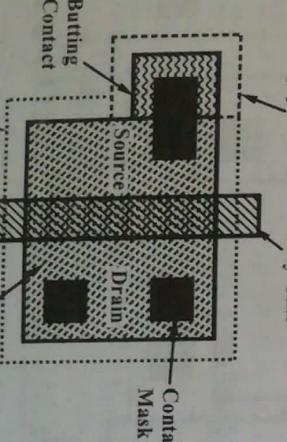
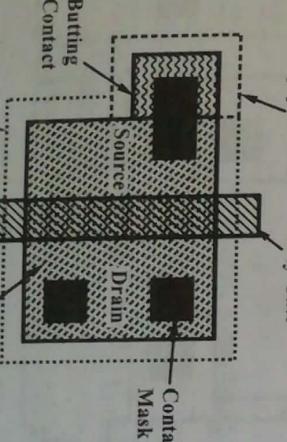
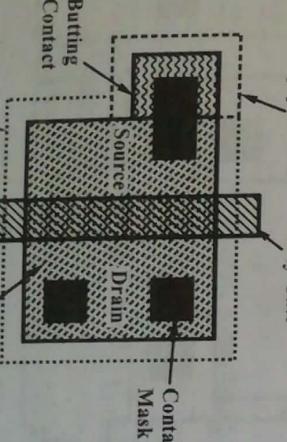
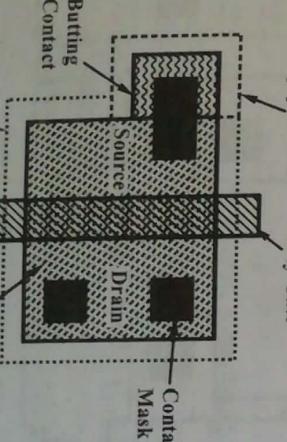
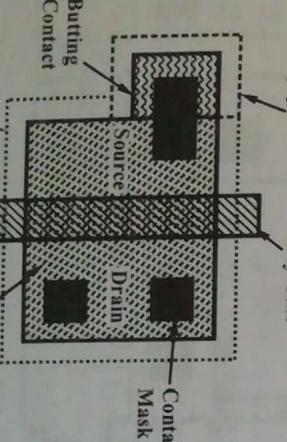
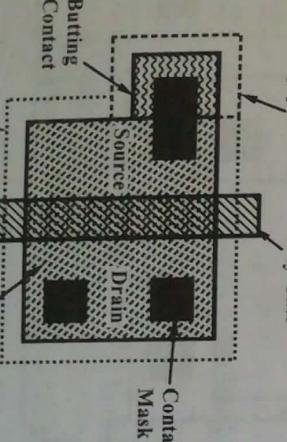
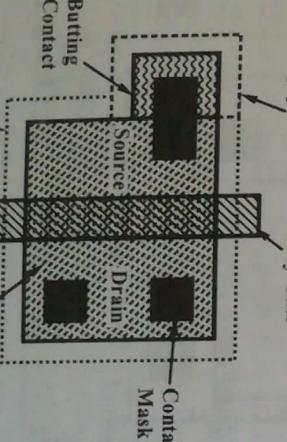
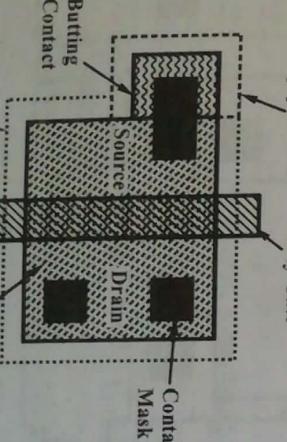
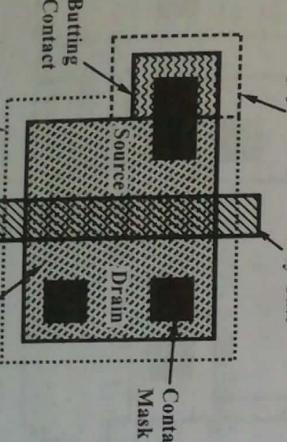
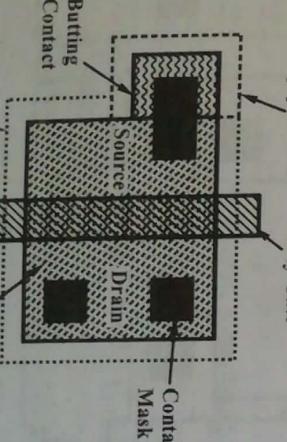
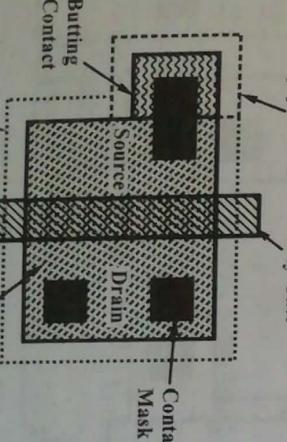
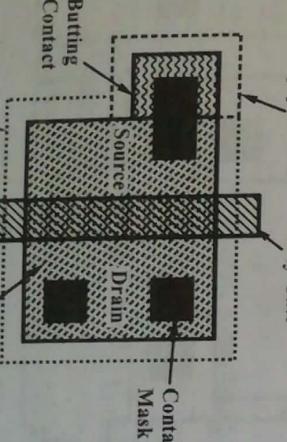
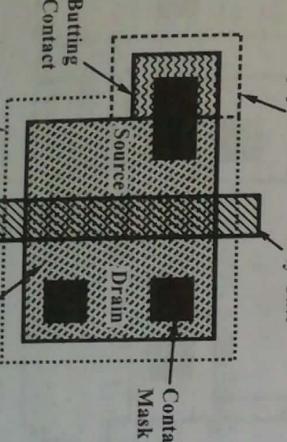
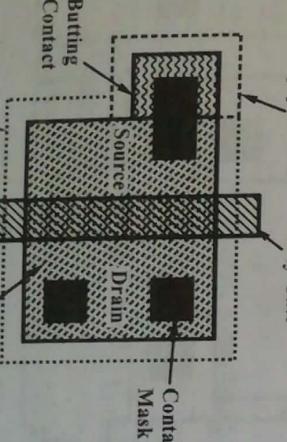
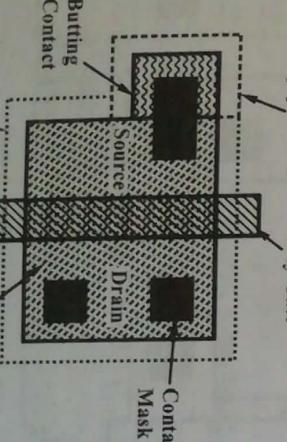
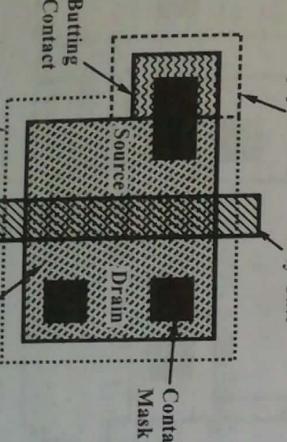
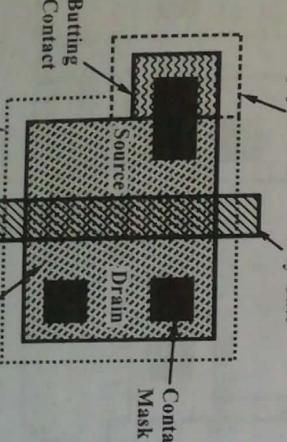
(iv) Guard Rings – Guard rings that are p⁺ source/drain

p-substrate and n⁺ diffusions in the n-well are used to collect injected minority carriers. If they are implemented in a structure, then n⁺ guard rings must be tied to V_{DD}, while p⁺ guard rings must be tied to V_{SS}. A p⁺ diffusion with n⁺ guard ring is shown in fig. 1.26 (a), while an n⁺ diffusion with p⁺ guard ring is shown in fig. 1.26 (b).

Different well-enclosure rules may apply for guard-ring structures. The structure shown in fig. 1.26 (a) is also that for a pnp transistor if one was required. The transistor terminals have been marked. The area of the center p⁺ region is the area of the emitter. The base is the n-well and is connected via the n⁺ ring. The collector is substrate.

Fig. 1.25 Structure of a Merged or Abutting Substrate Contact

Via Rules – Processes may vary in whether they allow vias to be placed over polysilicon and diffusion regions. Some processes allow vias to be placed



within these areas but do not allow the vias to straddle the boundary of polysilicon or diffusion. This results from the sudden vertical topology variations that occur at sublayer boundaries.

Metal 2 Rules – The possible increase in width and separation of second level metal are conservative rules to ensure against broken conductors or shorts between adjoining wires due to the vertical topology. Modern processes frequently have the metal 1 and metal 2 pitches identical.

Via 2 Rules – Similarly to first vias, the rules for placement of via 2 may vary with process.

Metal 3 Rules – These rules usually but not always increase in width and separation over metal 2. Metal 3 is generally used primarily for power supply connections and clock distribution.

Q.42. Explain construction rules for transistor and vias.

(R.G.P.V., June 2017)

Ans. Refer to the ans. of Q.41 (ii) and (v).

Q.43. Explain briefly Lambda based design rule.

Ans. Lambda rules specify the layout constraints in terms of a single parameter (λ) and hence permit linear, proportional scaling of all geometrical constraints. Lambda based layout design rules were originally devised to simplify the industry-standard micron-based design rules and to permit scaling capability for various processes. However, it must be emphasized that most of the submicron CMOS process design rules do not tend themselves to straightforward linear scaling. So, use of lambda-based design rules must be handled with caution in submicron geometries.

Q.44. Discuss the design flow for a VLSI circuit. (R.G.P.V., Dec. 2014)

Ans. The VLSI design process (Y-chart) contains three major domains as shown in fig. 1.27.

- (i) Behavioural domain
- (ii) Structural domain
- (iii) Geometrical layout domain.

The design flow begins from the algorithm which describes the behaviour of the target chip. The corresponding architecture of the processor is then defined. It is mapped onto the chip surface by floor planning. The next design evolution in the behavioural domain defines finite state machines (FSMs) which are structurally implemented with functional modules like registers and arithmetic logic units (ALUs). These modules are then geometrically placed onto the chip surface using CAD tools for automatic

module placement followed by routing with a aim of minimizing the interconnects area and signal delays. The third evolution involves the behavioural module description. Individual modules evolution begins with a leaf cells. The chip is described in terms of logic gates (leaf cells) at this stage, which can be placed and interconnected by using a cell placement and routing program. The last evolution involves a detailed Boolean description of leaf cells followed by a transistor level implementation of leaf cells and mask generation. In standard-cell based design, leaf cells and mask generation are already pre-designed and stored in a library for logic design use.

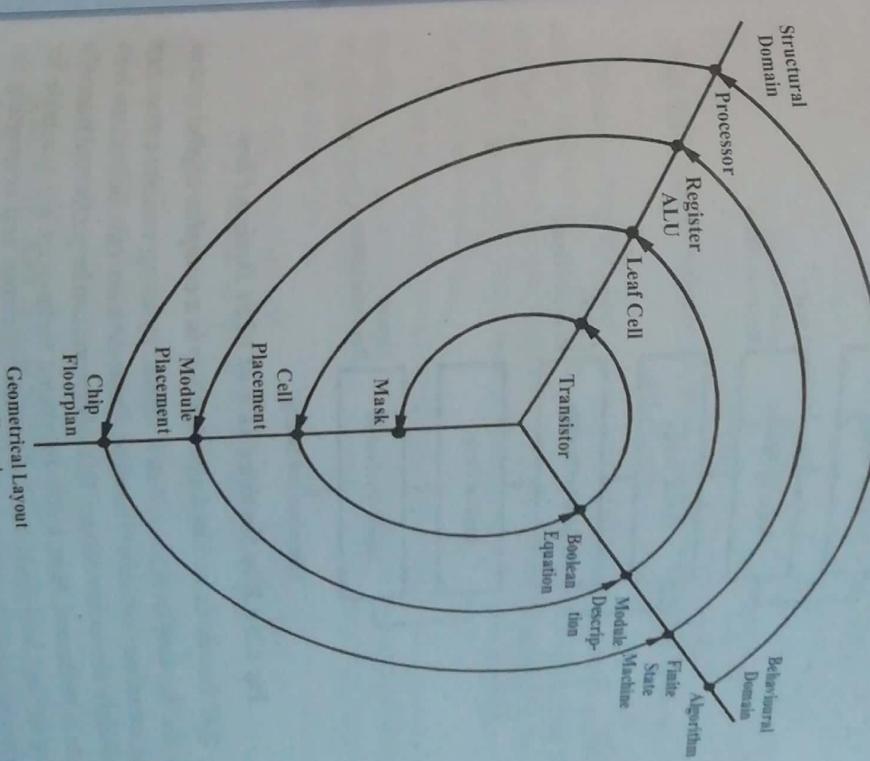
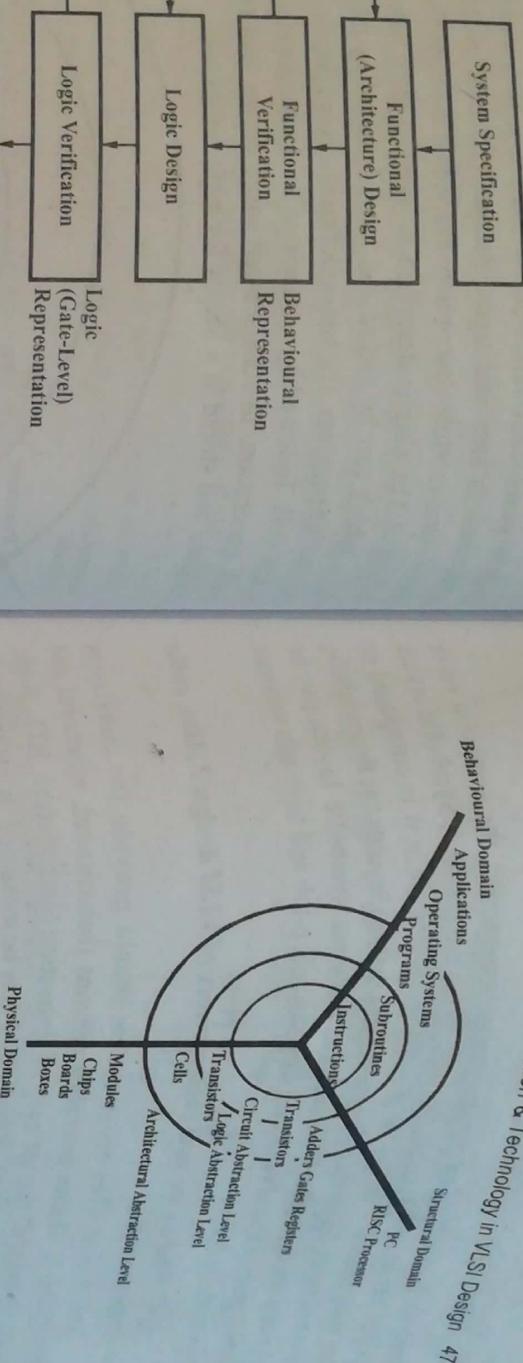


Fig. 1.27 VLSI Design Flow in Three Domains

Fig. 1.28 shows a more simplified view of the VLSI design flow, taking into account the various representations, or abstractions of design – behavioural, logic, circuit and mask layout. During this process, the verification of design plays a very important role in every step.

Fig. 1.29 Key Design Domains and Levels of Abstraction



What a particular system does, is specified by the behavioural domain and how entities are connected together to affect the prescribed behaviour, is specified by the structural domain. Finally, the physical domain specifies, how to actually construct a structure which has the needed connectivity to implement the prescribed behaviour.

There are a variety of levels of abstraction at which each domain can be specified. Various levels of abstraction which are common in electronic design are represented by the concentric circles around the centre. From highest to lowest they might be -

- (i) Architectural
 - (ii) Algorithmic
 - (iii) Module or functional block
 - (iv) Logical
 - (v) Switch
 - (vi) Circuit levels

(v) Switch
In general, any design can be expressed in terms of the three design domains, and the levels of domain, which are used, vary depending on design style and circuit complexity.

Fig. 1.28 A More Simplified View of VLSI Design Flow

Ques. Describe the various design domains in a complex digital system.

or can be mechanized. Now, highly automated techniques are available for taking very high level descriptions of system behaviour and converting them

Q.46. Write short note on layout editors.

been developed to describe integrated electronic systems. Fig. 1.29 shows the various digital design domains and levels of abstraction, in which three distinct design domains are shown by three radial lines. These domains are as follows:

... write short note on layout editor.

stick diagram layouts, that include some...
...stick diagrams but are still more abstract as compared to pure layouts.
example: 

symbolic layout; if a final physical layout is requested, the symbolic layout is fleshed out into all the rectangles needed for the process. Symbolic layout has many benefits – the layout is easier to specify since it is composed of fewer elements; the layout editor guarantees that the layouts for the symbolic elements are appropriately formed and the same symbolic layout can be used to produce several variations, such as n-tub, p-tub and twin-tub versions of a symbolic design.

Q.47. What are the main characteristics of VLSI design ? Also, enlis its design parameters.

Ans. A good VLSI design system should provide for consistent descriptions in all three description domains (behavioural, structural and physical) and at all relevant levels of abstraction (architecture, RTL, logic circuit). The means by which this is done may be measured in various terms which differ in importance based on the application. These design parameters are given as below –

- (i) Performance – speed, power, function, flexibility
- (ii) Size of die (hence cost of die)
- (iii) Time to design (hence cost of engineering and schedule)
- (iv) Ease of test generation and testability.

Design is a continuous trade-off to obtain adequate results for all of the above parameters. As such, the tools and methodologies used for a particular chip will be a function of these parameters. Certain end results have to be satisfied (that is, the chip must conform to performance specifications), but other constraints may be a function of economics (that is, size of die affecting yield) or even subjectivity.

If the process of designing a system on silicon is complicated, the role of good VLSI design aids is to minimize this complexity, increase productivity and assure the designer of a working product. A good method of simplifying the approach to a design is by the use of constraints and abstractions. The tool designer has some hope of automating procedures and taking a lot of the “legwork” out of a design by using constraints. The designer can collapse details and arrive at a simpler concept with which to deal by using abstractions.

Design methodologies permit a variation in the freedom available in the design strategy. The selection assuming all styles are equally available, should be entirely economic. According to function, appropriate design methods are chosen. Because of inefficiencies in layout, some styles will not be capable of implementing the function. Following these steps, the required die cost is estimated and the fastest means of achieving that die should be selected.

Prob.3. Design of an inverter layout as shown in fig. 1.30.

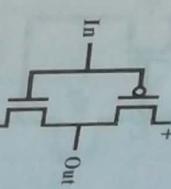


Fig. 1.30

Sol. The inverter circuit is simple (+ is V_{DD} and the triangle is V_{SS}). The layout is shown in fig. 1.31.

Fig. 1.31

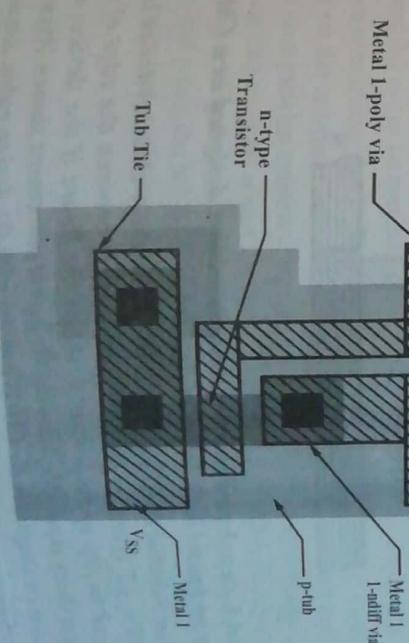


Fig. 1.31

NUMERICAL PROBLEMS

Prob.4. Draw the layout of the circuit shown in fig. 1.32.

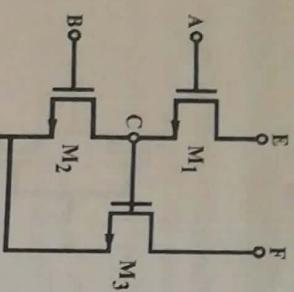


Fig. 1.32

Sol. Fig. 1.33 represents the layout structure which is obtained by σ_1 in circuit diagram.

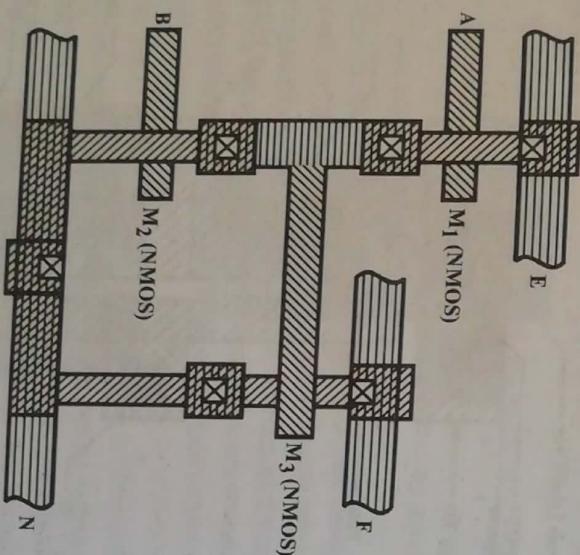


Fig. 1.33

process are depicted in the figure of Fig. 1.

If the p-channel density is ρ , then $\rho = \rho_0$.

p-tub and the edge of the p-mosat, d , shown the figure if the devices are packed as closely as possible following the layout placement shown. Assume the devices are designed in the CMOS process with the design rules. Assume $\lambda = 0.75 \mu$

<i>Dimension</i>	<i>Design rule</i>	<i>Minimum Size</i>
d ₁ , d ₃	2.5	2λ
d ₂ , d ₈	2.1, 3.1	2λ
d ₄	2.3	6λ
d ₅ , d ₁₁	5.8	λ
d ₆ , d ₁₀	5.1	2λ
d ₇ , d ₉	5.6	2λ

The dimensions $d_1 - d_{11}$ must satisfy the design rules. The restriction on these dimensions as imposed by the design rules are as follows:

The layout itself introduces some additional constraints. From th

specified, it can be concluded that $d_2 \geq 2L_{\min}$ and $d_8 \geq 6W_{\min}$. From design rules 2.1 and 3.1 it can be concluded that $d_2 \geq 40$ and $d_5 \geq 120$. The layout itself also places constraints on d_1 . Since the constraint on d_1 is the size of the model and

...concerns on U_1 . Since the contact as well as the edges of the metal and poly on the left-hand side on the n-channel transistor are to remain inside the p-well (a somewhat arbitrary requirement) it can be argued by design rule 5.6 that the contact must be at least 2λ . From design rules 5.4 and 5.7, the poly and metal

must overhang the contact by λ . Since there is no minimum spacing between the poly and p-tub, the left-hand edge of the poly in the tub can be coincident with the tub edge (although the outer ring may be broken). It thus follows that,

$$d_1 \geq 5\lambda$$

$$\text{But, } d = \sum_{i=1}^n d_i$$

Sol. Since only the L/W ratios are specified, W will be chosen minimum size for the n-channel transistor and L will be chosen minimum size for the p-channel device.

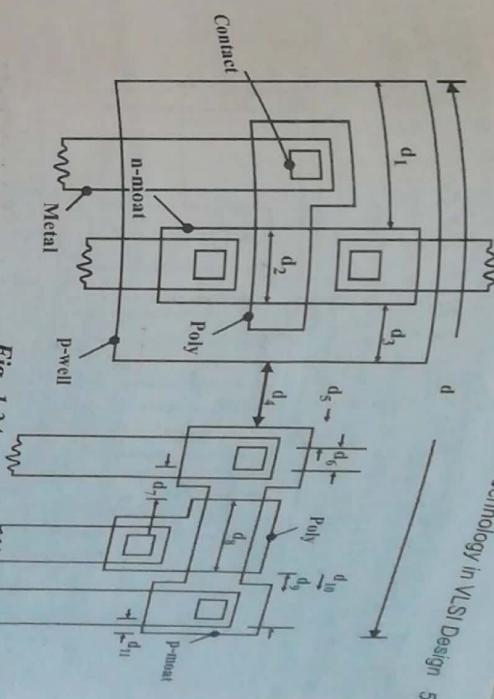


Fig. 1.34

Prob. 6. A thick film resistor layout strategy is shown in fig. 1.35. Determine the minimum substrate size ($L \times H$) if the resistor is to have a nominal value of $325 \text{ k}\Omega$ and is to use the layout strategy of this figure, the design rules ($\lambda = 250\mu$) and the process parameters.

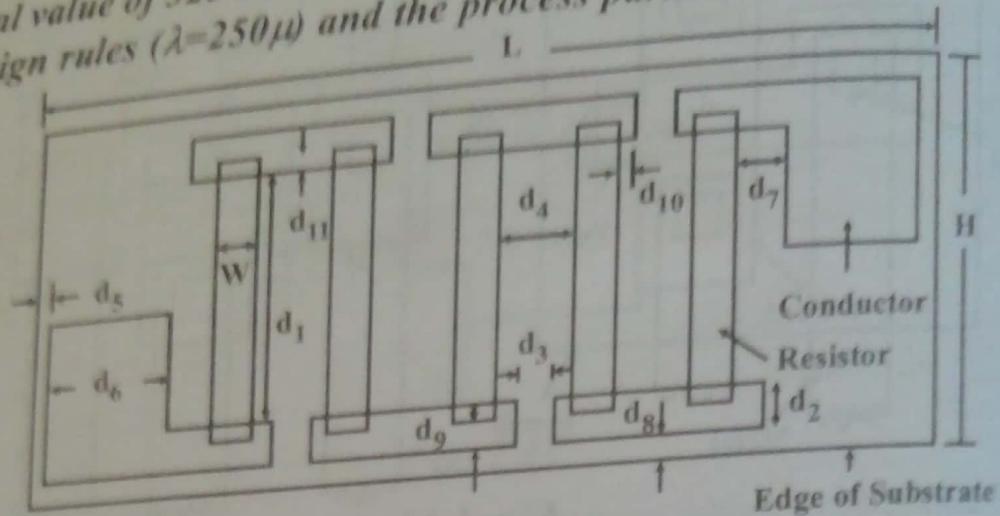


Fig. 1.35

Sol. Since $R = 325 \text{ k}\Omega$ and since the goal is to minimize area, the higher sheet resistance screening will be used for the resistors. We obtain $R_s = 10,000 \Omega/\lambda$. If the contact resistance and sheet resistance are neglected we require $n = 325 \text{ k}\Omega/R_s = 32.5$ squares of resistive material. Since there are five equal width resistances in series, each of width W , the length of each must equal $32.5W/5 = 6.5 W$.

From fig. 1.35, it follows that the length and height of the substrate are given, respectively by –

$$L = 2d_5 + 2d_6 + 2d_7 + 5W + 4d_4$$

$$H = 2d_8 + 2d_2 + d_1$$

The following minimum sizes are obtained for each of the parameters $d_2 - d_{11}$ and W –

It should be noted that even though these are minimum spacings, the layout itself may impose more stringent requirements to avoid layout violations. Specifically,

$$d_4 \geq d_3 + 2d_{10} = 4\lambda$$

$$d_2 \geq d_9 + d_{11} = 2\lambda$$

$$d_1 \geq 5\lambda$$

We thus obtain –

$$L = (2)(2\lambda) + (2)(4\lambda) + 2(2\lambda) + (5)(5\lambda) + (4)(4\lambda) = 57\lambda$$

$$H = (2)(2\lambda) + (2)(2\lambda) + (6.5)(5\lambda) = 40.5\lambda$$

With $\lambda = 250 \mu$, the minimum substrate size is

$$= 1.425 \text{ cm} \times 1.0125 \text{ cm}$$

Parameter	Rule	Size
d_2	1	2λ
d_3	1.2	2λ
d_4	2.2	2λ
d_5, d_8	1.5	4λ
d_6	4.0	2λ
d_7	2.3	λ
d_9	1.3a	λ
d_{10}	1.3b	λ
d_{11}	2.4	5λ
d_1, W	2.1	

Ans
■■