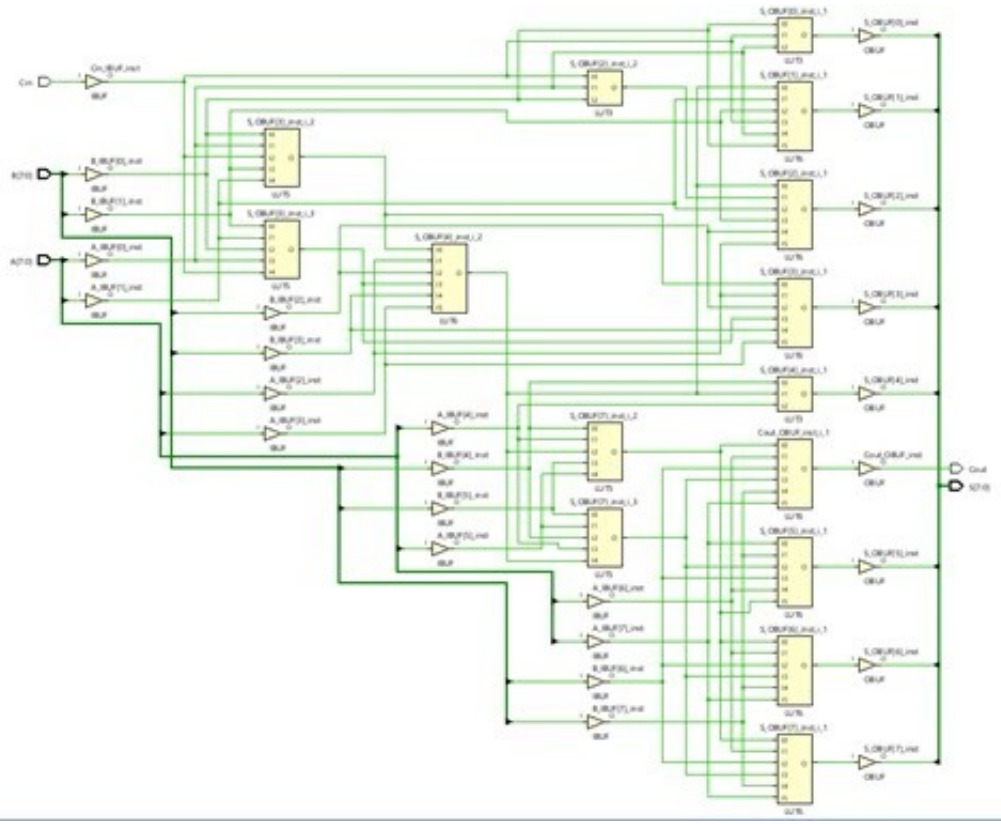
```
module bcd(A,B,Cin,S,Cout);
input [7:0] A;
input [7:0] B;
input Cin;
output [7:0] S;
output Cout  ;
wire [4:0] LSD_sum;
wire [4:0] MSD_sum;
wire LSD_carry;
wire MSD_carry;
assign LSD_sum = {1'b0, A[3:0]} + {1'b0, B[3:0]} + Cin;
assign LSD_carry = (LSD_sum > 9) ? 1'b1 : 1'b0;
assign S[3:0] = (LSD_sum > 9) ? (LSD_sum[3:0] + 4'b0110) : LSD_sum[3:0];
assign MSD_sum = {1'b0, A[7:4]} + {1'b0, B[7:4]} + LSD_carry;
assign MSD_carry = (MSD_sum > 9) ? 1'b1 : 1'b0;
assign S[7:4] = (MSD_sum > 9) ? (MSD_sum[3:0] + 4'b0110) : MSD_sum[3:0];
assign Cout = MSD_carry;
endmodule
```

```
module bcd_tb;
reg [7:0] A,B;
reg Cin;
wire [7:0] S;
wire Cout;
 bcd uut (.A(A),.B(B),.Cin(Cin),.S(S),.Cout(Cout));
initial begin
$display("Time\tA\t\tB\t\tCin\tS\t\tCout");
A = 8'b00010010;
B = 8'b00000101;
Cin = 0;
#10 $display("%0dns\t%h\t%h\t%b\t%h\t%b", $time, A, B, Cin, S, Cout);
A = 8'b00010010;
B = 8'b00000101;
Cin = 1;
#10 $display("%0dns\t%h\t%h\t%b\t%h\t%b", $time, A, B, Cin, S, Cout);
A = 8'b00010011;
B = 8'b00010010;
Cin = 0;
#10 $display("%0dns\t%h\t%h\t%b\t%h\t%b", $time, A, B, Cin, S, Cout);
A = 8'b00010100;
B = 8'b00010110;
Cin = 0;
#10 $display("%0dns\t%h\t%h\t%b\t%h\t%b", $time, A, B, Cin, S, Cout);
A = 8'b10011001;
B = 8'b00000001;

Cin = 0;
#10 $display("%0dns\t%h\t%h\t%b\t%h\t%b", $time, A, B, Cin, S, Cout);
end
endmodule
```

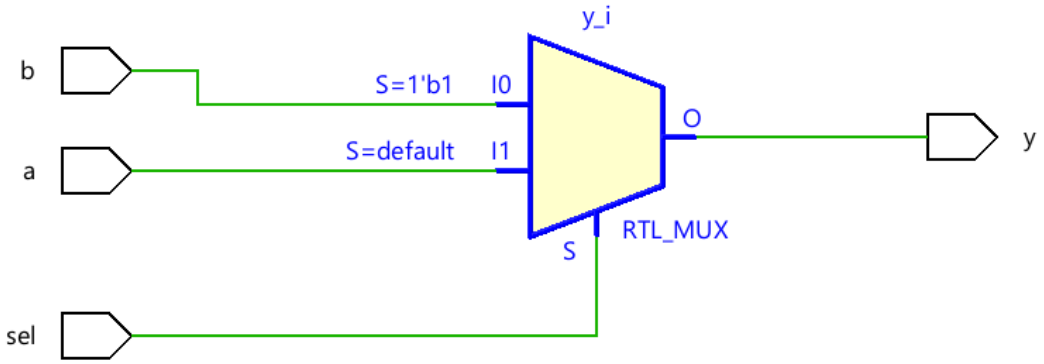


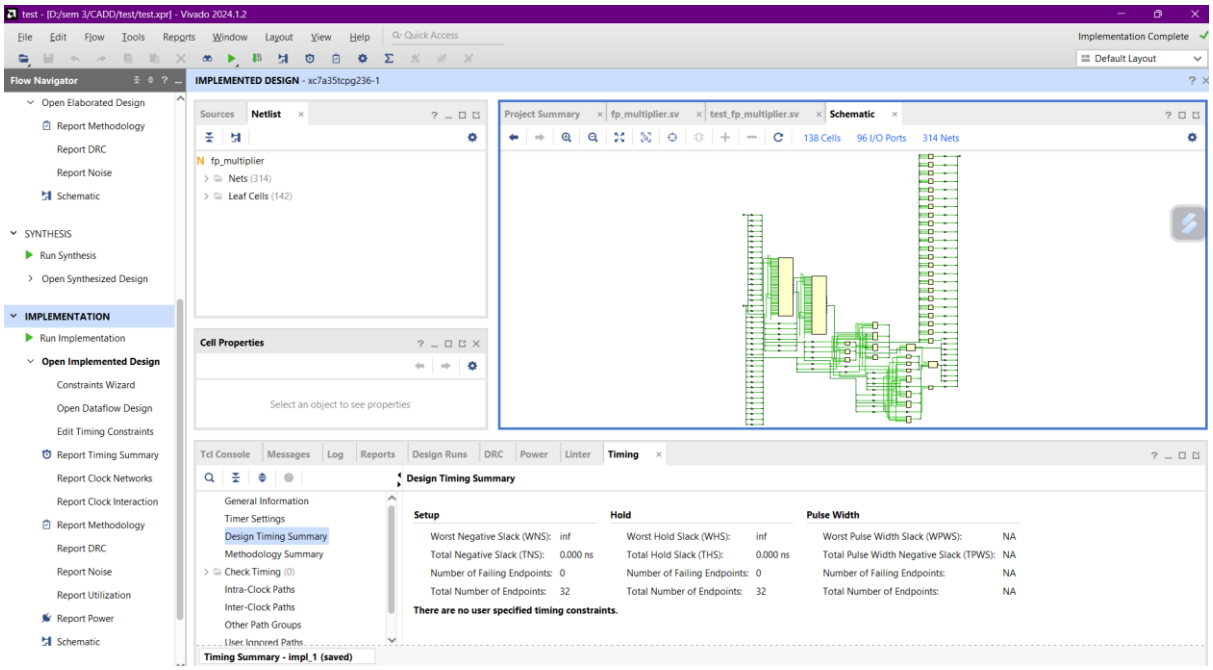
```
  input [31:0] a,
  input [31:0] b,
output [31:0] result
);
  wire sign_a, sign_b, sign_result;
  wire [7:0] exp_a, exp_b, exp_result;
  wire [23:0] mant_a, mant_b, mant_result;
  wire [47:0] mant_mult;
  wire [7:0] exp_sum;

  assign sign_a = a[31];
  assign sign_b = b[31];
  assign exp_a = a[30:23];
  assign exp_b = b[30:23];
  assign mant_a = {1'b1, a[22:0]};
  assign mant_b = {1'b1, b[22:0]};

  assign sign_result = sign_a ^ sign_b;
  assign exp_sum = exp_a + exp_b - 8'd127;
  assign mant_mult = mant_a * mant_b;

  assign mant_result = mant_mult[47] ? mant_mult[46:24] : mant_mult[45:23];
  assign exp_result = mant_mult[47] ? exp_sum + 1 : exp_sum;

  assign result = {sign_result, exp_result, mant_result[22:0]};
endmodule
```

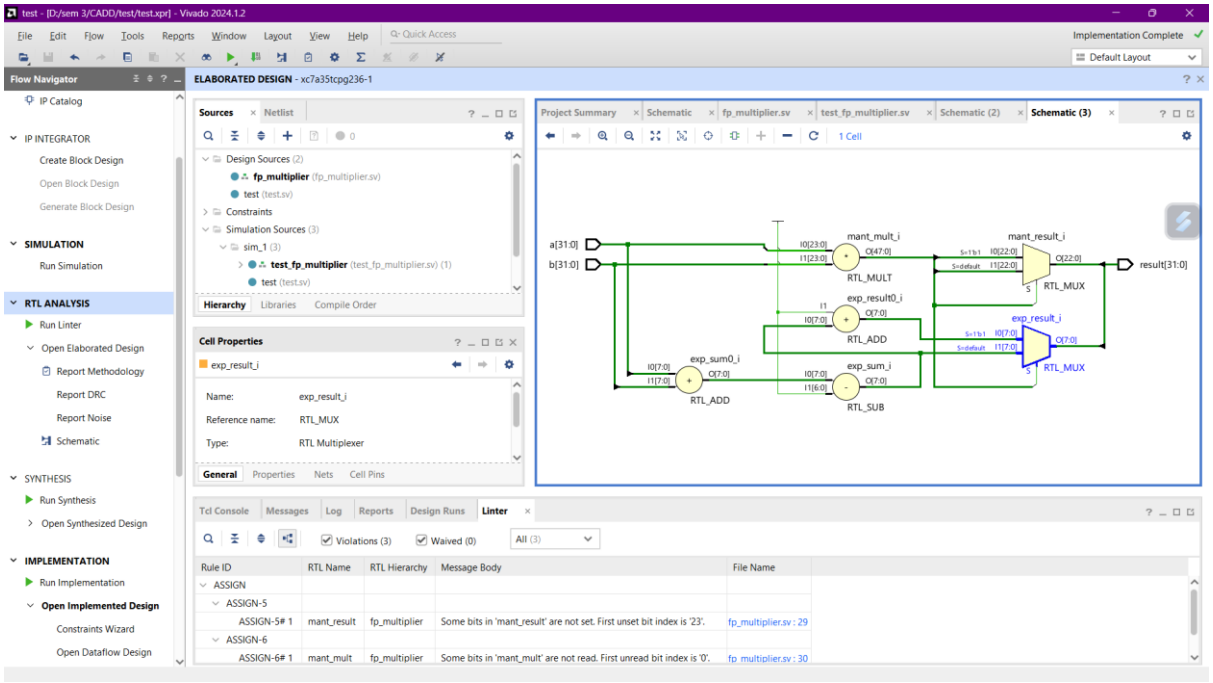
Testbench

```
module test_fp_multiplier;
  logic [31:0] a, b;
  logic [31:0] result;

  fp_multiplier uut (
    .a(a),
    .b(b),
    .result(result)
```

```
  );

  initial begin
    $display("Time\t a\t\t\t b\t\t\t result");
    $monitor("%0t\t %h\t %h\t %h", $time, a, b, result);

    // Test cases
    a = 32'h3f800000; // 1.0
    b = 32'h40000000; // 2.0
    #10;

    a = 32'h40400000; // 3.0
    b = 32'h40800000; // 4.0
    #10;

    a = 32'h3f800000; // 1.0
    b = 32'h3f800000; // 1.0
    #10;

    a = 32'h3f800000; // 1.0
    b = 32'h00000000; // 0.0
    #10;

    a = 32'h3f800000; // 1.0
    b = 32'hbf800000; // -1.0
    #10;

    $finish;
  end
endmodule
```


y_i
b
S=1'b1
I0
O
y
a
S=default
I1
RTL_MUX
S
sel


test - [D:/sem 3/CADD/test/test.xpr] - Vivado 2024.1.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Implementation Complete
Default Layout
Flow Navigator
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Open Dataflow Design
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
Sources
Netlist
fp_multiplier
Nets (314)
Leaf Cells (142)
Cell Properties
Select an object to see properties
Project Summary
fp_multiplier.sv
test_fp_multiplier.sv
Schematic
138 Cells
96 I/O Ports
314 Nets
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Linter
Timing
Design Timing Summary
General Information
Timer Settings
Design Timing Summary
Methodology Summary
Check Timing (0)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Setup
Worst Negative Slack (WNS): inf
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 32
Hold
Worst Hold Slack (WHS): inf
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 32
Pulse Width
Worst Pulse Width Slack (WPWS): NA
Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
There are no user specified timing constraints.
Timing Summary - impl_1 (saved)


test - [D:/sem 3/CADD/test/test.xpr] - Vivado 2024.1.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Implementation Complete
Default Layout
Flow Navigator
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Open Dataflow Design
ELABORATED DESIGN - xc7a35tcpg236-1
Sources
Netlist
Design Sources (2)
fp_multiplier (fp_multiplier.sv)
test (test.sv)
Constraints
Simulation Sources (3)
sim_1 (3)
test_fp_multiplier (test_fp_multiplier.sv) (1)
test (test.sv)
Hierarchy
Libraries
Compile Order
Cell Properties
exp_result_i
Name: exp_result_i
Reference name: RTL_MUX
Type: RTL Multiplexer
General
Properties
Nets
Cell Pins
Project Summary
Schematic
fp_multiplier.sv
test_fp_multiplier.sv
Schematic (2)
Schematic (3)
1 Cell
a[31:0]
b[31:0]
mant_mult_i
RTL_MULT
mant_result_i
RTL_MUX
result[31:0]
exp_result0_i
RTL_ADD
exp_result_i
RTL_MUX
exp_sum0_i
RTL_ADD
exp_sum_i
RTL_SUB
Tcl Console
Messages
Log
Reports
Design Runs
Linter
Violations (3)
Waived (0)
All (3)
Rule ID
RTL Name
RTL Hierarchy
Message Body
File Name
ASSIGN
ASSIGN-5
ASSIGN-5# 1
mant_result
fp_multiplier
Some bits in 'mant_result' are not set. First unset bit index is '23'.
fp_multiplier.sv : 29
ASSIGN-6
ASSIGN-6# 1
mant_mult
fp_multiplier
Some bits in 'mant_mult' are not read. First unread bit index is '0'.
fp_multiplier.sv : 30

32-bit prefix adder

Input A -> Input B -> Generate & Propagate -> Prefix Tree -> Sum Calculation -> Output Sum.

System Verilog design code for 32-prefix adder

```
module prefix_adder (
  input [31:0] a,
  input [31:0] b,
  output [31:0] sum
);
  wire [31:0] g, p, c;

  assign g = a & b;
  assign p = a ^ b;

  assign c[0] = 0;
  genvar i;
  generate
    for (i = 1; i < 32; i = i + 1) begin
      assign c[i] = g[i-1] | (p[i-1] & c[i-1]);
    end
  endgenerate

  assign sum = p ^ c;
endmodule
```

testbench

```
module test_prefix_adder;
  logic [31:0] a, b;
  logic [31:0] sum;

  prefix_adder uut (
    .a(a),
    .b(b),
```

```
    .sum(sum)
  );

  initial begin
    $display("Time\t a\t\t\t b\t\t\t sum");
    $monitor("%0t\t %h\t %h\t %h", $time, a, b, sum);

    // Test cases
    a = 32'h00000000; b = 32'h00000000; #10;
    a = 32'h00000001; b = 32'h00000001; #10;
    a = 32'hFFFFFFFF; b = 32'h00000001; #10;
    a = 32'h12345678; b = 32'h87654321; #10;
    a = 32'hAAAAAAAA; b = 32'h55555555; #10;

    $finish;
  end
endmodule
```

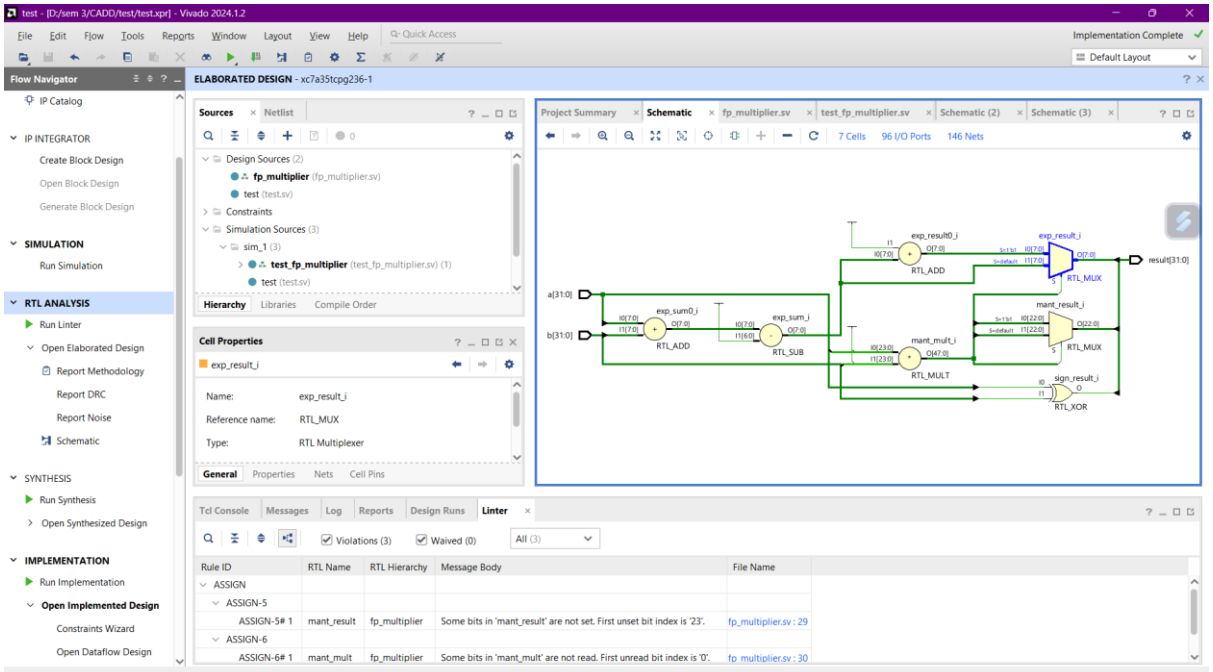
Delay Calculation

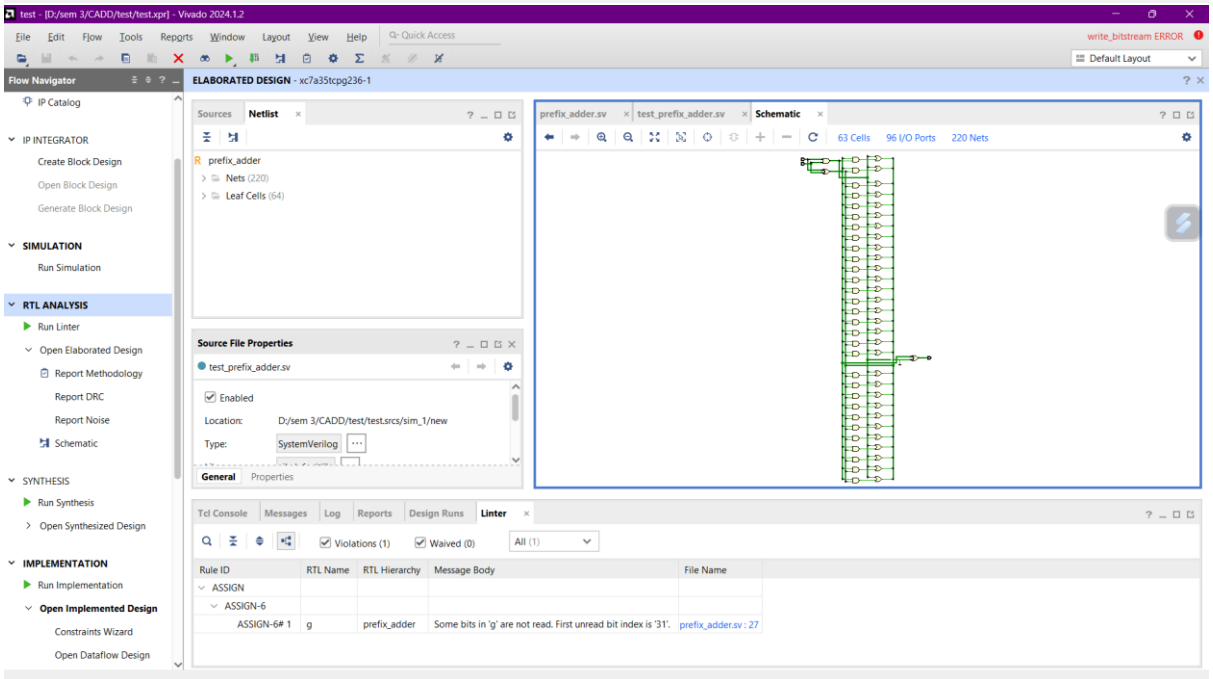
The delay of the 32-bit prefix adder can be calculated based on the number of stages in the prefix tree. Assuming each two-input gate delay is 100 ps, the delay can be estimated by counting the number of stages

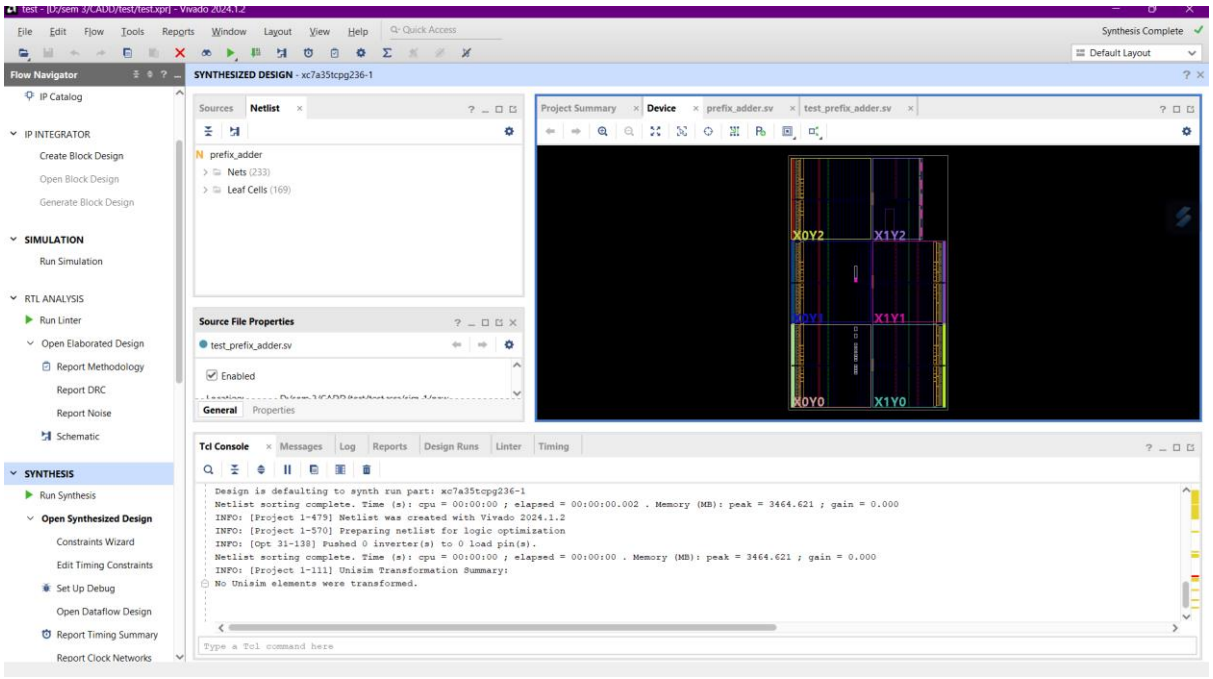
pipelined_prefix_adder

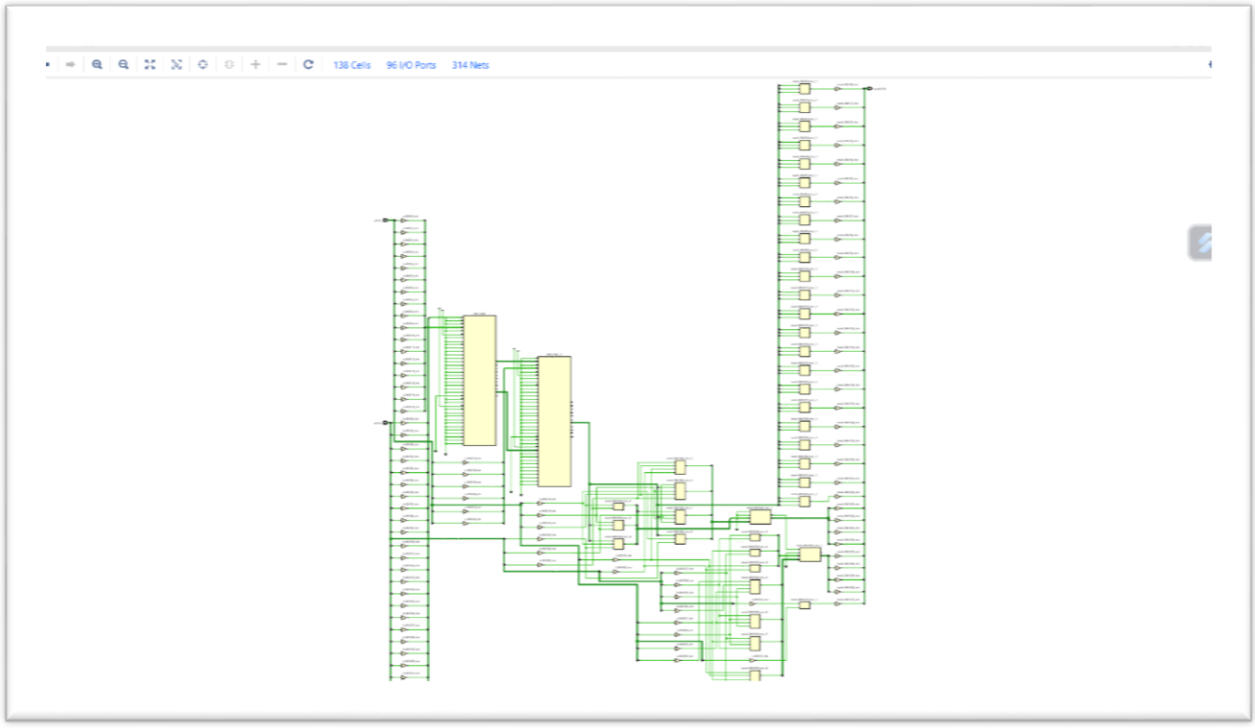
```
module pipelined_prefix_adder (
  input clk,
  input [31:0] a,
  input [31:0] b,
  output reg [31:0] sum
);
  reg [31:0] g, p, c;

  always @(posedge clk) begin
    g <= a & b;
    p <= a ^ b;
```

```
  end

  always @(posedge clk) begin
    c[0] <= 0;
    for (int i = 1; i < 32; i = i + 1) begin
      c[i] <= g[i-1] | (p[i-1] & c[i-1]);
    end
  end

  always @(posedge clk) begin
    sum <= p ^ c;
  end
endmodule
```


test - [D:/sem 3/CADD/test/test.xpr] - Vivado 2024.1.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Implementation Complete
Default Layout
Flow Navigator
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Open Dataflow Design
ELABORATED DESIGN - xc7a35tcpg236-1
Sources
Netlist
Design Sources (2)
fp_multiplier (fp_multiplier.sv)
test (test.sv)
Constraints
Simulation Sources (3)
sim_1 (3)
test_fp_multiplier (test_fp_multiplier.sv) (1)
test (test.sv)
Hierarchy
Libraries
Compile Order
Cell Properties
exp_result_i
Name: exp_result_i
Reference name: RTL_MUX
Type: RTL Multiplexer
General
Properties
Nets
Cell Pins
Project Summary
Schematic
fp_multiplier.sv
test_fp_multiplier.sv
Schematic (2)
Schematic (3)
7 Cells
96 I/O Ports
146 Nets
a[31:0]
b[31:0]
result[31:0]
exp_result0_i
exp_result_i
exp_sum0_i
exp_sum_i
mant_result_i
mant_mult_i
sign_result_i
RTL_ADD
RTL_SUB
RTL_MUX
RTL_MULT
RTL_XOR
Tcl Console
Messages
Log
Reports
Design Runs
Linter
Violations (3)
Waived (0)
All (3)
Rule ID
RTL Name
RTL Hierarchy
Message Body
File Name
ASSIGN
ASSIGN-5
ASSIGN-5# 1
mant_result
fp_multiplier
Some bits in 'mant_result' are not set. First unset bit index is '23'.
fp_multiplier.sv : 29
ASSIGN-6
ASSIGN-6# 1
mant_mult
Some bits in 'mant_mult' are not read. First unread bit index is '0'.
fp_multiplier.sv : 30


test - [D:/sem 3/CADD/test/test.xpr] - Vivado 2024.1.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
write_bitstream ERROR
Default Layout
Flow Navigator
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Open Dataflow Design
ELABORATED DESIGN - xc7a35tcpg236-1
Sources
Netlist
prefix_adder
Nets (220)
Leaf Cells (64)
Source File Properties
test_prefix_adder.sv
Enabled
Location: D:/sem 3/CADD/test/test.srcs/sim_1/new
Type: SystemVerilog
General
Properties
prefix_adder.sv
test_prefix_adder.sv
Schematic
63 Cells
96 I/O Ports
220 Nets
Tcl Console
Messages
Log
Reports
Design Runs
Linter
Violations (1)
Waived (0)
All (1)
Rule ID
RTL Name
RTL Hierarchy
Message Body
File Name
ASSIGN
ASSIGN-6
ASSIGN-6# 1
g
prefix_adder
Some bits in 'g' are not read. First unread bit index is '31'.
prefix_adder.sv : 27


File Edit Flow Tools Reports Window Layout View Help
Synthesis Complete
Default Layout
Flow Navigator
SYNTHESIZED DESIGN - xc7a35tcpg236-1
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Open Dataflow Design
Report Timing Summary
Report Clock Networks
Sources
Netlist
prefix_adder
Nets (233)
Leaf Cells (169)
Source File Properties
test_prefix_adder.sv
Enabled
General
Properties
Project Summary
Device
prefix_adder.sv
test_prefix_adder.sv
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Tcl Console
Messages
Log
Reports
Design Runs
Linter
Timing
Design is defaulting to synth run part: xc7a35tcpg236-1
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.002 . Memory (MB): peak = 3464.621 ; gain = 0.000
INFO: [Project 1-479] Netlist was created with Vivado 2024.1.2
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 3464.621 ; gain = 0.000
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
Type a Tcl command here


138 Cells
96 I/O Ports
314 Nets