Bundelkhand Institute of Engineering & Technology,Jhansi, Uttar Pradesh

Class Test- 1

Class (Yr&Branch): 2nd(EE)Semester: 4th Subject:Digital Eloctronics (KEE-401)

Attempt all the questions (3X5 =15)

1. Express the following numbers in decimal : $(10110.0101)_2$, $(16.5)_{16}$, $(26.24)_8$
2. Simplify the function $F(w,x,y,z)=\Sigma m(0,1,2,4,5,12,13,14)$ using Karnaugh map. don't care conditions $\Sigma d(6,8,9)$.
3. A) Implement the following Boolean function using 8:1 multiplexer $F(A,B,C.D) = \Sigma m\ (0,1,2,5,7,8,9,14,15)$

   B) Explain about Decimal Adder?
4. Explain the SR flip-flop in brief.
5. A) Design a 4 bit binary parallel subtractor and the explain operation in detail?

   B) Design the combinational circuit of 4 Bit Parallel Adder?

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Class Test- 2

Class (Yr&Branch): 2nd(EE)Semester: 4th Subject:Digital Eloctronics (KEE-401)

Attempt any three questions (3X5=15)

1. **Describe the operation of 4-bit universal shift registers.**
2. Design synchronous UP/DOWN counter.
3. **Explain the operation of Ring counter and Jonshon counter.**
4. Explain the function of 2-input RTL with neat circuit diagram.

Total Number of Printed Pages: 02 KEE-401

(Roll No. to be filled by candidate)									
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B. TECH.
EVEN SEMESTER THEORY EXAMINATION, 23
KEE-401
DIGITAL ELECTRONICS

Time: 03 Hours **Max. Marks: 100**

Note:

- Attempt all questions. All questions carry equal marks.
- Assume missing data suitably.

1. Attempt any ***FOUR*** parts of the following: 4×5=20 CO
   a. $(650)_{10}$ to hexadecimal, gray, BCD and binary.. CO1
   b. Given X= $(38)_{10}$ and Y= $(105)_{10}$. Using 2's complement method calculate (i) X-Y (ii) Y-X CO1
   c. Realize the Boolean expression Z=ABC + AD + CD' using NAND gates only CO1
   d. Find the standard Product of Sum (POS) for the logic expression F=(A + B'C) C CO1
   e. Using K map, minimize the expression F(A,B,C,D) =∑m(1,2,3,8,14,15) + d(0,4,6,10). CO1
   f. Design a full subtractor logic circuit. CO1

2. Attempt any **TWO** parts of the following: 2×10=20 CO
   a. Realize the following function F(A,B,C,D) = ∑m(1,3,4,10,11,12,13) using (i) 4 X 1 MUX (ii) 8 X 1 MUX CO2
   b. . (i) Explain the working of decimal to BCD encoder circuit. CO2
   (ii) Realise a full adder using two half adders.
   c. Using a 4 variable K map, simplify, F(A,B,C,D) = ∑m (1,4,9,10,11,12,14) + d (0,8,13) Realize the function using NAND gates only CO2

3. Attempt any **TWO** parts of the following: 2×10=20 CO

a. (i)Draw the logic diagram of J-K flip flop and explain it. What is the advantage of J-K flip flop over S-R flip flop. (ii) Explain a 3 bit asynchronous up counter. Draw the timing diagram and truth table CO3

b. Design a 3-bit gray code synchronous counter using J-K flip flop and explain the steps in detail. CO3

c. Design a mod-11 asynchronous counter using T flip flops and discuss its disadvantages. CO3

4. Attempt any **TWO** parts of the following: 2×10=20 CO

a. Design a MOD-12 asynchronous counter (ripple counter) using JK flip flop. Explain the working with truth table and timing diagram. CO4

b. Describe the operation of 4 bit SISO shift register with the help of block diagram, truth table and timing diagram CO4

c. Explain the following: a) Race around problem. b) Synchronous and asynchronous counters. c) Johnson and ring counter. CO4

5. Attempt any **TWO** parts of the following: 2×10=20 CO

a. Explain in brief of the following: CO5
i) DTL, TTL ,ECL ii) CMOS inverter

b. Explain in brief of the following: CO5
i) ROM, RAM, Fan out, Fan in ii)Noise margin, PLA, PAL, CPLD, FPGA

c. Explain the operation of successive approximation ADC. Discuss its merits and demerits. CO5