Design of High Speed Latched Comparator
A Comparative Study between Single Tail and Double Tail Dynamic Latched Comparator Architectures

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Keypoints

Latched comparator

Single tail

Double tail

Speed & power consumption

Accuracy

Abstract

The design of high-speed latched comparators is of paramount importance in the field of analog and mixed-signal integrated circuit design. The Single Tail Dynamic Latched Comparator (ST-DLC) and the Double Tail Dynamic Latched Comparator (DT-DLC) are two well-known architectures that are compared in-depth in this research article. This study's goal is to assess and contrast the speed, power consumption, and accuracy performance traits of these two architectures.

The ST-DLC and DT-DLC designs are implemented in the research using the Cadence design platform and its extensive library of parts and tools. To optimise the performance metrics, the design process adopts a systematic methodology that includes transistor sizing, biassing, and layout considerations.

A collection of representative test vectors and cutting-edge CMOS technology are used to conduct the experimental evaluation. Critical parameters including propagation delay, power dissipation, and offset voltage are evaluated using simulations. The findings are analysed, contrasted, and interpreted to offer insightful information about the advantages and disadvantages of each architecture.

The study's conclusions show that the DT-DLC architecture outperforms the ST-DLC architecture in terms of speed. Dual tail transistors make it possible for internal nodes to be charged and discharged more quickly, which reduces propagation latency. In contrast, the ST-DLC architecture exhibits higher power effectiveness, with lower power dissipation as a result of its streamlined design.

The findings of this study add to the body of knowledge about high-speed latching comparators and help design engineers choose the best architecture in light of certain design constraints. Insights from this study can also be used as a foundation for future developments in comparator design and optimisation.

Introduction

The design of high-speed latched comparators, which are essential in several applications including data converters, clock and data recovery circuits, and high-speed communication systems, was made necessary by the ongoing development of analogue and mixed-signal integrated circuits. These comparators are in charge of comparing input voltages to get precise and speedy choices.

In addition to these, the characteristics of ADCs, such as high-speed, low-power, and reduced area on die, make them widely accepted in the semiconductor industry at a time when the majority of devices are becoming portable and battery-operated. The

comparator, the most practical representative of the ADCs, is affected by all of these issues. Additionally, analogue circuit design is more difficult due to the requirement for reliability, where supply voltages must be lowered due to the tiny size of the transistors.

Comparator design is more demanding and challenging at low supply voltage in ultra-deep sub-micron CMOS technology because the threshold voltage of devices is not scaled down at the same rate as the technology. Larger size transistors are utilised in the design to make up for the drop in supply voltage, which increases power consumption and die size.

Switching and the input common-mode voltage range are additional issues with low supply voltage designs. Several methods are published in the literature to address the low voltage design issues, including supply boosting, current-mode design using body-driven transistors, and dual-oxide technologies.

There are numerous high-speed comparator architectures, including the regenerative latch comparator, the preamplifier latch comparator, and the multistage open-loop comparator. Using the multistage open-loop comparator, high resolution and high speed may be easily achieved among the various topologies. On the other hand, because of its high speed and low power consumption, the latch-type comparator is the most useful clocked regenerative comparator. It is founded on the latch of cross-coupled inverters. Strong positive feedback and no static power indulgence enable latch-type comparators to make decision more quickly.

Methods

Reducing Capacitive Loading: By minimising capacitance at key nodes in the comparator circuitry, one can speed up operation by reducing the time needed for charging and discharging. Transistor and connection layout and sizing considerations can help with this. Biasing and Supply Voltage: Increasing the supply voltage can result in more headroom and quicker operation. Power usage and heat dissipation should be taken into account to maintain equilibrium. The performance and speed of the comparator circuitry can also be enhanced by careful biassing.

Process Technology and Transistor Sizing: Using a high-speed CMOS process or another suitable process technology can result in quicker transistor switching rates. The performance of the comparator can also be improved by choosing the right transistor size based on the desired speed requirements.

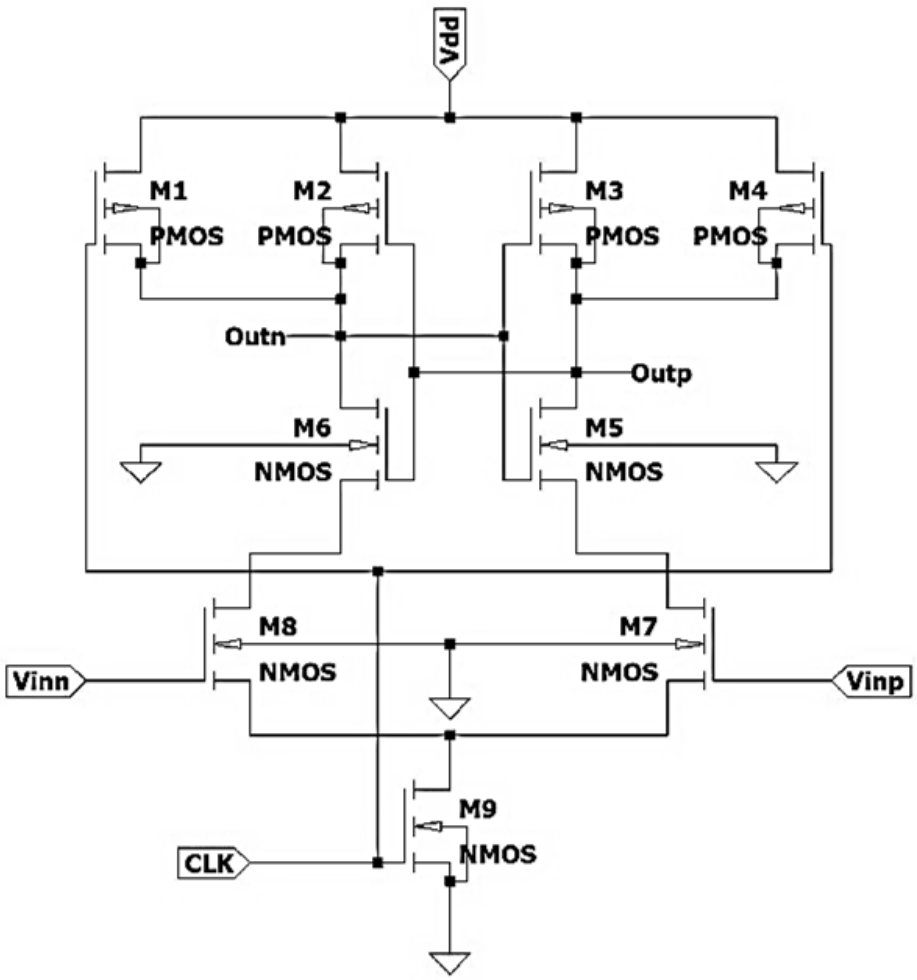
Single tail Dynamic Latched Comparator

In comparison to alternative architectures, the strong positive feedback based dynamic latch comparators are preferred because they satisfy the needs of high-speed and low-power ADC. In the literature, different performance metrics, such as noise input referred offset voltage, kick-back noise, and random decision errors, are analysed and published. The benefits and demerits of the two typically utilised topologies, single tail current dynamic latch comparator (STDLC) and double tail current dynamic latched comparator (DTDLC), are thoroughly analysed in this section.

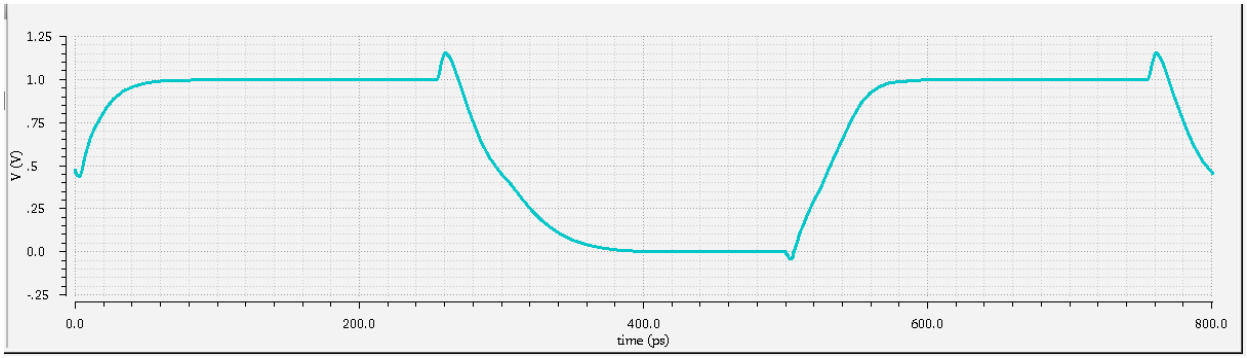
Dynamic comparators are essential in analog and digital circuits for high-speed and accurate comparison of voltages. They enable precise decision-making and are commonly used in applications such as ADCs, clock synchronization. They play a crucial role in signal processing by providing rapid voltage comparisons, enabling efficient and reliable operations in a wide range of electronic devices and systems. The schematic representation of a single tail current latching comparator is shown in the image above. The two phases of the comparator's operation are

reset (when CLK is low) and regeneration (when CLK is high). M7 and M8 are ON during the reset phase, bringing the output terminals (Outn and Outp) to Vdd. Furthermore, the tail current source, Mt1, is OFF,

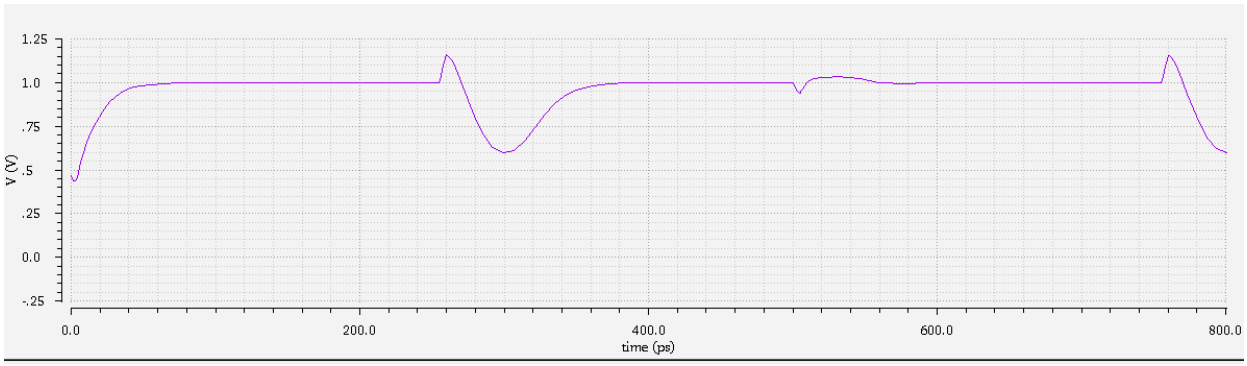
which completely eliminates static currents from Vdd to ground (apart from the small leakage currents). The regeneration phase begins with the activation of the current supply, at which point the output voltages begin to discharge to the ground at varying rates proportional to the corresponding input voltages.The transient behaviour of STDLC is as shown in figure



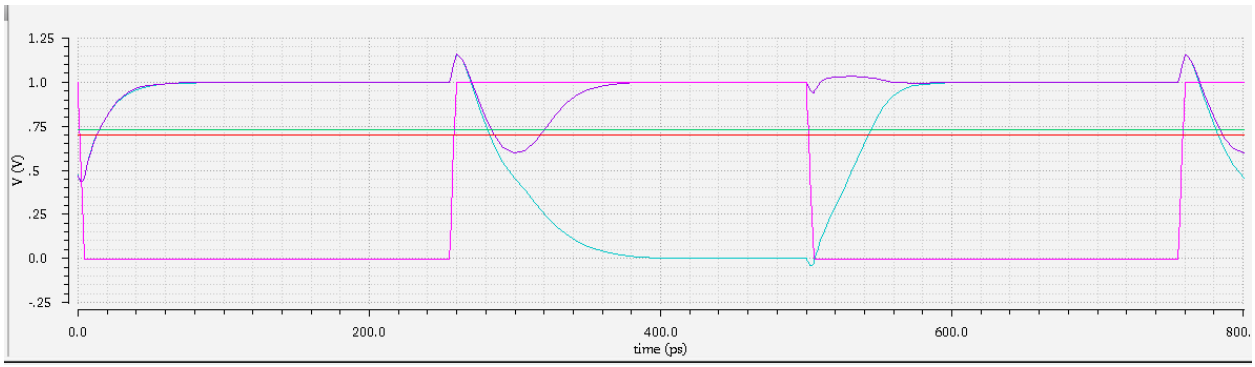
Outp:



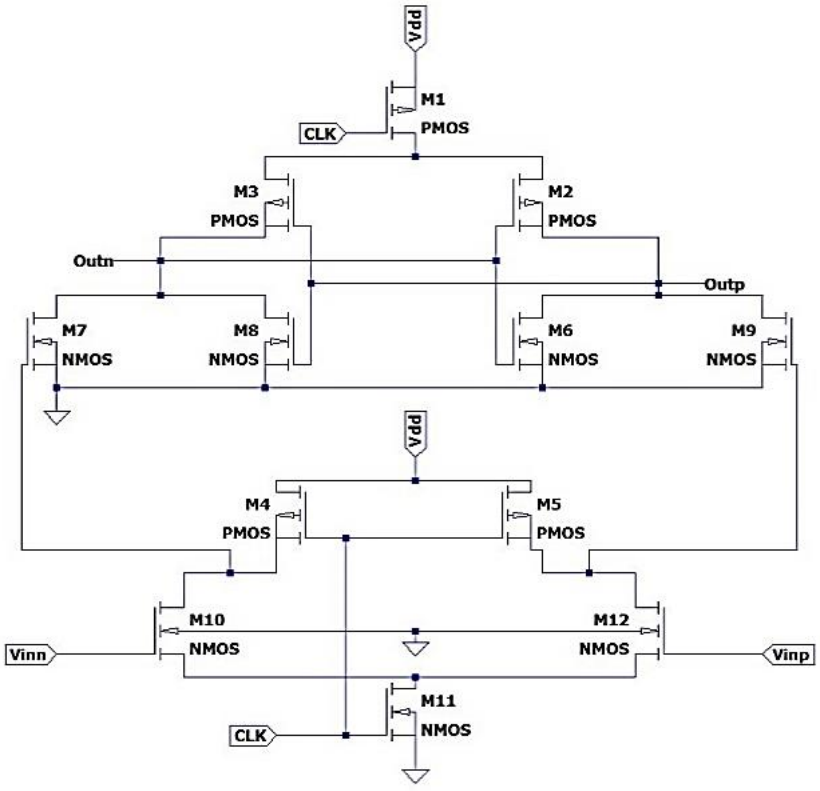
Outn:



Comparative plot of inputs and outputs:



Double tail Dynamic Latched Comparator

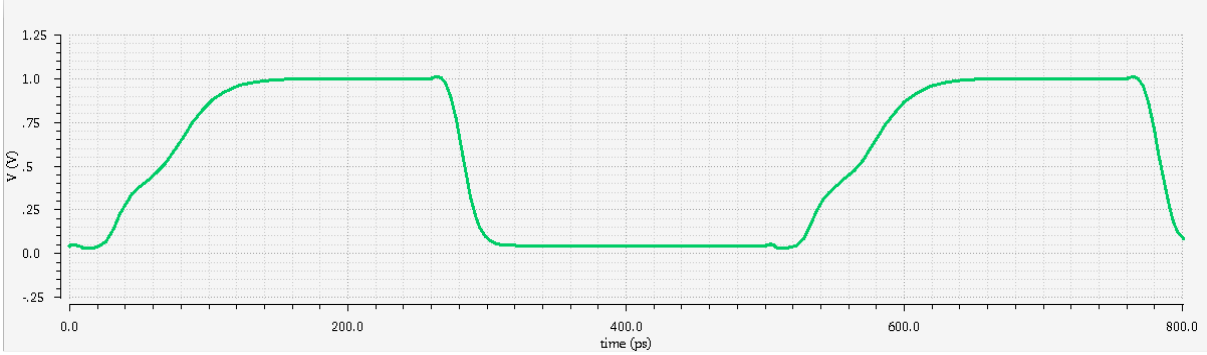


As compared to the previous STDLC, this double tail current latched comparator consists of two stages with two separate current tails. While the second stage (latch) has a strong tail current to give shorter delay, the first stage has a tiny tail current to achieve low offset. The double-tail latched comparator operates in two phases, just like the other latch comparator. The current sources of both stages, M1 and M11, are turned OFF during the reset phase (i.e., when CLK is low), guaranteeing that there is no static power consumption in the first phase. The terminals fp and fn are being pulled to Vdd by M4 and M5, which are ON. Because of this, M7 and M9 are turned ON, and Outn and Outp are reset to ground. When CLK is high, or during the regeneration phase, the current sources turn ON while M4 and M5 are turned OFF. As a result, the discharge rates of terminals fp and fn will differ and be proportionate to their respective inputs.

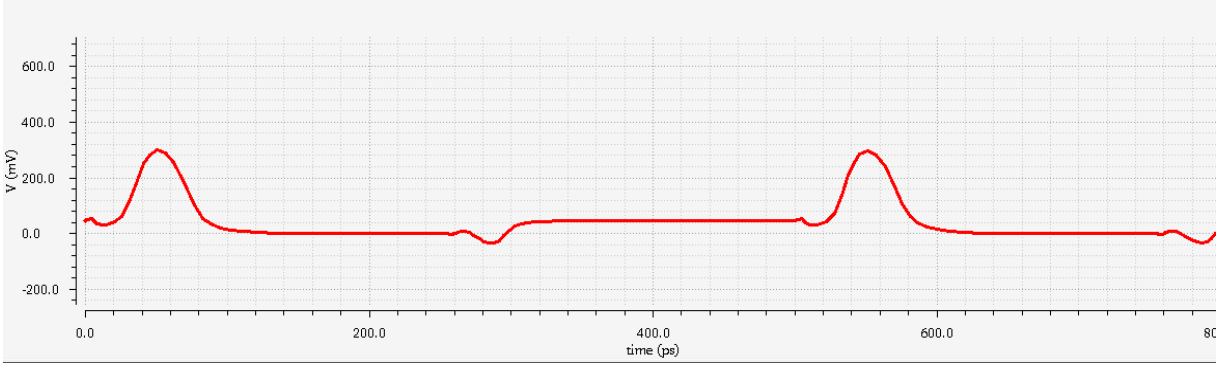
The intermediate transistor (M7 or M9) switches OFF when one of the first stage outputs falls below the threshold voltage of that transistor. The latch's positive feedback kicks in, forcing one output to ground and the other to Vdd. Additionally, there are two components to the delay in this comparator: t0 (capacitive discharge of load capacitance before the first NMOS (either M6 or M8) switches ON) and tdelay (latch delay). This is how time t0 is determined.

There are two stages in it: a preamplifier and a latch. Utilising a differential pair, the preamplifier amplifies the voltage difference between the inputs, and the latch stage stores the outcome of the comparison. The double-tail dynamic comparator's capacity to perform quick and precise comparisons by using a regenerative latch mechanism is its major feature. The preamplifier reacts quickly to changes in the inputs, forcing the latch to the desired output state. This comparator is frequently employed in applications where accuracy and speed are essential, such as high-speed communication systems and analog-to-digital converter.

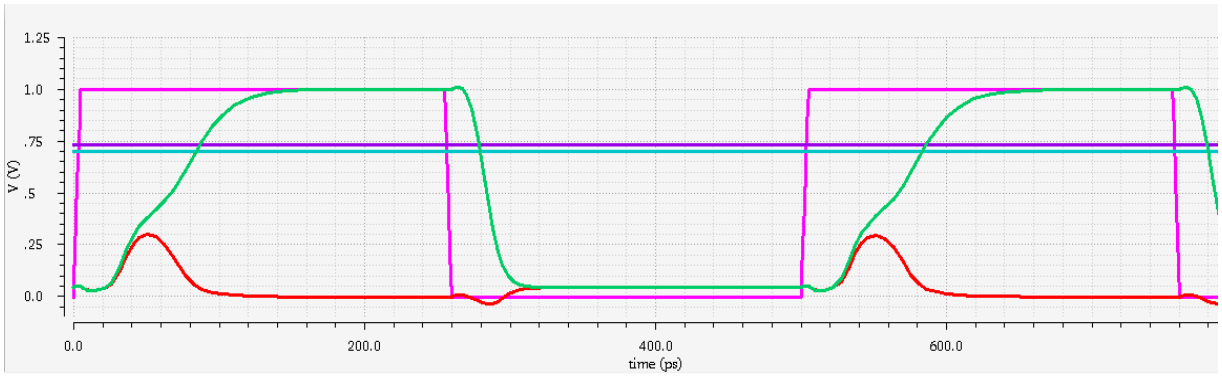
Outp:



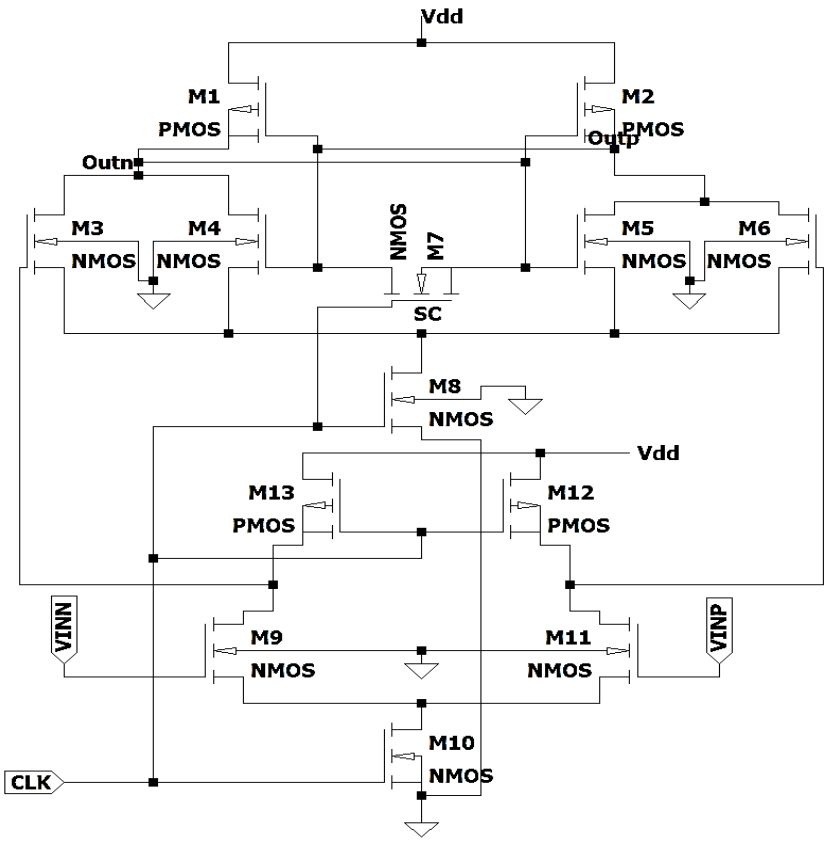
Outn:



Comparative plot of inputs and outputs:



Proposed Dynamic Latched Comparator



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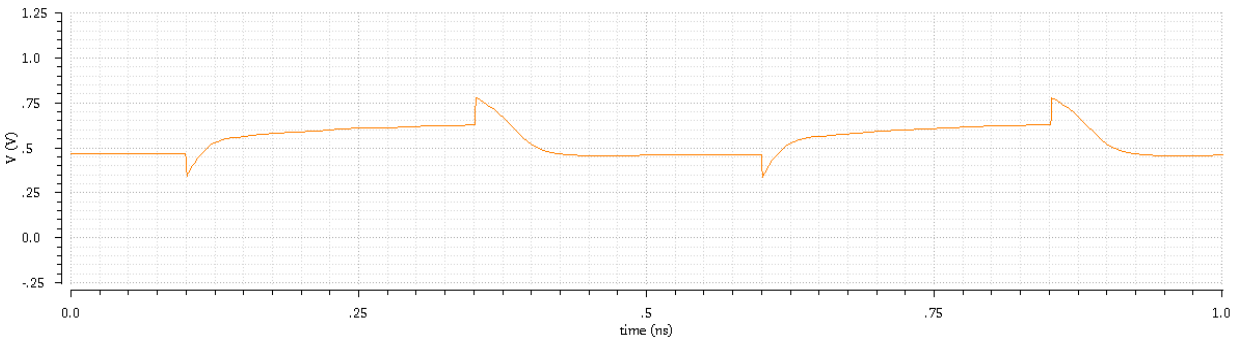
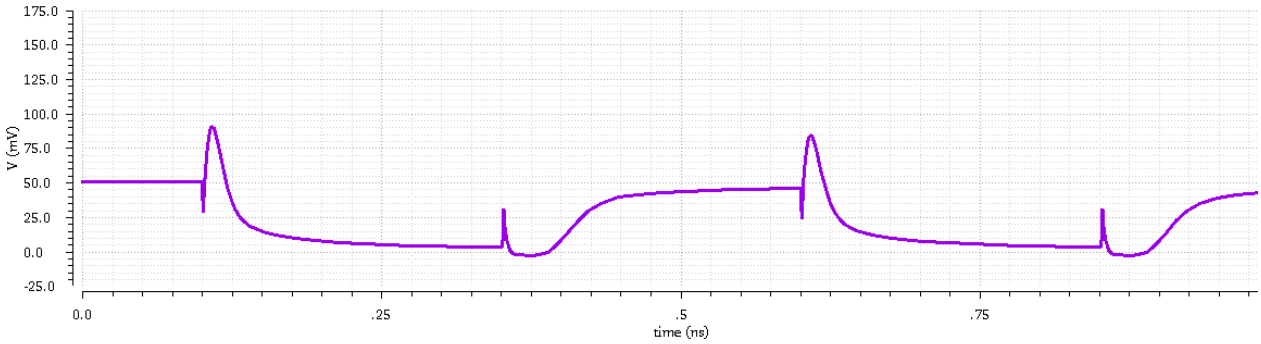
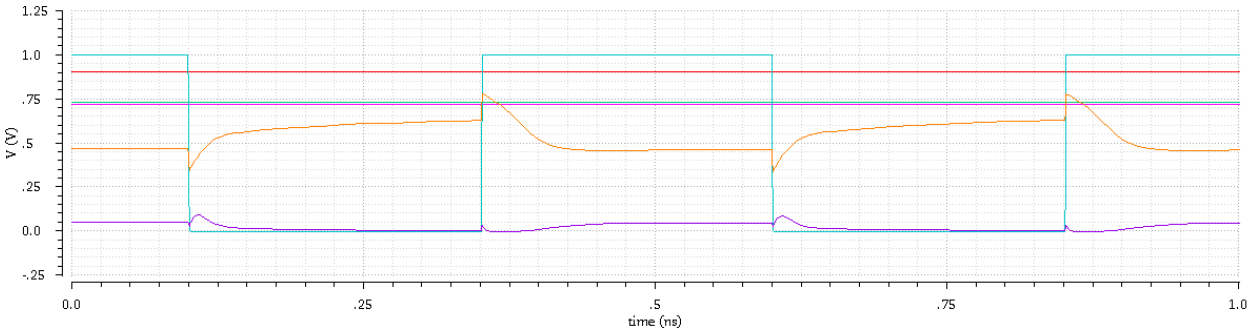


Outp:



Comparative plot of inputs and outputs:



Parameters used in Proposed Topology:

Component	Width (nm)	Length (nm)
PMOS M1	120	100
PMOS M2	120	100
PMOS M12	120	100
PMOS M13	120	100
NMOS M3	120	100
NMOS M4	120	100
NMOS M5	120	100
NMOS M6	120	100
NMOS M7	120	100
NMOS M8	120	100
NMOS M9	120	100
NMOS M10	120	100
NMOS M11	120	100

Input parameters:

Clock period-500ps,

Rise & Fall time-1ps,

Pulse width-250p,

Vdd-0.9Volts,

Vinp-0.72Volts,

Vinn-0.73Volts.

Software used: CADENCE 90nm

Comparative analysis

Analog comparators come in two basic configurations that are employed in electronic circuits, single-tail latched and double-tail latched. Let's contrast them based on their salient traits:

Single-Tail Latched Comparator: A single-tail latched comparator latches the output based on how well the input signal compares to a reference voltage. In general, single-tail comparators use less power than double-tail comparators. A single input signal is compared to a reference voltage or another input signal using a single-tail latch comparator. The output of a single-tail latched comparator is typically a single-ended signal, meaning it has only one output terminal.

Double-Tail Latched Comparator: When two input signals are compared in a double-tail latched comparator, the output is latched in accordance with the results. Due to their differential architecture and the requirement

for additional circuitry, double-tail comparators typically consume more power. This device contrasts two input signals. The output of a double-tail latched comparator is usually a differential signal, consisting of two output terminals with opposite polarities.

Conclusion:

This paper proposes a high speed, low power, two-stage dynamic latching comparator. In this suggested design, the first stage power consumption is reduced by restricting the voltage swing of the pre-amplifier to Vdd/2. Voltage swing restriction energises the evaluation stage and expedites comparison. The recommended dynamic latched comparator is shown to have a less time delay and less power loss. When compared to traditional CMOS comparators, the suggested dynamic latched comparator reduces power and delay. Finally, the graphical simulation of the 180 nm comparator mentor significantly saves power and delay.

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