

UNIVERSITY OF LAGOS
DEPARTMENT OF COMPUTER SCIENCES
B.Sc. (Hons) CONTINUOUS ASSESSMENT TEST
CSC313: ANALYSIS AND DESIGN OF DIGITAL SYSTEMS

Time Allowed: 1 hour 30 minutes

Instruction: Attempt ALL Questions

- 1 Which of the following is NOT TRUE about the impact of advances in digital integrated circuit technology?
 a It has led to dramatic reductions in the cost of digital devices
 b The number of transistors that can be put on a piece of silicon increases dramatically to support the integration of complex functions.
 c The speed at which digital devices can operate increases dramatically.
 d Equipment built with highly integrated digital devices become increasingly unreliable and highly susceptible to failure.
 e None of the above.
-
- 2 An n-bit register can store any binary number from
 a 0 to 2^{n-1} b 0 to $2^n - 1$ c 0 to $2n - 1$ d 0 to 2^{n-1} e None of the above
-
- 3 The even parity bit p_e of the N digit binary number $a_1a_2 \dots a_N$ can be generated as
 a $p_e = \overline{a_1 \oplus a_2 \oplus \dots \oplus a_N}$ b $p_e = \overline{a_1 \oplus a_2 \oplus \dots \oplus a_N}$ c $p_e = a_1 \oplus a_2 \oplus \dots \oplus a_N$
 d $p_e = a_1 \odot a_2 \odot \dots \odot a_N$ e None of the above
-
- 4 The generated parity bit in an even parity scheme is
 I 0 if the number of 1's is even II 1 if the number of 0's is even
 III 0 if the number of 1's is odd IV 1 if the number of 0's is odd
 a I only b II only c I & III only d II & IV only e None of the above
-
- 5 Which of the following is NOT TRUE?
 a A CPU enclosed in a small integrated-circuit is called a microprocessor.
 b A CPU combined with memory and interface control to form a small-size computer is called a microcomputer.
 c The CPU is made up of an Arithmetic Unit and a Control Unit.
 d The processor performs arithmetic and other data-processing tasks.
 e None of the above
-
- Answer questions 6 and 7 with the expression of a number in base r written below:
 $a_n r^n + a_{n-1} r^{n-1} + \dots + a_2 r^2 + a_1 r + a_0 + a_{-1} r^{-1} + a_{-2} r^{-2} + \dots + a_{-m} r^{-m}$
-
- 6 The $(r-1)$'s complement of the positive number N_r with n digits is
 a $r^n - N$ b $r^n - N$ c $r^n - N - 1$ d $(r-1)^n - N$ e $(r-1)^n - N - 1$
-
- 7 The value that may be represented by the coefficients $a_n a_{n-1} a_{n-2} \dots a_1 a_0$ in base r is
 a r^{n+1} b $r^n + 1$ c $r^n - 1$ d r^n e $r^{n-1} - 1$
-
- 8 Which of the following is NOT TRUE?
 a The 2's complement has advantage over 1's complement of being easier to implement by digital circuits.
 b The 1's complement requires two arithmetic additions when an end-carry carry occurs.
 c During subtraction of two numbers the 2's complement has advantage over 1's complement in that only one arithmetic operation is required.
 d The 1's complement has a disadvantage of possessing two arithmetic zeroes.
 e The 1's complement is equivalent to a logical inversion operation.
-
- 9 Convert $(0.6875)_{10}$
 a $(0.1101)_2$ b $(0.0111)_2$ c $\checkmark (0.1011)_2$ d $(0.1110)_2$ e None of the above
-
- Answer questions 10 to 14 with the following binary code for decimal digits:
 a BCD b 84-2-1 c Excess 3 d 2421 e None of the above
-
- 10 Which code has error detection capabilities?
-
- 11 Which 4-bit code is NOT a weighted code?
-
- 12 Which 4-bit code represents 7 with a combination that contains two ones and two zeroes?
-
- 13 Which code is weighted and self-complementing?
-
- 14 In which 4-bit code is the code 0111 not valid?
-
- 15 Which of the following is NOT CORRECT in the following steps that describe the subtraction of two unsigned n-digit numbers the minuend M and the subtrahend N in base r.
 I Add the minuend M to the r's complement of the subtrahend N.
 II If $M \geq N$ the sum does not produce an end carry and is equal to $r^n - (N - M)$.
 III If $M < N$ the sum will produce an end carry r^n which will be discarded; what is left is the result $M - N$.
 a I only b II only c II & III d III only e None of the above

- 16 Parity code schemes fail when there is (are)
 a an odd number of errors.
 b an even number of errors.
 c errors in alternate bit positions.
 d errors in powers of two.
 e a single error.
- 17 The 16's complement of B2FA is
 a 5D05
 b 5D06
 c 4D05
 d 4D06
 e None of the above
- 18 Which of the following is NOT TRUE?
 a Integrated circuits are cheaper than discrete components.
 b Discrete components can operate at higher speeds than integrated circuits.
 c Integrated circuits reduce the number of external wiring connections required to build circuits when compared to discrete components.
 d Digital circuits built from integrated circuits are smaller than circuits built from discrete components.
 e None of the above.

- 19 The solutions to the quadratic equation $x^2 - 11x + 22 = 0$ are $x = 3$ and $x = 6$. What is the base of the numbers?
 a 7
 b 8
 c 10
 d 16
 e None of the above

Answer questions 20 to 23 with the following scientists:

- a De Morgan
 b Boole
 c Shannon
 d Huntington
 e None of the above
- 20 Introduced a two-valued Boolean algebra called switching algebra.
- 21 Formalized Boolean algebra.
- 22 Invented the transistor.
- 23 Developed a theorem for the complement of logic operations.

- 24 Which of the following is NOT TRUE?
 a Huntington postulates do not include the associative law.
 b The complement operator in Boolean algebra is not available in ordinary algebra.
 c The inhibition operator is not commutative.
 d The exclusive-OR operation is both commutative and associative.
 e The equivalence function is an odd function.

Answer questions 25 to 29 with the following logic families:

- a Transistor-transistor logic (TTL)
 b Emitter-coupled logic (ECL)
 c Metal-oxide semiconductor (MOS)
 d Integrated-injection logic (I^2L)
 e Complementary metal-oxide semiconductor (CMOS)
- 25 It is the most popular logic family for fabricating SSI, MSI and LSI circuits.
- 26 It is the logic family used in systems requiring low power consumption.
- 27 It is the logic family used in systems requiring high-speed operations.
- 28 It is the logic family most frequently used to fabricate microprocessors.
- 29 It is the logic family used as an alternative to MOS for the fabrication of high density integrated circuits.
- 30 Which representation of signed binary numbers has only one version of the number zero?
 a Signed-1's complement
 b Signed-2's complement
 c Signed magnitude
 d All of the above
 e None of the above
- 31 The duality principle states that every algebraic expression deducible from the postulates of Boolean algebra remains valid if
 a operators are interchanged only
 b variables are complemented and operators are interchanged
 c operators and identity elements are interchanged
 d variables are complemented and operators and identity elements are interchanged
 e variables are complemented only

- 32 Which of the following is CORRECT?
 a $x \uparrow (y \uparrow z) = (x \uparrow y) \uparrow z$
 b $x \downarrow (y \downarrow z) = (x \downarrow y) \downarrow z$
 c $\overline{x \uparrow y} = x \downarrow y$
 d $\overline{x/y} = y/x$
 e None of the above

- 33 Which of the following is NOT TRUE of the ASCII code?
 a It is an alphanumeric code that is replacing Unicode.
 b It is a 7-bit code that is stored as a byte; the eighth bit is sometimes used as a parity bit for error checking.
 c It has characters that can be printed and non-printing characters for control functions.
 d Its character set includes, lowercase alphabets, uppercase alphabets and numbers.
 e All of the above.

- 34 Which of the following is NOT CONSIDERED when constructing logic gates?
 a Feasibility of implementing the gate with electronic components
 b Economy of implementing the gate with electronic components

- BLPA
EFDC
-
- c The ability of the gate to implementing Boolean functions alone or in conjunction with other gates.
 d The convenience of representing gate functions that are frequently used.
 e None of the above
-
- 35 Which of the following is NOT CORRECT?
- a Gate delay is the amount of time it takes for an input change to result in the corresponding output change.
 b NAND (NOR) gates are slower and more expensive than AND (OR) gates respectively because they include an additional NOT gate for functional equivalence.
 c Gate delay is influenced by gate type and number of inputs.
 d The INVERTER is a degenerate version of NAND and NOR gates with just one input.
 e NAND and NOR gates are called universal logic gates and are said to be functionally complete because each alone can implement any logic function.
-
- 36 The dual of the function $XY + \bar{X}Z + YZ$ is
- a $\bar{X}\bar{Y} + XZ + \bar{Y}Z$
 ✓ $(X+Y)(\bar{X}+Z)(Y+Z)$
 b $(X+Y)(\bar{X}+Z)(Y+Z)$
 c $(\bar{X}+\bar{Y})(X+\bar{Z})(\bar{Y}+Z)$
 d None of the above
-
- 37 Which of the following identities, if applied, will simplify the function $XY + \bar{X}Z + YZ$?
- a DeMorgan's theorem
 b Duality principle
 c Idempotent law
 d Consensus theorem
 e Distributive law
-
- 38 Which of the following is NOT TRUE of minterms?
- a There are 2^n minterms for n Boolean variables. These minterms can be generalized from the binary numbers from 0 to $2^n - 1$.
 b Any Boolean function can be expressed as a logical product of minterms.
 c The complement of a function contains those minterms not included in the original function.
 d A function that includes all the 2^n minterms is equal to logic 1.
 e None of the above.
-
- 39 What is the gate-input cost of the function $G(A,B,C,D) = (\bar{A}+B)(\bar{B}+C)(\bar{C}+D)(\bar{D}+A)$
- a 8 b 10 c 12 d 14 e 16
-
- 40 The Boolean function $G(A,B,C,D) = \bar{A}\bar{C}\bar{D} + \bar{A}\bar{D} + \bar{B}C + CD + A\bar{B}\bar{D}$ in its canonical form is
- a $\sum m(0,1,2,3,4,5,7,8,10,11,15)$
 b $\sum m(1,2,3,4,5,6,7,9,11,12,15)$
 c $\sum m(0,1,2,3,4,5,7,8,9,10,11,15)$
 d $\sum m(0,1,2,3,4,5,7,8,10,11,15)$
 e $\sum m(1,2,3,4,5,6,7,8,10,11,15)$
-
- 41 The minimization of the function in question 40 is
- a $BD + \bar{A}\bar{C} + CD$
 b $BD + AC + CD$
 c $\bar{B}\bar{D} + AC + CD$
 d $\bar{B}\bar{D} + \bar{A}\bar{C} + CD$
 e $BD + \bar{A}\bar{C} + \bar{C}\bar{D}$
-
- 42 Which of the following is TRUE?
- a A product term is an implicant of a function if the function has the value 0 for all minterms of the product term.
 b If the removal of ANY literal from an implicant P results in a product term that is not an implicant of the function, then P is a prime implicant.
 c If a minterm of a function is included in more than one prime implicant, that prime implicant is said to be essential.
 d The prime implicant of a function can be obtained from a map of the function as all possible minimum collections of 2^m squares containing 1s that constitute rectangles.
 e None of the above.
-
- 43 If an incompletely specified function $F(A,B,C,D) = \sum m(1,3,7,11,15)$ can be minimized as $CD + \bar{A}\bar{B}$ or $CD + \bar{A}D$ then it has don't care minterms
- a 0 b 0,2 c 0,5 d 2,5 e All of the above
-
- 44 Which of the following is an even function?
- a $1 \oplus A \oplus B \oplus C$
 b $1 \oplus A \oplus B \oplus C$
 c $0 \oplus A \oplus B \oplus C$
 d $0 \oplus A \oplus B \oplus C$
 e $1 \oplus A \oplus B \oplus C$
-
- 45 The function $F = \sum(1,2,4,7,8,11,13,14)$ is
- a $A \oplus B \oplus C \oplus D$
 b $A \oplus B \oplus C \oplus D$
 c $A \oplus B \oplus C \oplus D$
 d $A \oplus B \oplus C \oplus D$
 e None of the above
-
- Match the definitions in questions 45 to 48 with the following gate parameters:
- a Fan-out
 b Propagation delay
 c Power dissipation
 d Noise margin
 e None of the above
-
- 45 The maximum voltage added to the input signal of a digital circuit that does not cause an undesirable change in the circuit output.
-
- 46 Denotes how relatively fast signals pass through a gate when compared with an inverter.
-
- 47 Energy dissipated by signals propagated through wires connecting gates.

- 48 The maximum number of input lines to other gates that may be driven by the output of a gate without impairing its operations
- 49 Which of the following is NOT TRUE?
- The NAND gate is a universal logic gate.
 - The implementation of a Boolean function with NAND gates requires that the function be simplified in the product of sums.
 - Terms that may be included in the simplified expression of a function are called prime-implicants.
 - Essential prime implicants are terms that MUST be included in the simplified expression of a function.
 - All of the above.
- 50 Using the NAND technology the function $F = AB + (A\bar{B})C + (\bar{A}\bar{B})\bar{D} + E$ is implemented with x inverters and y NAND gates.
Select the CORRECT option from the following 2-tuple values of x and y .
- | | | | | |
|--------|--------|--------|--------|--------|
| a 2, 6 | b 3, 6 | c 2, 5 | d 2, 4 | e 3, 4 |
|--------|--------|--------|--------|--------|
- 51 The direct implementation of the function F in question 50 using the NOR technology will require
- the same number of inverters but more NOR gates than NAND gates
 - more inverters but the same number of NOR gates as NAND gates
 - the same number of inverters and the same number of NOR gates as NAND gates
 - the same number of inverters but fewer NOR gates than NAND gates
 - more inverters and more NOR gates than NAND gates
- 52 When implementing a function it is sum of products standard form, using the NAND technology will always have
- a higher gate-input cost when compared with the NOR technology
 - the same gate-input cost when compared with the NOR technology
 - a lower gate-input cost when compared with the NOR technology
 - a complexity component that make the comparison of gate-input cost with the NOR technology function dependent
 - None of the above

0 $M(0,0)$	1 $M(0,1)$	3 $M(0,2)$	2 $M(0,3)$	6 $M(0,4)$	7 $M(0,5)$	5 $M(0,6)$	4 $M(0,7)$
8 $M(1,0)$	9 $M(1,1)$	11 $M(1,2)$	10 $M(1,3)$	14 $M(1,4)$	15 $M(1,5)$	13 $M(1,6)$	12 $M(1,7)$
24 $M(2,0)$	25 $M(2,1)$	27 $M(2,2)$	26 $M(2,3)$	30 $M(2,4)$	31 $M(2,5)$	29 $M(2,6)$	28 $M(2,7)$
16 $M(3,0)$	17 $M(3,1)$	19 $M(3,2)$	18 $M(3,3)$	22 $M(3,4)$	23 $M(3,5)$	21 $M(3,6)$	20 $M(3,7)$

Figure 1

Cells in a 5-variable k-map (Figure 1) are labelled by the 2-tuple parameter $M(x,y)$ that has the decimal label of the cell as its value, e.g. $M(1,2) = 11$; if row and column indices are in modulo 4 and 8 respectively attempt questions 53 to 59. Assume variables A, B, C, D and E .

- 53 The maxterm of cell $M(3,5)$ is
- | | | |
|-----------------------------------|---|-----------------------------------|
| a $A + \bar{B} + C + D + E$ | b $\bar{A} + B + \bar{C} + \bar{D} + \bar{E}$ | c $A + B + C + \bar{D} + \bar{E}$ |
| d $\bar{A} + \bar{B} + C + D + E$ | e None of the above | |
- 54 What are the values of cells that are minimized to BDE ?
- | | | | | |
|------------------|------------------|------------------|----------------|------------------|
| a 14, 15, 30, 31 | b 11, 10, 27, 26 | c 10, 14, 26, 30 | d 2, 6, 14, 15 | e 18, 22, 26, 30 |
|------------------|------------------|------------------|----------------|------------------|
- 55 Which parameter describes a cell NOT adjacent to cell $M(i,j)$?
- | | | | | |
|--------------|--------------|--------------|--------------|---------------------|
| a $M(i,j-1)$ | b $M(i,j+1)$ | c $M(i-1,j)$ | d $M(i+1,j)$ | e None of the above |
|--------------|--------------|--------------|--------------|---------------------|
- 56 What is the sum-of-products minimization of cells in the range $9 < M(i,j) < 20$?
- | | | |
|--|--|---|
| a $A\bar{B}\bar{C} + \bar{A}BC + A\bar{B}\bar{C}D$ | b $A\bar{B}\bar{C} + \bar{A}BD + ABC\bar{D}$ | c $A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}CD$ |
| d $A\bar{B}\bar{C} + \bar{A}BC + ABD$ | e $A\bar{B}\bar{C} + \bar{A}BC + BDE$ | |
- 57 The minimization of cells described by the product $\prod_j M(i,j) \forall i = 0,1,2,3$ for $j = 6$ is
- | | | | | |
|-----------|-----------------|-----------------------|-----------------------|---------------------|
| a $C + E$ | b $\bar{C} + E$ | c $\bar{C} + \bar{E}$ | d $\bar{C} + \bar{E}$ | e None of the above |
|-----------|-----------------|-----------------------|-----------------------|---------------------|
- 58 The minimization of cells described by the sum $\sum_j M(i,j) \forall j = 0,1,2,3$ for $i = 2$ is
- | | | | | |
|--------|--------------|--------------|--------------------|---------------------|
| a BC | b $\bar{B}C$ | c $B\bar{C}$ | d $\bar{B}\bar{C}$ | e None of the above |
|--------|--------------|--------------|--------------------|---------------------|
- 59 The minimization of cells described by the sum $\sum_{i=\text{even}} \sum_{j=\text{even}} M(i,j)$ is
- | | | |
|---|---|---|
| a $A \oplus B \oplus C \oplus D \oplus E$ | b $A \downarrow B \uparrow C \uparrow D \downarrow E$ | c $A \downarrow B \downarrow C \downarrow D \downarrow E$ |
| d $A \ominus B \ominus C \ominus D \ominus E$ | e None of the above | |

- 60 Which is NOT a prime implicants of $G(a, b, c, d) = \sum(1, 4, 6, 7, 8, 9, 10, 11, 15)$
 a 7, 15 b 8, 9 c 11, 15 d 8, 9, 10, 11 e None of the above

- 61 How many essential prime implicants are in G above?
 a 0 b 1 c 2 d 3 e 4

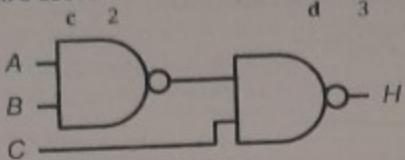


Figure 2

- 62 The function H in Figure 2 is
 a \overline{ABC} b $\overline{AB}C$ c $AB + \bar{C}$ d $AB\bar{C}$ e None of the above

- 63 If all the gates in question 62 are replaced by NOR gates then the function H becomes
 a $\overline{A+B+C}$ b $\overline{A+B} + C$ c $A+B\bar{C}$ d $A+B+\bar{C}$ e None of the above

- 64 How many NOR gates will implement a 3-input AND gate?
 a 1 b 2 c 3 d 4 e None of the above

- 65 How many NAND gates will implement a 3-input NOR gate?
 a 1 b 2 c 3 d 4 e None of the above

- 66 How many XNOR gates are in a 4-bit odd parity checker? Assume only XOR and XNOR gates are used.
 a 1 b 2 c 3 d 4 e None of the above

- 67 Two binary numbers in 2's complement $X = 1010100$ and $Y = 1000011$ produce the result 1101111 from which of the following operations:
 a $X - Y$ b $-X - Y$ c $Y - X$ d $-Y - X$ e None of the above

- 68 A full adder has three inputs, A , B and C . If C is the carry in signal then the carry out signal is generated by one of the following, assume $G = AB$ and $P = A \oplus B$
 a $P \oplus C$ b $PG + C$ c $G + PC$ d $G \oplus C$ e None of the above

- 69 A 1-bit comparator compares has two inputs x and y and three outputs $A = x\bar{y}$, $B = \bar{x}y$ and $C = x \oplus y$. AC means
 a x is less than y b y is less than x c x is less than or equal y
 d y is less than or equal x e None of the above

- 70 A decoder with enable input can function as a
 a encoder b demultiplexer c multiplexer d multiplier e None of the above

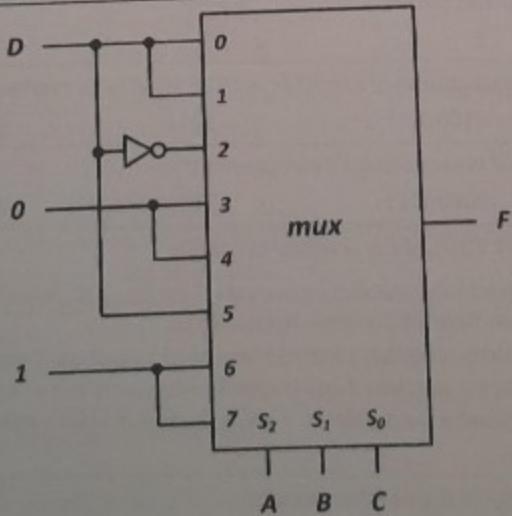


Figure 3

- 71 The function F in Figure 3 is
 a $\sum(0, 1, 5, 11, 12, 13, 15)$ b $\sum(0, 1, 3, 4, 6, 12, 13, 15)$ c $\sum(1, 3, 4, 6, 12, 13, 14, 15)$

- d $\sum(1, 3, 4, 11, 12, 13, 14, 15)$ e None of the above

- 72 A 4 to 1 line multiplexer can be implemented with three state buffers and a(n)
 a encoder b demultiplexer c 2 to 1 line multiplexer

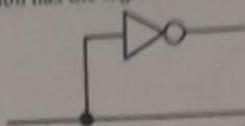
- d decoder e None of the above

Answer questions 43 to 47 with following digital functions:
 a Decoder b Demultiplexer c Encoder

d Full-Adder

e Multiplexer

- 73 Which digital function has the logic circuit realization below?

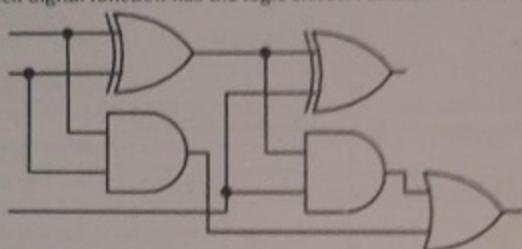


- 74 Which digital function provides the 2^n minterms of n input variables?

- 75 Which digital function has the following output equations:
 $A_0 = D_1 + D_3 + D_5 + D_7$
 $A_1 = D_2 + D_3 + D_4 + D_5$
 $A_2 = D_6 + D_7 + D_4 + D_5$

- 76 Which digital function has inputs $X_1 X_0 I_0, I_1, I_2, I_3$, and output $Y = \bar{X}_1 \bar{X}_0 I_0 + \bar{X}_1 X_0 I_1 + X_1 \bar{X}_0 I_2 + X_1 X_0 I_3$

- 77 Which digital function has the logic circuit realization below?



- 78 The signed 2's complement of -8 in an eight bit computer is

- a 11111000 b 11110000 c 11111001 d 11110111 e None of the above

- 79 The subtraction of two n -digit unsigned number can be done by the algorithm below as follows:

- 1 Add the 2's complement of the subtrahend to the minuend.
- 2 If the sum produces a carry, discard the carry, go to 4.
- 3 Take the 2's complement of the sum.
- 4 End

Which steps of the algorithm has errors?

- a 1 b 2 c 3 d 1 and 3 e None of the above

- 80 If the signed magnitude representation of a number is 1011, what is its representation in signed 2's complement?

- a 1110 b 1100 c 1011 d 1100 e None of the above

- 81 What is $-6 + (-19)$ in signed binary using 1's complement?

- a 00010011 b 00000111 c 11111001 d 11101100 e None of the above

- 82 Which of the following is NOT TRUE of the overflow condition:

- a If the sum of two unsigned n -bit numbers generates 0 for $C_{n-1} \otimes C_n$ where C_{n-1} and C_n are carry in and carry out of the n -bit position of the sum, then an overflow has occurred.
- b Overflow is a problem with computers and can lead to computational errors if not monitored.
- c Overflow exceptions can be monitored and trapped using hardware or software.
- d If the sum of two n -bit numbers occupies $n + 1$ bits then an overflow has occurred.
- e None of the above

- 83 Which of the following is TRUE of sequential circuits?

- a Sequential circuits receive binary information from their environment via inputs. These inputs determine the next state of the sequential circuits and the binary values of their outputs.
- b The behaviour of a synchronous sequential circuit depends on its inputs and the order the inputs change at any instant in time.
- c Complex synchronous sequential circuits are difficult to design since their behaviour is highly dependent on the delays and on the timing of the input changes.
- d The storage elements used in the simplest form of clocked sequential circuits are called flip-flops. Each flip-flop can be in any of 2^n states if it has n inputs.
- e None of the above.

- 84 The $\bar{S}\bar{R}$ latch has two cross-coupled

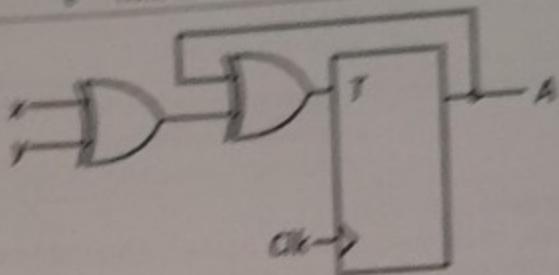
- a NOR gates b AND gates c NAND gates d OR gates e XOR gates

- 85 When all three inputs of ONE of the following latches are equal to 1 it is placed in an indeterminate state.
- a SR latch
 - b $\bar{S}\bar{R}$ latch
 - c clocked SR latch
 - d clocked $\bar{S}\bar{R}$ latch
 - e None of the above
-
- 86 Flip-flops are preferred to clocked latches as storage elements in sequential circuits for ONE of the following reasons:
- a Latches are complex
 - b Latches have variable delay
 - c Latches are transparent
 - d Latches need a clock
 - e Latches may inadvertently be placed in an indeterminate state
-
- 87 Which of the following statements is (are) TRUE?
- I Two states of a sequential circuit are equivalent if the output produced for each input symbol is identical and the next states for each input symbol are the same or equivalent.
 - II Sequential circuits in which the outputs depend on the states is referred to as Mealy model circuits.
 - III Edge-triggered flip-flops change state during the transition of the clock signal.
 - IV Sequential circuits in which the outputs depend on the inputs as well as on the states is referred to as Moore model circuits.
 - V State reduction through state equivalence may or may not result in reduced circuit costs.
- a II & IV
 - b I, II & IV
 - c I, II & III
 - d I, III & V
 - e II, III & IV
-
- 88 Which of the following is NOT CORRECT?
- a The state of a SR latch with two cross-coupled NOR gates is indeterminate if both inputs are 1.
 - b Storage elements controlled by clock transitions are referred to as latches.
 - c A reduction in the number of states of a sequential circuit may not result in a reduction in the number of flip-flops used in its design.
 - d Asynchronous inputs are used to force synchronous flip-flops into a particular state independent of the clock.
 - e None of the above
-
- 89 A sequential circuit has one flip-flop Q , two inputs X and Y , and one output S . the circuit consists of a D flip-flop with S as its output and logic implementing the function $D = \bar{X}Z + \bar{Y}Z + XY\bar{Z}$, with D as the input to the D flip-flop. If the flip-flop is set which of the following values of X and Y will reset it?
- a 0, 0
 - b 0, 1
 - c 1, 0
 - d 1, 1
 - e All of the above
-
- 90 Phases in the design of sequential circuits are listed below in alphabetical order.
- | | | |
|----------------------------------|---------------------------------|---------------------|
| I Formulation | II Input Equation Determination | III Optimization |
| IV Output Equation Determination | V Specification | VI State Assignment |
| VII Technology Mapping | VIII Verification | |
- Which of the following ordering of phases is the CORRECT procedure for sequential circuit design?
- a I, V, II, IV, VI, III, VII, VIII
 - b I, VI, II, IV, V, III, VII, VIII
 - c V, VI, I, II, IV, VII, III, VIII
 - d I, V, II, IV, VI, VII, III, VIII
 - e V, I, VI, II, IV, III, VII, VIII
-
- 91 A synchronous sequential circuit S with a single D flip-flop labelled A , has an input equation $A(t+1) = A(t) \oplus X$. If external input $X = 1$ which of the following is the CORRECT output sequence of S after 5 clock pulses?
- a 1, 1, 1, 1, 1 ...
 - b 1, 0, 0, 0, 0 ...
 - c 0, 1, 1, 1, 1 ...
 - d 0, 0, 0, 0, 0 ...
 - e 1, 0, 1, 0, 1 ...
-
- 92 Which of the following distinguishes a Mealy type Finite State Machine (FSM) from a Moore type?
- a In the Mealy model the output is a function of the input only.
 - b In the Moore model the output is a function of the input only.
 - c In the Mealy model the output is a function of the present state and the input.
 - d In the Moore model the output is a function of the present state and the input.
 - e None of the above.
-
- 93 Which of the following is NOT CORRECT about sequential circuits?
- a A sequential circuit is specified by a time sequence of inputs, outputs and internal states.
 - b The behaviour of an asynchronous sequential circuit can best be defined from the knowledge of its input signals at discrete instants in time.
 - c The storage elements commonly used in asynchronous sequential circuits are time-delay devices.
 - d The storage elements used in synchronous circuits are flip-flops.
 - e Asynchronous sequential circuits can be unstable at times.
-
- 94 A Master-slave flip-flop constructed with two D flip-flops is triggered by the
- a negative edge of the synchronizing clock pulse
 - b positive edge of the synchronizing clock pulse
 - c negative level of the synchronizing clock pulse
 - d positive level of the synchronizing clock pulse
 - e None of the above
-
- 95 Which of the following flip-flops is constructed from a clocked SR latch, an inverter and an XOR gate?
- a D latch
 - b JK flip-flop
 - c Edge triggered D latch

96 a T flip-flop

c None of the above

96



Which of the following is the state equation of the sequential circuit shown above?

- a $A(t+1) = A \oplus x \oplus y$
b $A(t+1) = x \oplus y$
c $A(t+1) = x \otimes y$

- b $A(t+1) = x \oplus y$
e None of the above

- c $A(t+1) = T \oplus x \oplus y$

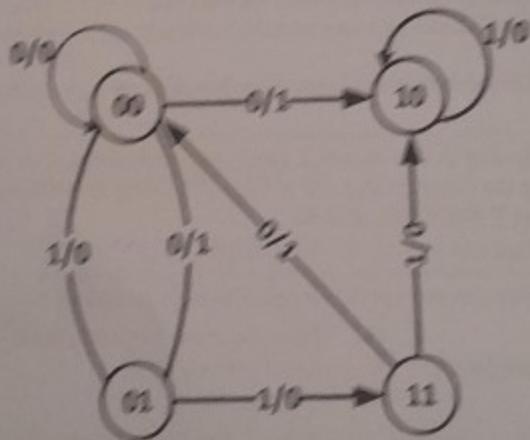
97 If the T flip-flop in question 96 is replaced with a D flip-flop the state equation becomes

- a $A(t+1) = A \oplus x \oplus y$
b $A(t+1) = x \oplus y$
d $A(t+1) = x \otimes y$

- b $A(t+1) = x \oplus y$
e None of the above

- c $A(t+1) = D \oplus x \oplus y$

A sequential circuit with two D flip-flops A and B has the state diagram below. Answer questions 98 to 100 with the options that follow:



a $\overline{AB}x$

b $(A+B)x$

c $\overline{T}x$

d $(A+B)\bar{x}$

e None of the above

98 What is the output equation?

99 What is the state equation of flip flop A?

100 What is the state equation of flip flop B?