CADD ASSIGNMENT

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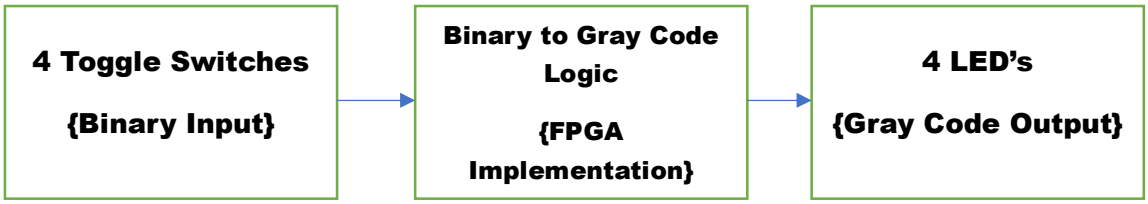
1. **Problem Statement:** To Design and implement Binary to Gray code Using Xilinx Vivado and FPGA Board.

2. **Idea About your Problem:** This project focuses on converting a 4-bit binary input into a 4-bit Gray code output using an FPGA. The goal is to design a digital system that implements the Binary-to-Gray code conversion logic efficiently and outputs the results in real-time. The output can be displayed using LEDs or sent to other external interfaces for further processing.

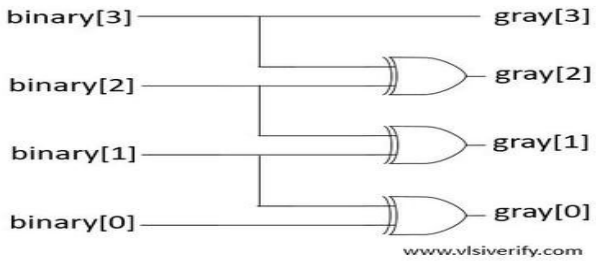
3. **Block Diagram:**



4. **Binary to Gray Code Truth Table:**

Decimal numbers	Binary code	Gray code
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

5. Circuit Diagram:



Binary to Gray Code Converter

6. D.sv:

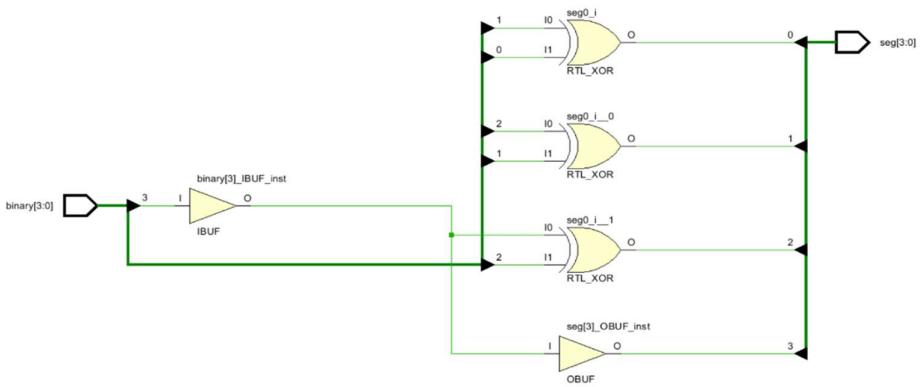
```
module TopModule (
   input logic [3:0] binary,    // 4-bit binary input
   output logic [3:0] seg      // 4-bit Gray code output
);

   // Binary to Gray code conversion logic
   always_comb begin
      seg[3] = binary[3];
      seg[2] = binary[3] ^ binary[2];
      seg[1] = binary[2] ^ binary[1];
      seg[0] = binary[1] ^ binary[0];
   end

endmodule
```

7. Tb.sv:

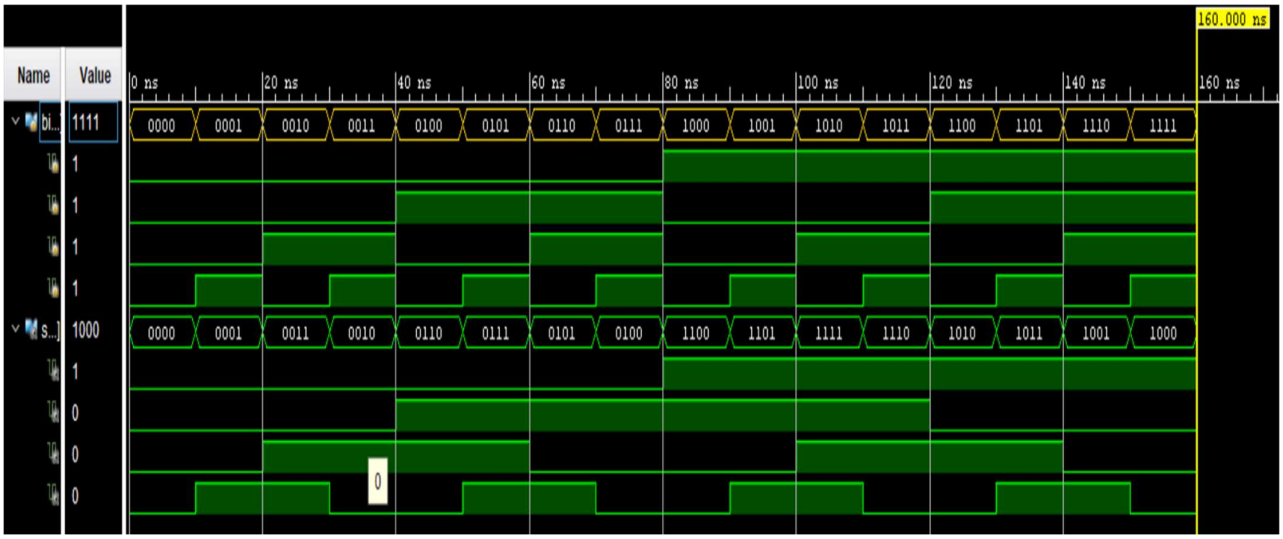
```
 `timescale 1ns / 1ps

 module TopModule_tb;

    logic [3:0] binary; // 4-bit binary input for testing
    wire [3:0] seg;    // 4-bit Gray code output

    // Instantiate the TopModule
    TopModule uut (
       .binary(binary),
       .seg(seg)
    );

    initial begin
       $monitor("Time=%0t | Binary=%b | seg=%b", $time, binary, seg);

       // Test a sequence of binary inputs
       binary = 4'b0000; #10;
       binary = 4'b0001; #10;
       binary = 4'b0010; #10;
       binary = 4'b0011; #10;
```

```
        binary = 4'b0100; #10;
        binary = 4'b0101; #10;
        binary = 4'b0110; #10;
        binary = 4'b0111; #10;
        binary = 4'b1000; #10;
        binary = 4'b1001; #10;
        binary = 4'b1010; #10;
        binary = 4'b1011; #10;
        binary = 4'b1100; #10;
        binary = 4'b1101; #10;
        binary = 4'b1110; #10;
        binary = 4'b1111; #10;

        $stop; // End simulation
    end

endmodule
```

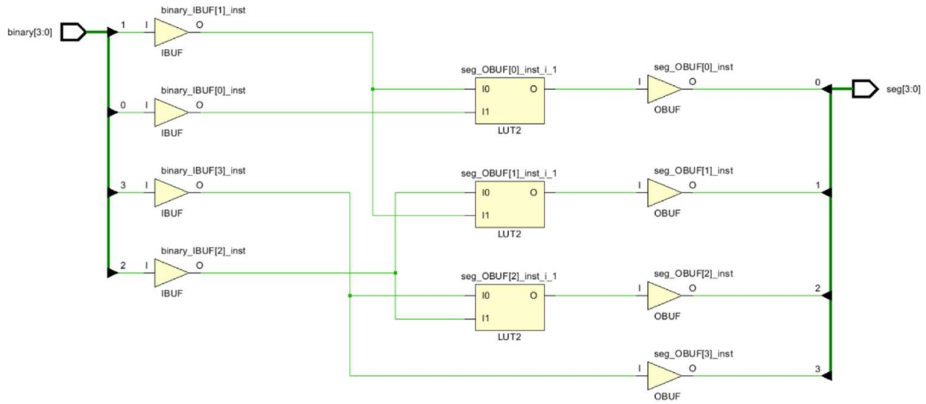
8. RTL schematic:



9. Run Simulation:



10. Synthesis Schematic:



11. Utilization Report:

Name	Slice LUTs (20800)	Bonded IOB (106)
TopModule	2	8

12. XDC File:

```
set_property IOSTANDARD LVCMOS33 [get_ports {binary[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {binary[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {binary[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {binary[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {seg[0]}]
set_property PACKAGE_PIN R2 [get_ports {binary[3]}]
set_property PACKAGE_PIN T1 [get_ports {binary[2]}]
set_property PACKAGE_PIN U1 [get_ports {binary[1]}]
set_property PACKAGE_PIN W2 [get_ports {binary[0]}]



set_property PACKAGE_PIN P1 [get_ports {seg[2]}]
set_property PACKAGE_PIN L1 [get_ports {seg[3]}]
set_property PACKAGE_PIN N3 [get_ports {seg[1]}]


set_property PACKAGE_PIN P3 [get_ports {seg[0]}]
```

13. Conclusion:- To Design and implement Binary to Gray code Using Xilinx Vivado and FPGA Board is implemented and verified successfully.