**CMOS Digital-to-Analog and Analog-to-Digital Converter Design**

**4-bit SAR ADC building blocks and design**

1. **Introduction**

1.5 V 4-bit SAR ADC is designed, and its characteristics measured. The design blocks are detailed below.

1. **Analog Blocks**
2. **[Comparator]**

**Description:**

To achieve the common-mode range of 0.1-1.4 V and rail-to-rail swing, the two amplifier blocks are cascaded (Fig.1). The amplifier block is shown in Fig.2.

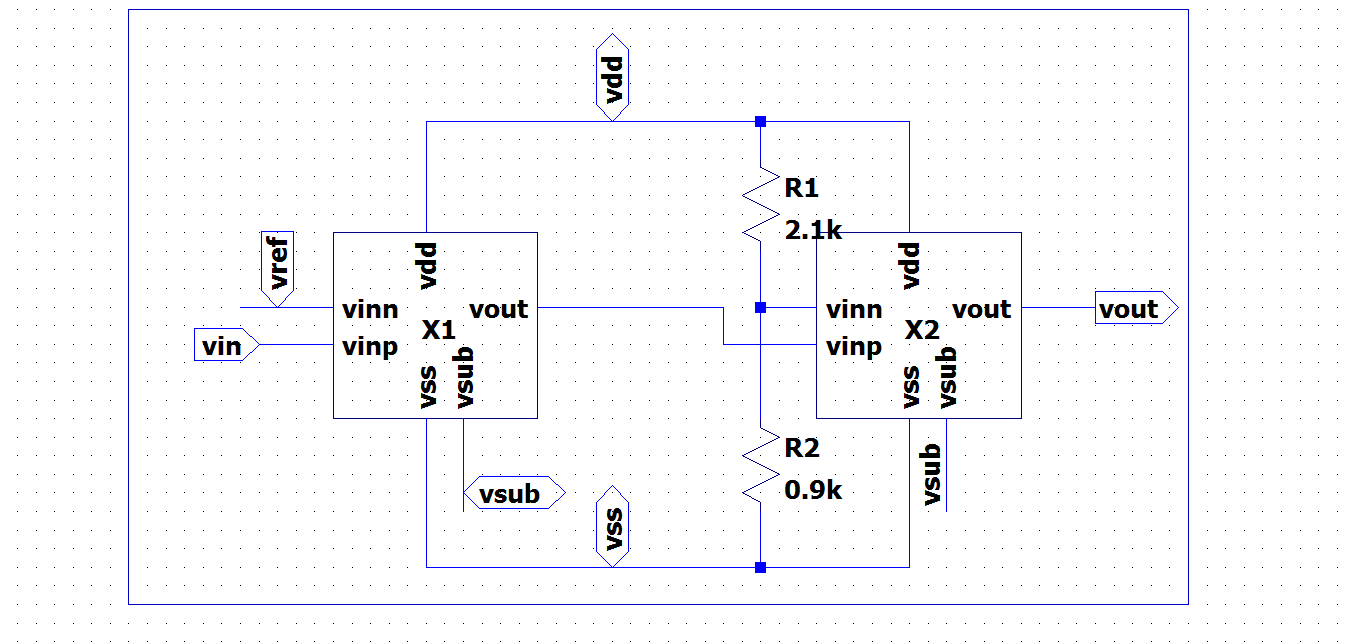
The voltage gain is controlled by the input devices M3-M4. The output resistance is controlled by the devices M7-M10. Increasing the length of these devices, affects the voltage gain, by increasing the output impedance. Keeping large input devices, increases the offset of the Comparator. Hence the size of M3-M4 was reduced.

Transistors have been sized according to the table below.

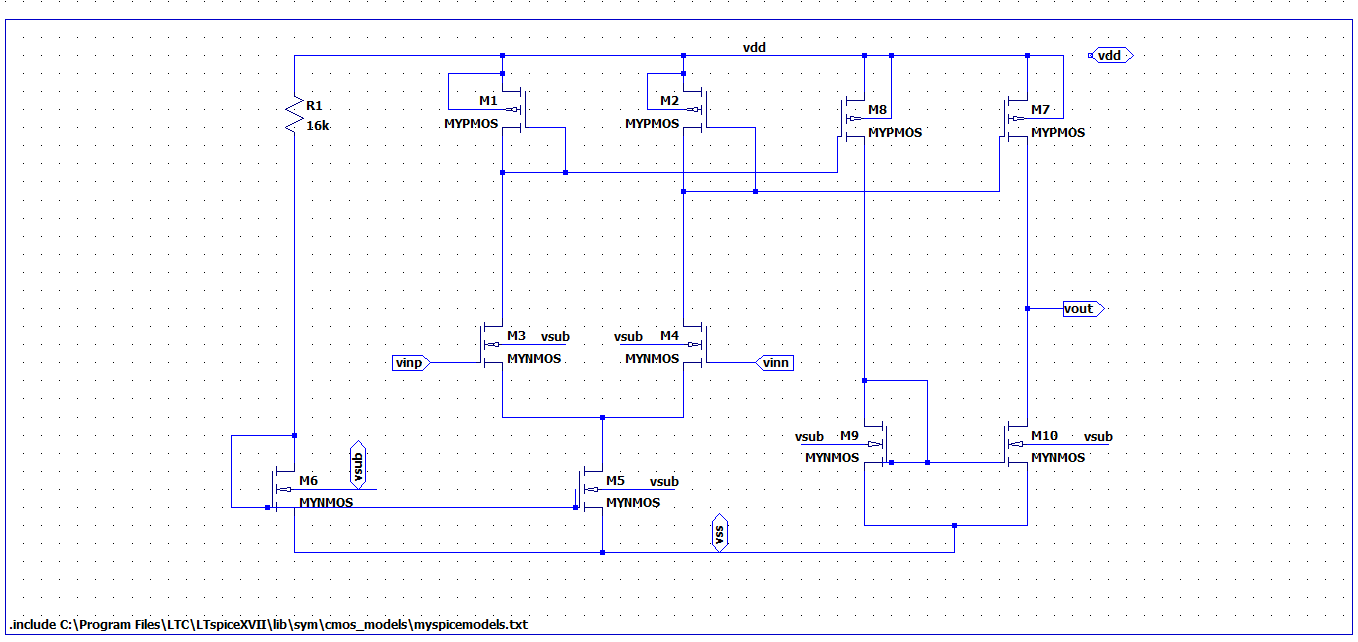
|  |  |  |  |
| --- | --- | --- | --- |
| **Transistor** | **W/L [µm/µm]** | **M[multiplier]** | **IB [µA]** |
| M1 | 1.2/0.18 | 2 | 0-51 |
| M2 | 1.2/0.18 | 2 | 0-51 |
| M3 | 1.2/0.18 | 3 | 0-51 |
| M4 | 1.2/0.18 | 3 | 0-51 |
| M5 | 10/3 | 2 | 51 |
| M6 | 10/3 | 2 | 51 |
| M7 | 1.2/0.25 | 2 | 20 |
| M8 | 1.2/0.25 | 2 | 20 |
| M9 | 1.2/0.25 | 1 | 20 |
| M10 | 1.2/0.25 | 1 | 20 |

Table 1: Comparator transistor sizes.

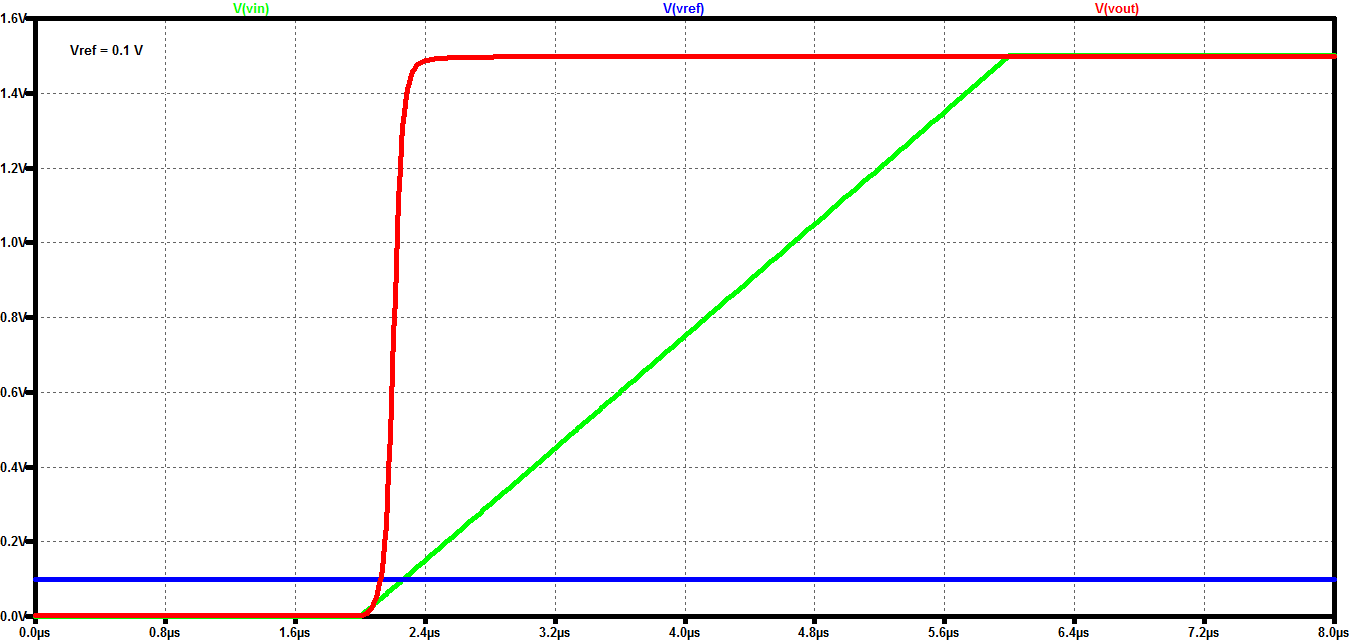
The resistors R1 = 2.1k and R2 = 0.9k were sized to generate the required over-drive for the entire common mode range to achieve rail-to-rail swing. The comparator response to the various inputs is depicted in figures 4-5-6. For the 1.4V case, the comparator output does not swing all the way to a high, due to insufficient gain. Having a relatively low gain helps in combating mis triggers, for the ADC as a system. In hindsight, the size of the tail transistors can be reduced, to save area.



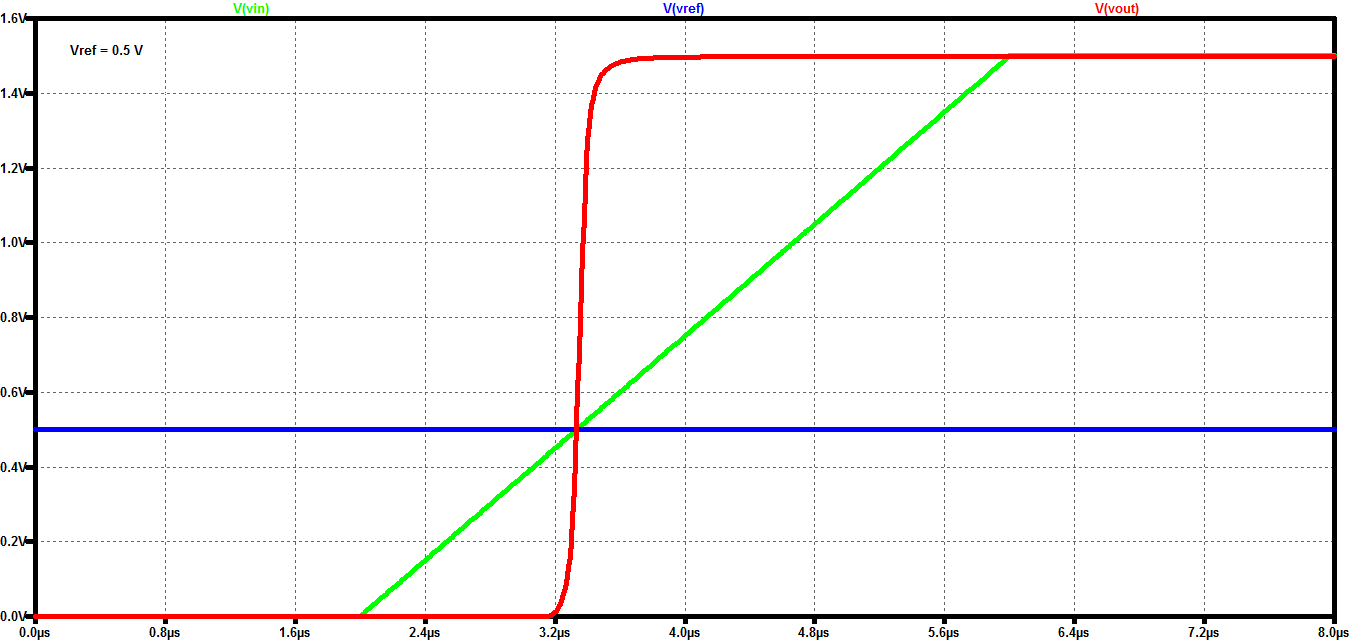
*Figure 1: Two-stage cascaded NMOS comparator*



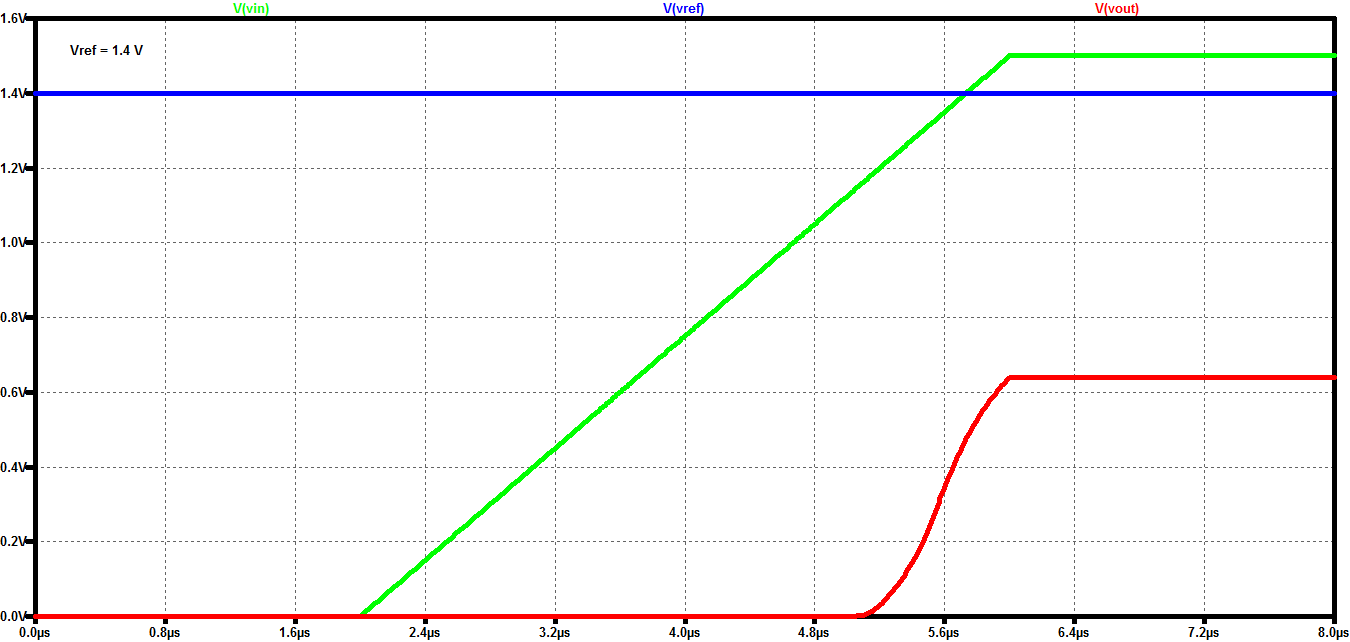
*Figure 2: NMOS input, with single ended output*



*Figure 4: Comparison with Vref=0.1V*



*Figure 5: Comparison with Vref=0.5V*

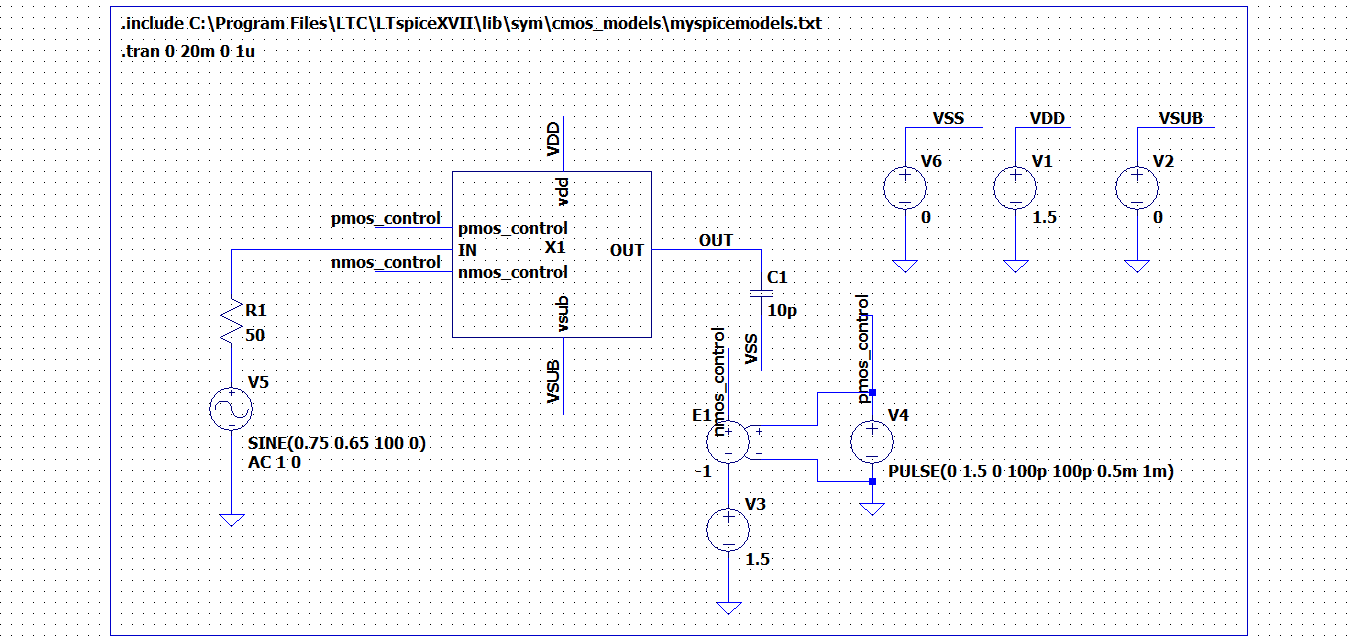


*Figure 6: Comparison with Vref = 1.4V*

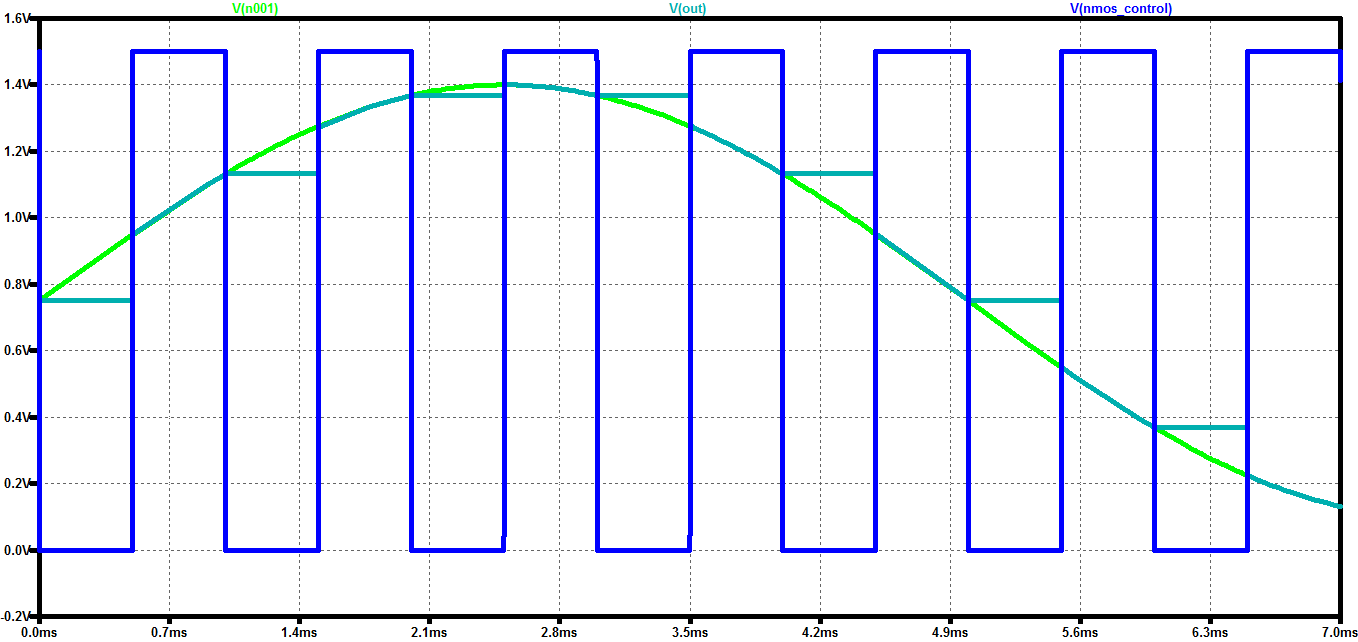
1. **[Sample and Hold Circuit]**

**Description:**

The sample and hold switch consist of a CMOS transmission gate, with independent PMOS and NMOS gate control. An external capacitor (in this case of 20pF) needs to be added at the output the TX gate, for reducing the voltage droop.



*Figure 7: Test bench for sample and hold*

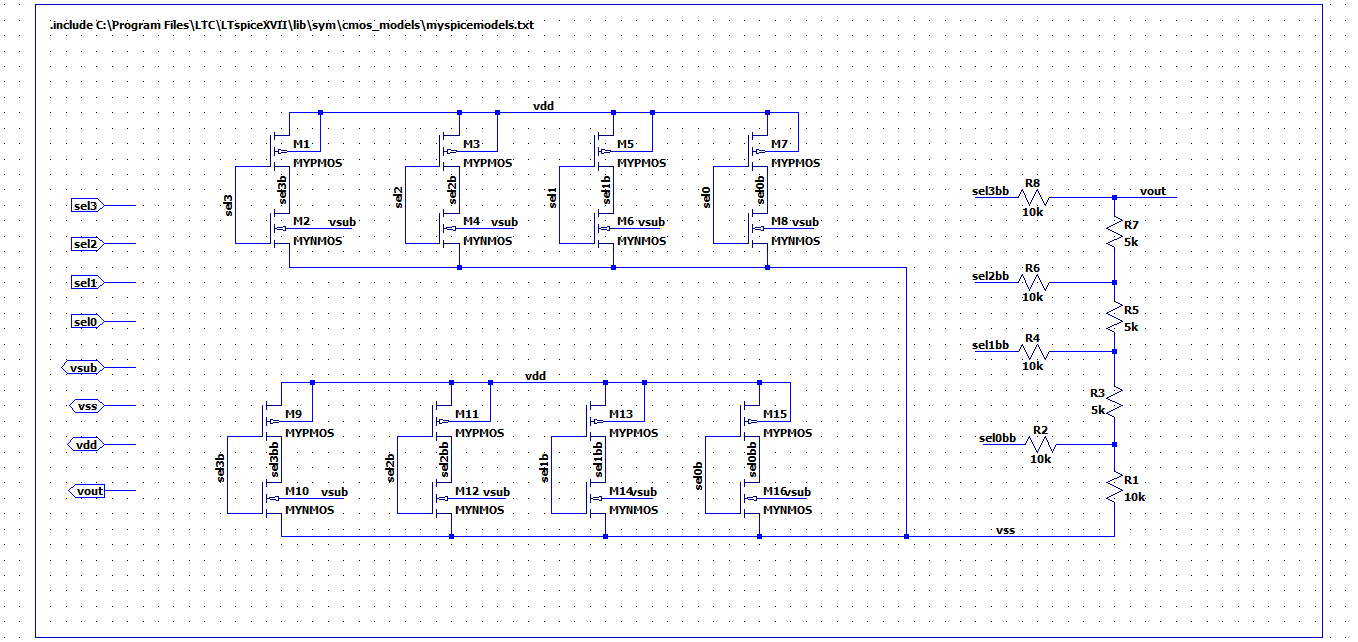


*Figure 8: Sample and hold waveform*

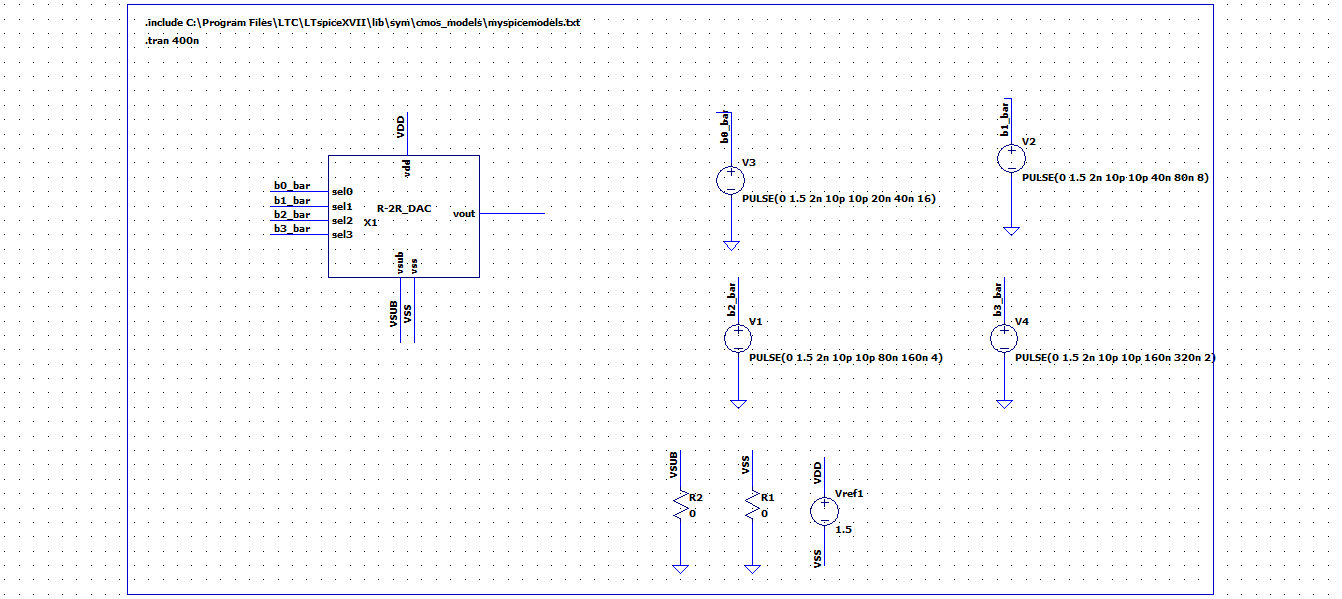
1. **[R-2R DAC]**

**Description:**

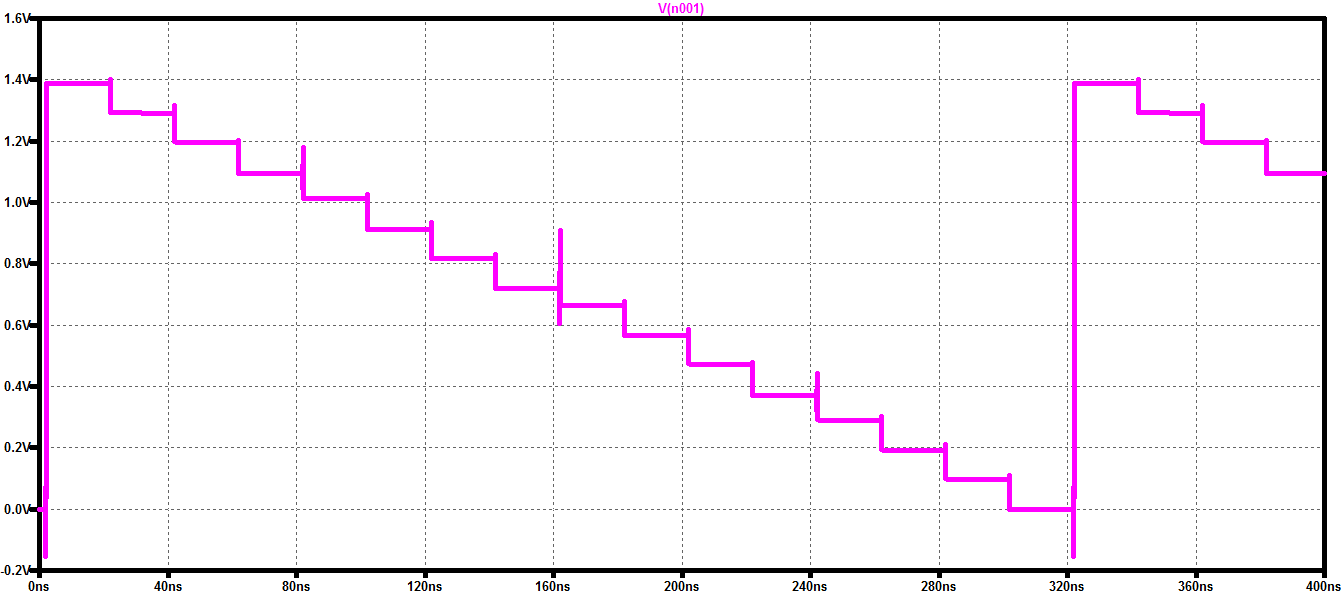
To generate the reference voltages for comparison, an R-2R DAC is utilized. The schematic is shown in Fig.9. By connecting R2-R4-R6-R8 to either vdd or vss the required voltages can be generated. This can easily be verified with the help of superposition. The CMOS switches are made wide to offer negligible resistance when closed. The code word sweep of the DAC is shown in Figure 11.



*Figure 9: R-2R DAC*



*Figure 10: Test-bench for evaluating the R-2R DAC*



*Figure 11: Control code sweep of the R-2R DAC*

|  |  |
| --- | --- |
| Control Code | Voltage recorded |
| 0000 | 3.1uV |
| 0001 | 97mV |
| 0010 | 190mV |
| 0011 | 290mV |
| 0100 | 370mV |
| 0101 | 470mV |
| 0110 | 564mV |
| 0111 | 664 mV |
| 1000 | 719mV |
| 1001 | 818mV |
| 1010 | 913mV |
| 1011 | 1.01V |
| 1100 | 1.09V |
| 1101 | 1.19V |
| 1110 | 1.28V |
| 1111 | 1.38V |

*Figure 12: Control voltage sweep*

The odd voltage spike seen around 160ns is when the MSB turns on and there is directly coupling between the output and the voltage source.

1. **Digital Blocks**
2. **[D-FlipFlop]**

**Description:**

The behavioral model of the flip flop already exists in the LTspice digital library. Buffers are added at the output, to get electrical domain signals. The schematic is shown in Figure 12.

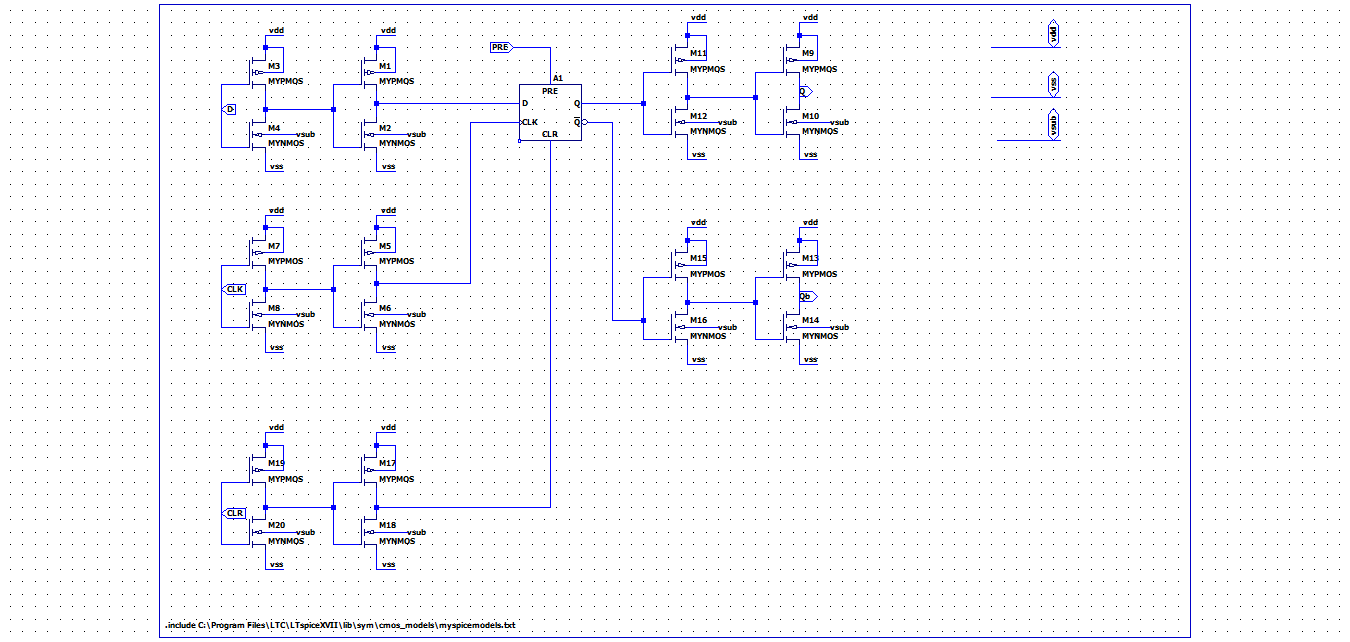


Figure 12: D-Flipflop

1. **[Clock-generator]**

**Description:**

The clock-generator outputs a phase-shifted select signals. The schematic is shown in Figure 13. The test bench outputs are shown in Figure 14. The test bench is shown in Figure 15.

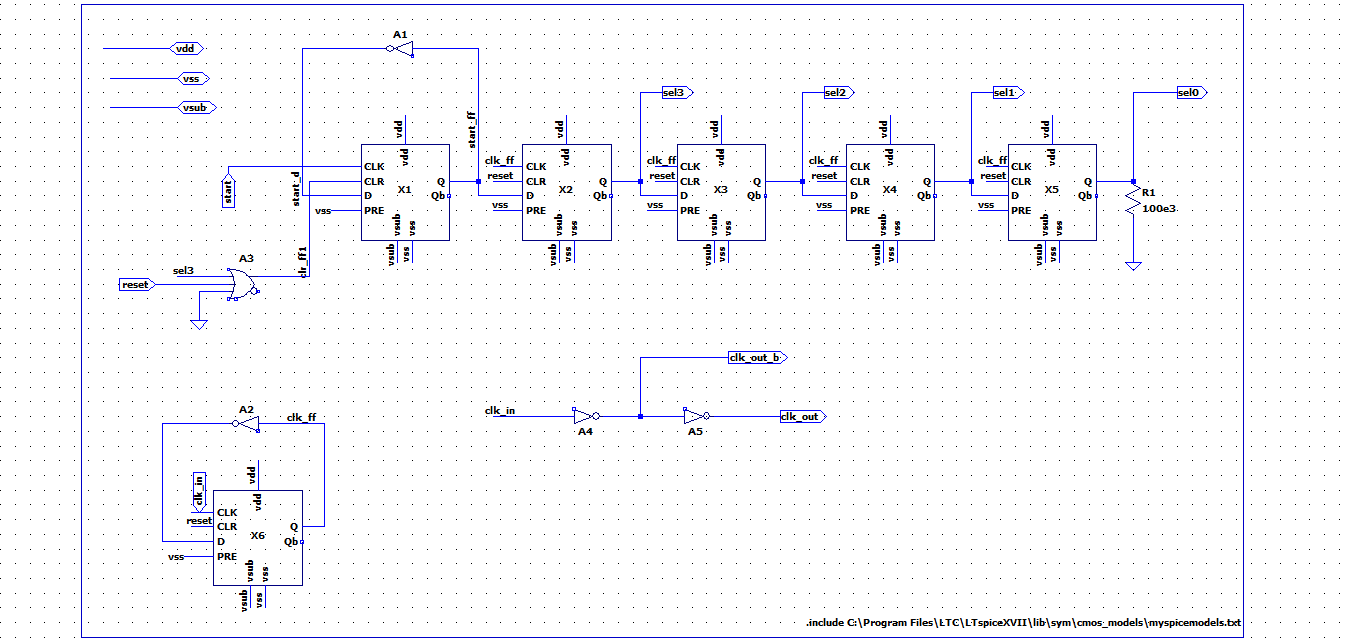


Figure 13: Clock generator for phase-shifted outputs

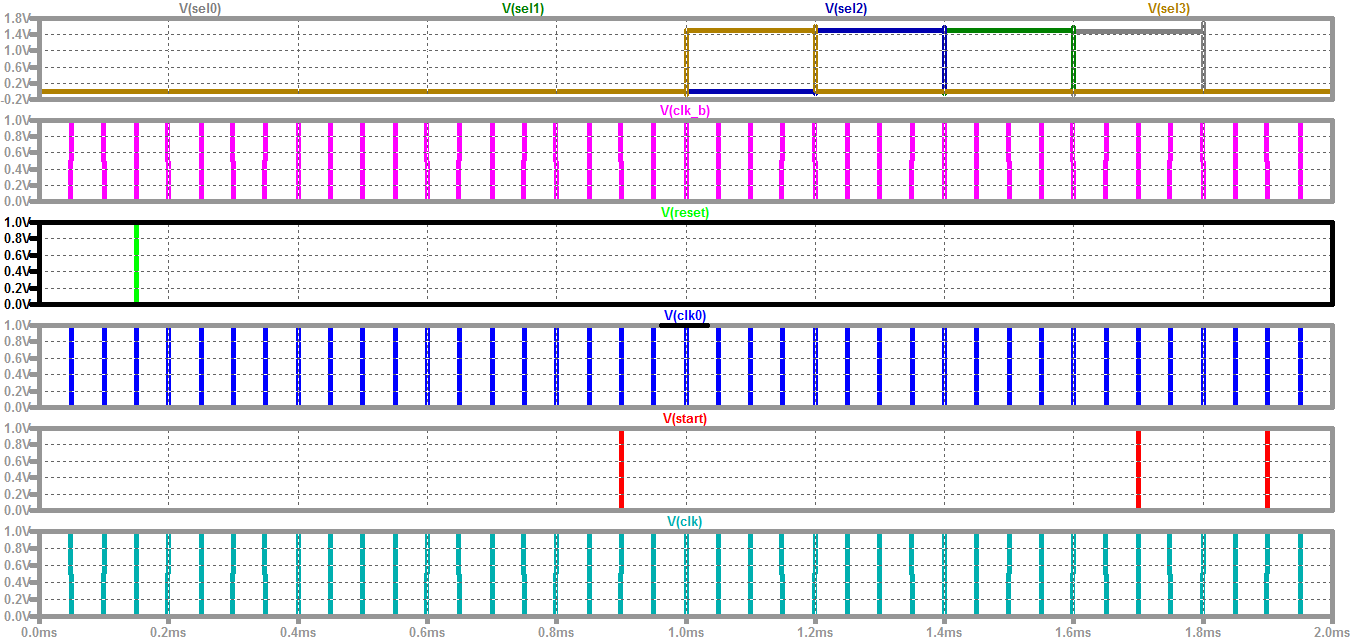


Figure 14: Test-Bench outputs for the evaluation of the clock generator.

1. **[2-to-1 Multiplexer]**

**Description:**

The schematic is shown in figure 16. Out = sel\*(Abar) + selbar \*(Bbar).

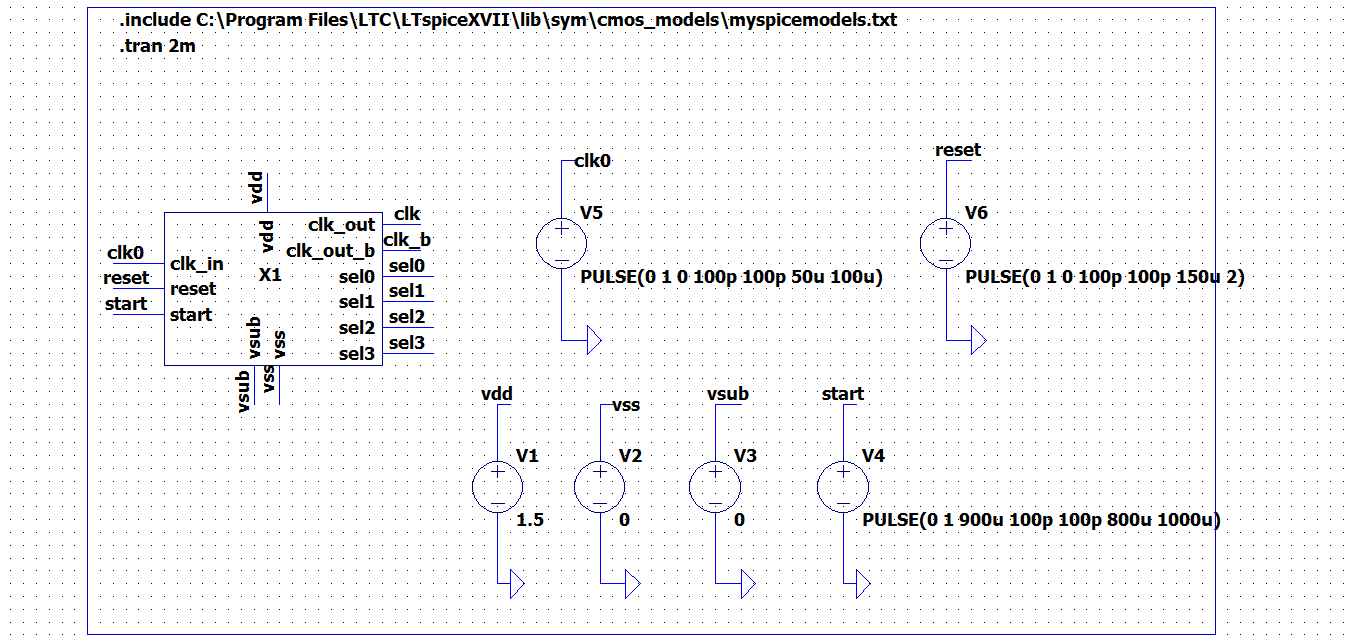


Figure 15: Test bench for evaluating the clock generator.

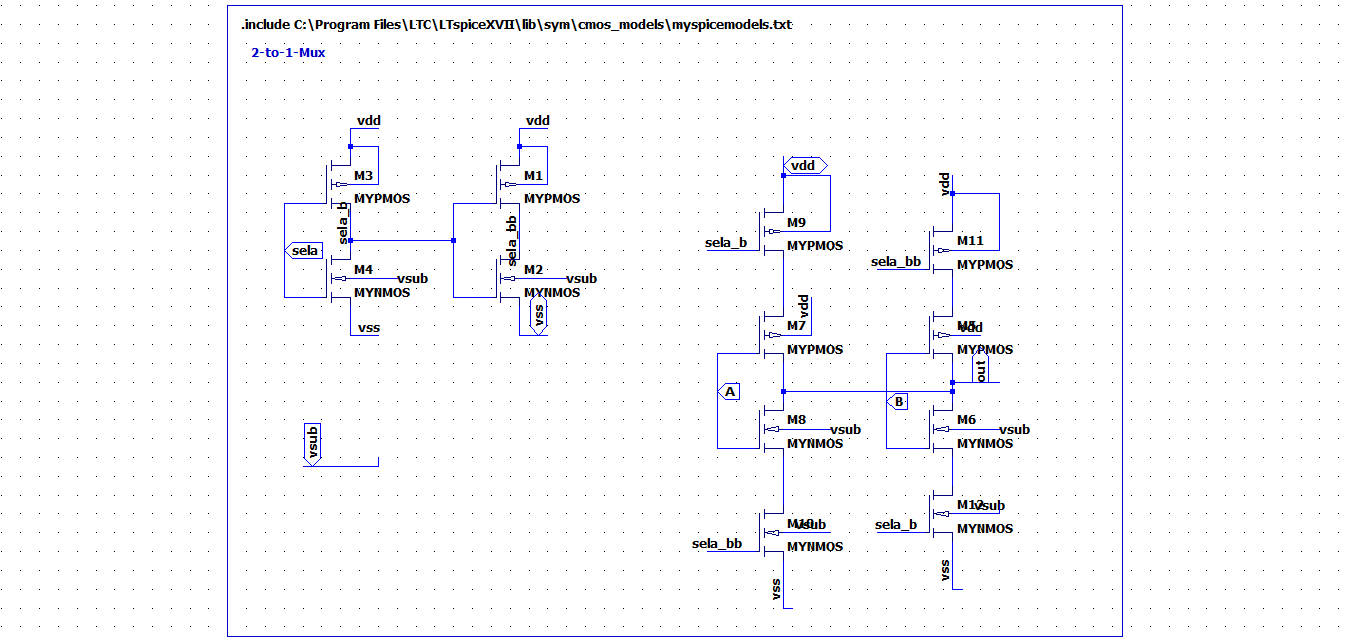


Figure 16: 2:1 Multiplexer

The SAR logic block is shown in figure 17.

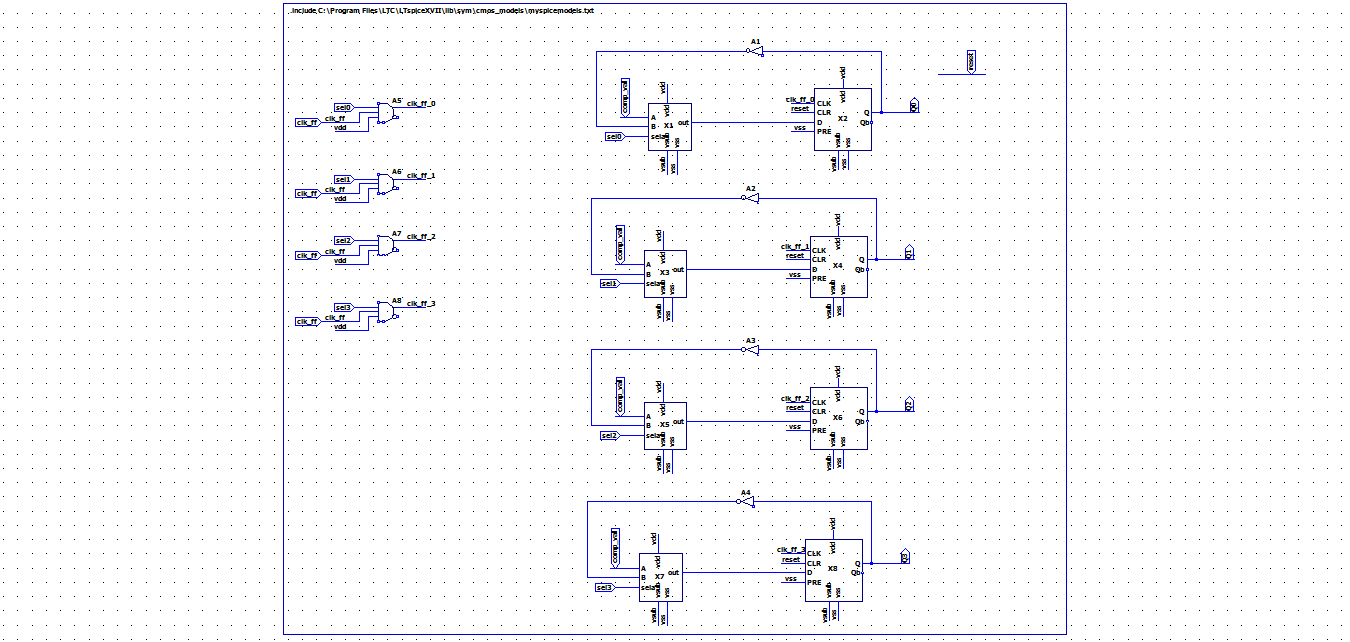


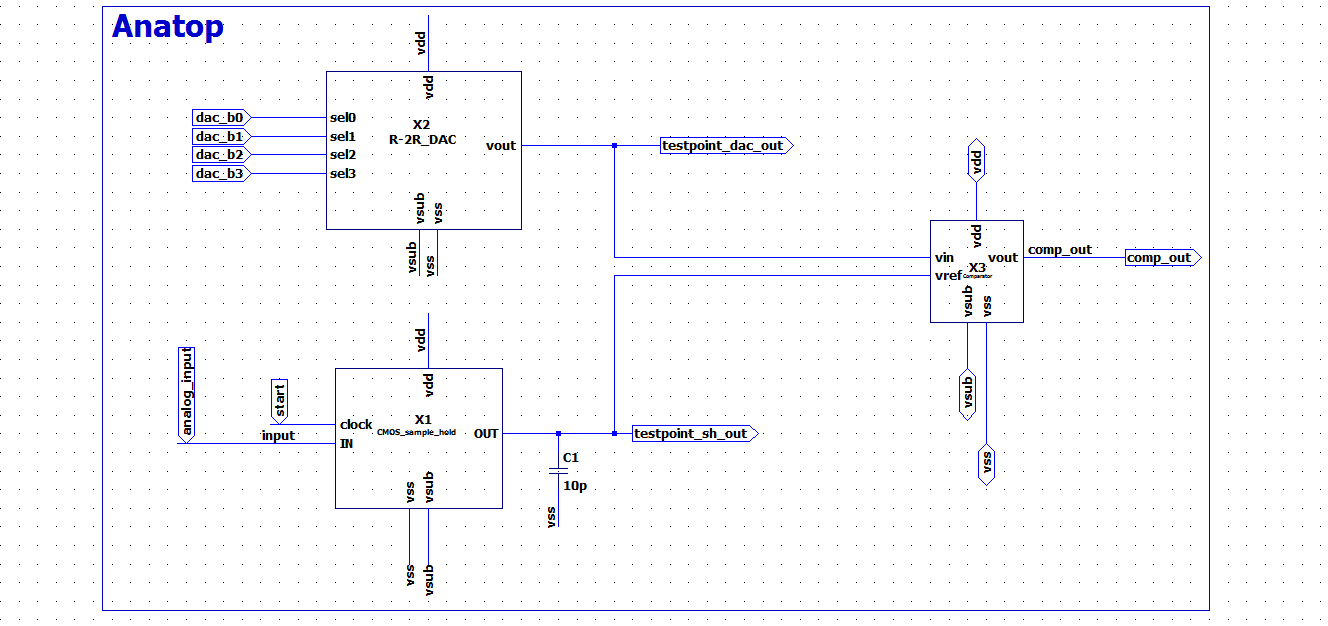
Figure 17: SAR Logic block

**4.Top-level**

**a. [Anatop]**

**Description:**

This block primarily compares the digital output and the sampled input. Here the comparison is as follows: comp\_out = (dac\_out > sh\_out)? 1:0. A 10pF capacitor is externally added to the CMOS sample and hold to increase the hold time and reduce voltage droop. The “start” pin going high, indicates the beginning of the hold mode.



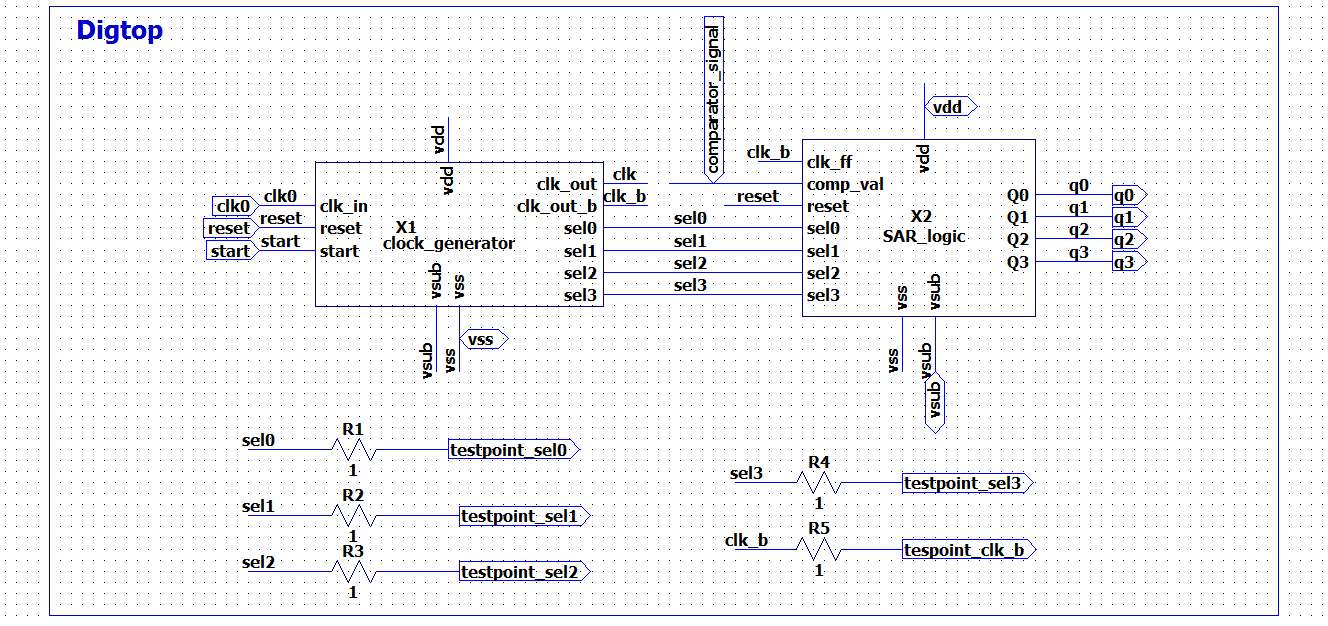


Figure 18: Top level digital blocks. The clock generator and the SAR logic are included.

**b. [Digtop]**

**Description:**

Shown in Fig.18 are the primary blocks associated with the digital logic. The externally generated clk0 drives the sequential logic. This block is responsible for generating the output code of the sampled analog signal, with q3 being the MSB of the code. The select bits control the bit position of the analog to digital conversion. For example, when Sel3 goes high the MSB(q3) of the digital code is being decided. Both the clock generator and the SAR logic are being controlled by the common reset signal.

**[SAR ADC top]**

**Description:**

The ADC top level is shown in Fig.19. The digital code generated in dig-top drives the R-2R DAC. The comparator output is fed back to the digital. The power domains of the analog and the digital are separated to provide noise isolation. An externally generated clock drives the SAR state machine. To ease the droop requirements on the sample and hold circuit, the conversion speed can be increased by increasing the clock frequency.

**[Test bench]**

**Description:**

The top-level test bench is shown in Fig20. A 10kHz- externally generated clock is used for the SAR ADC. The reset signal is applied initially followed by the start signal. Two conversion examples are described below.

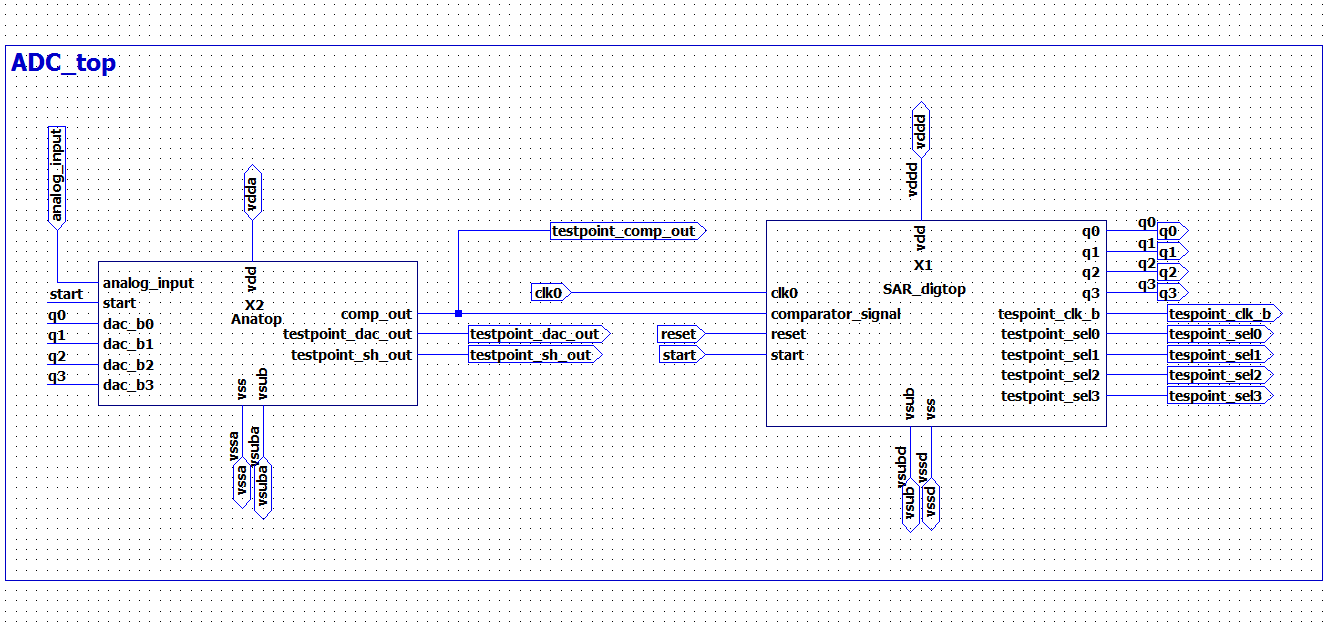


Figure19: 4-bit SAR ADC top.

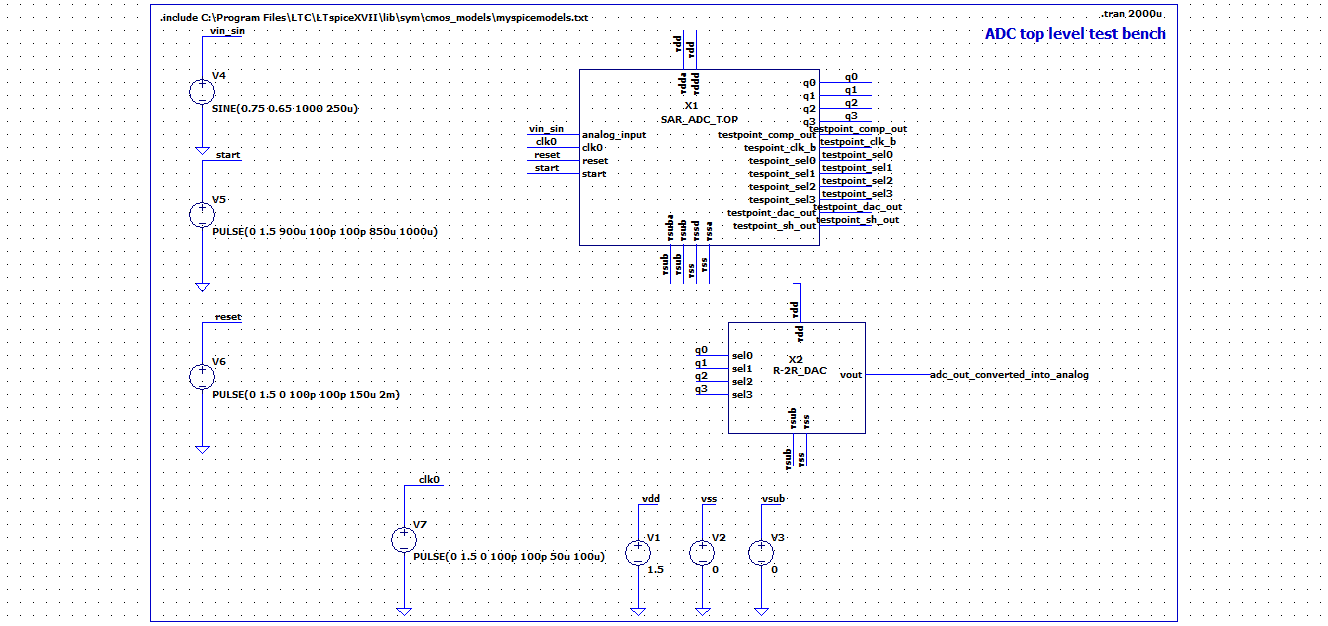


Figure 20: 4bit-SAR ADC top level test bench

**Conversion Example -1**

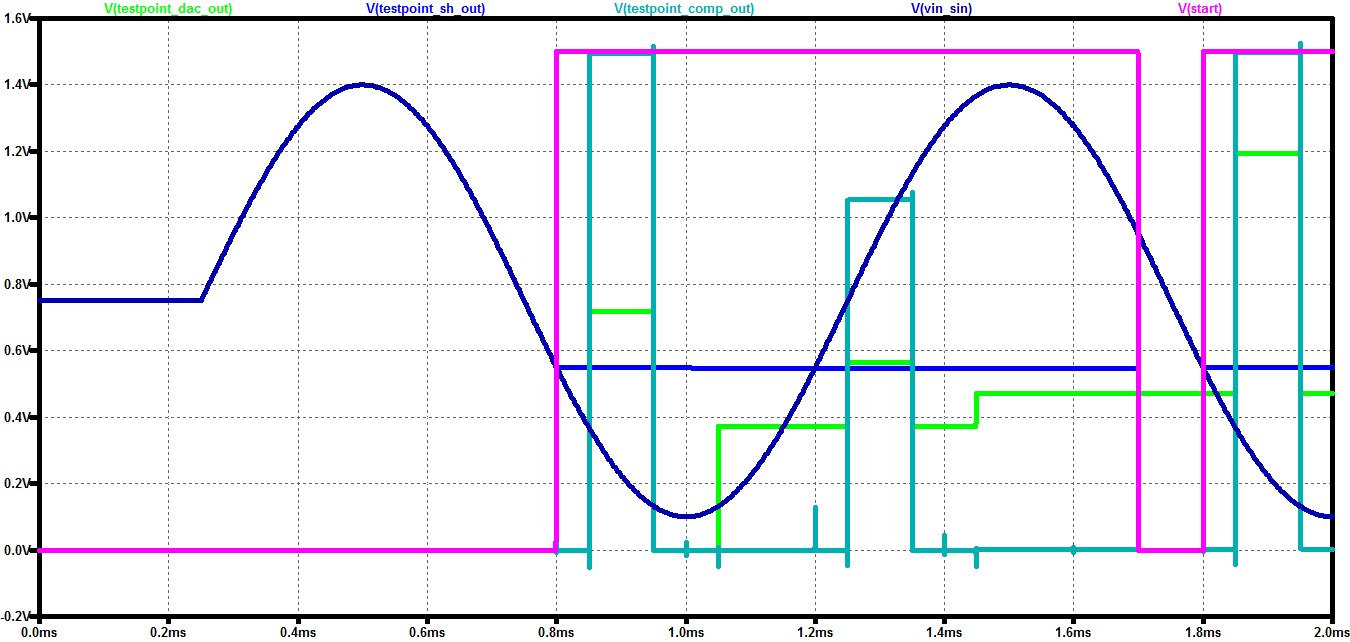


Figure 21: Analog input: 550.34 mV. DAC output Code: 0101

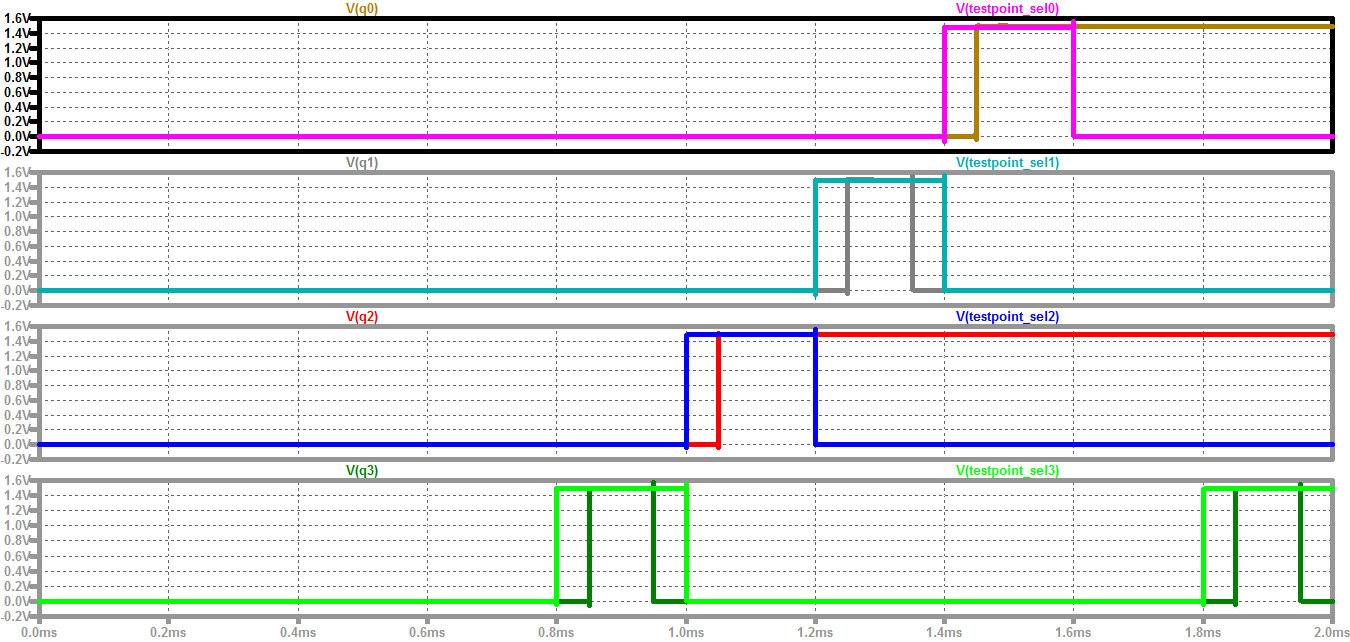


Figure 22: Conversion Sequence for analog input of 550.3 mV.

The above conversion is elucidated in the table below.

Analog Input : 550.3 mV. DAC output: 0101

|  |  |  |
| --- | --- | --- |
| Select-Cycle | DAC output (mV) | Decided bit |
| 3 | 719.46 | Comparator is high. Q3 = 0 |
| 2 | 370.81 | Comparator is low. Q2 = 1 |
| 1 | 564.78 | Comparator is high. Q1= 0 |
| 0 | 470.1 | Comparator is low. Q0 = 1 |

**Conversion Example -3**

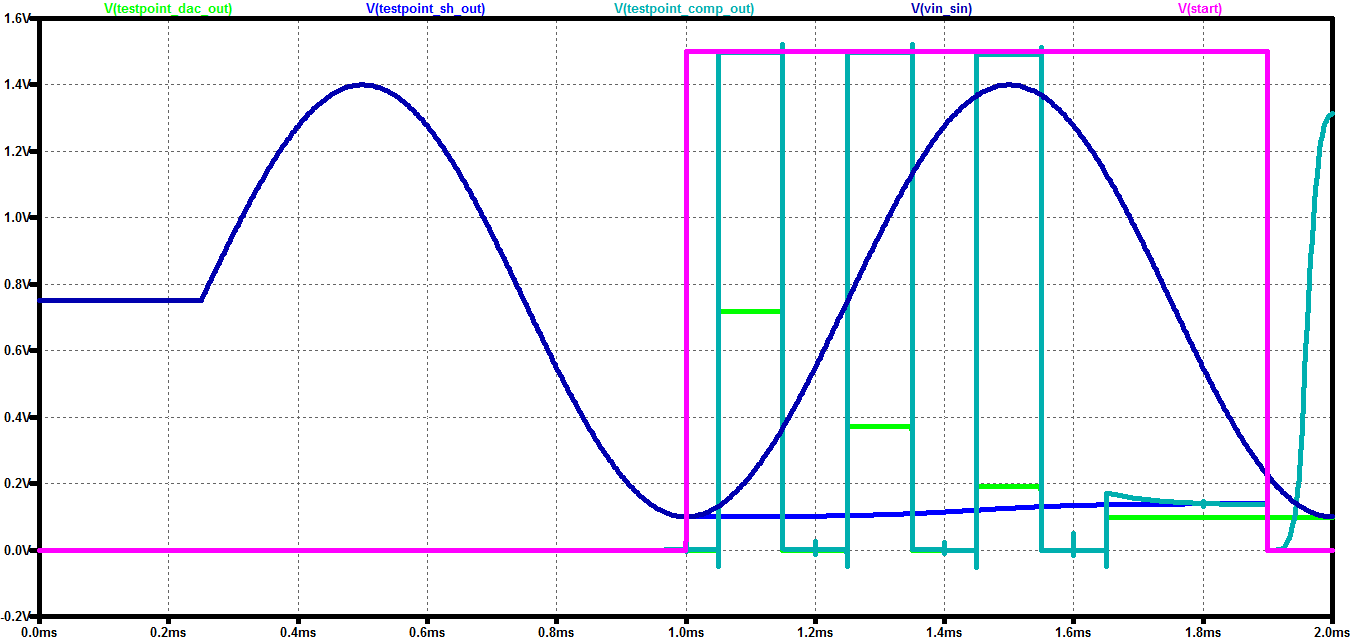


Figure 23: Analog Input 100mV. DAC output: 0001.

Analog Input: 1.4 V. DAC output: 0001

|  |  |  |
| --- | --- | --- |
| Select-Cycle | DAC output (mV) | Decided bit |
| 3 | 719 | Comparator is high. Q3 = 0 |
| 2 | 370.8 | Comparator is high. Q2 = 0 |
| 1 | 190.9 | Comparator is high. Q1= 0 |
| 0 | 97.69 | Comparator is not high. Q0 = 1. |

Because of the droop in the sample and hold circuit, the DAC output appears to be lower. 0000 is the missing code. This can be eliminated by running the clock at a higher frequency. This is depicted in the figure below.

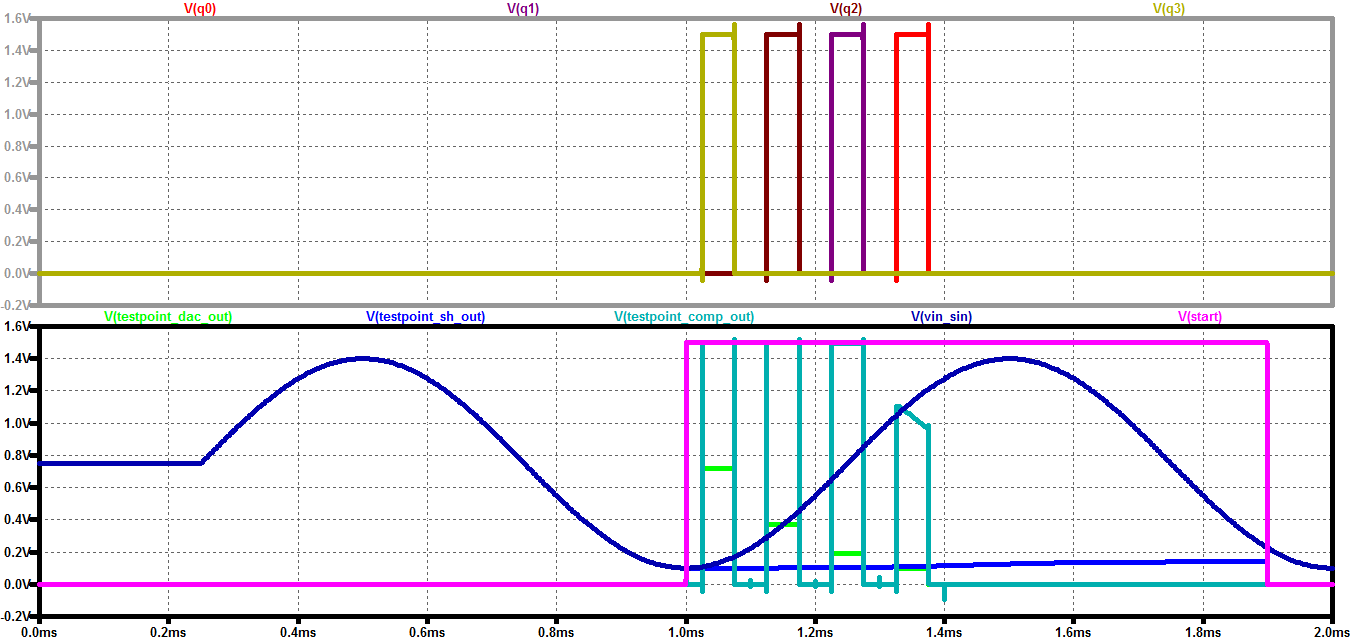


Figure 24: Running the clock at 20kHz, the droop gets reduced.

**[SAR ADC Conversion Characteristics]**

1. **Measurement Details**

**Description:**

A linear ramp is applied at the analog\_input of the SAR ADC. The start signal of the ADC is varied and applied at different time instants. The digital code obtained from the SAR algorithm is fed through another instance of R-2R DAC. The resulting output is plotted against the input signal to obtain static metrics of the SAR.

Figure 25 shows the use of “.param” SPICE directive to sweep the analog\_input applied. By using the “.meas” we can measure the output of the DAC for the swept sample values. The digital Output (represented in voltage) is plotted against analog input voltage, as shown in Figure 26. As we can see from the static plot the missing code is 0001.

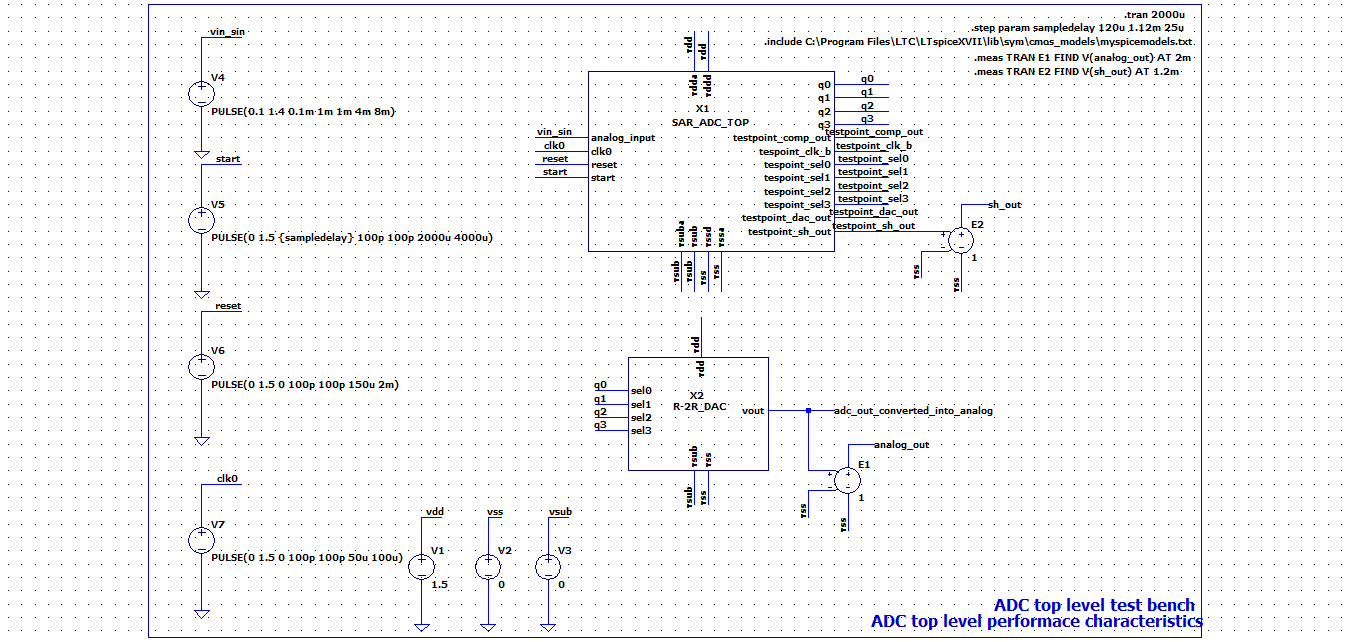


Figure 25: Static ADC characteristics.

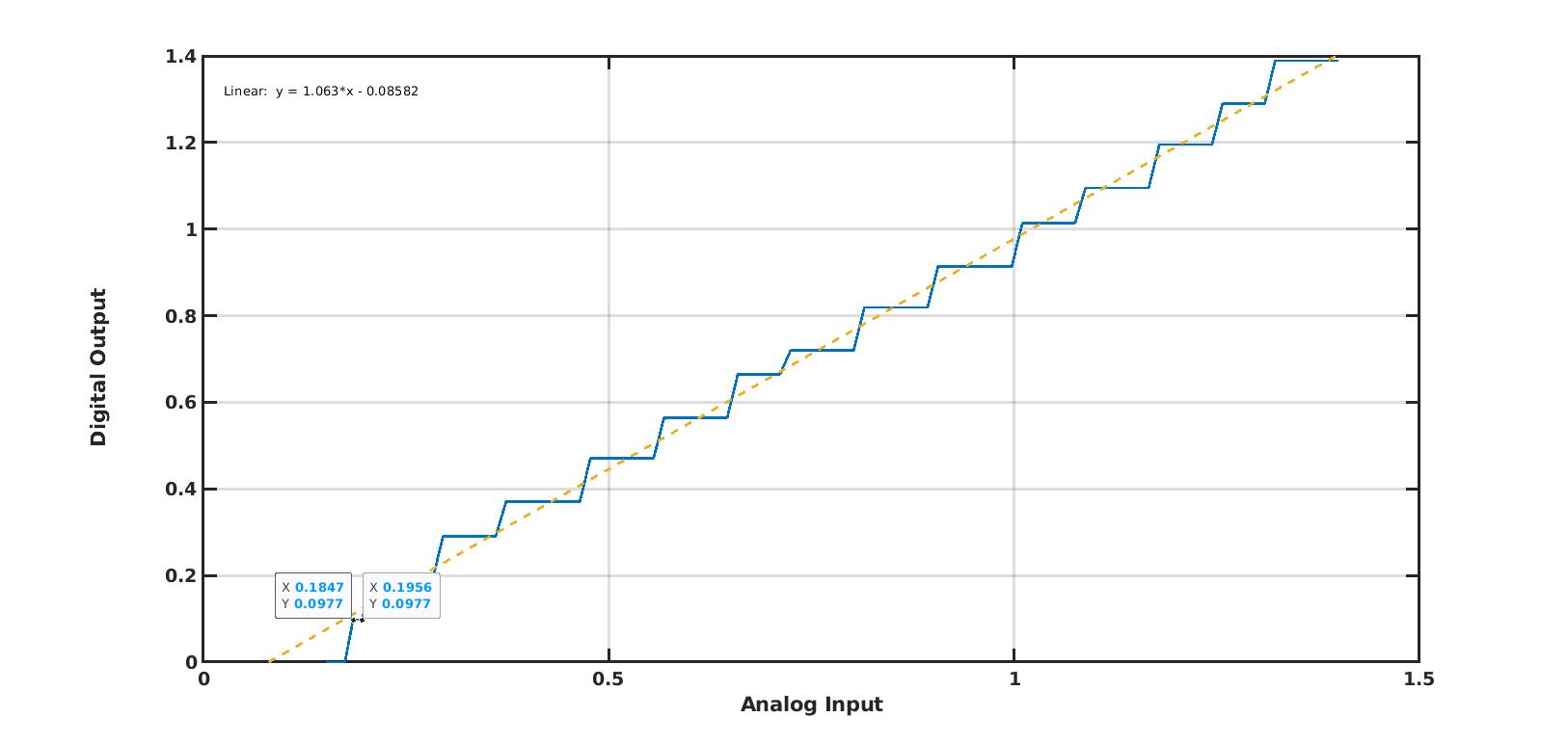


Figure 26: Static ADC performance characteristics.

**2. Static ADC Metrics**

**Description:**

|  |  |
| --- | --- |
| **Parameter** | **Measured Value** |
| 1 LSB | 97.7 mV |
| DNL | -0.88 LSBs |
| INL | 0.3 LSBs |
| Offset | -0.085 V |
| Anatop RMS current draw per conversion | 892.47µA |
| Digtop RMS current draw per conversion | 835.22µA |
| Theoretical SNR (6.02\*N +1.76 )db | 25.84 dB |

[**Layout Floorplan**]

Layout Floorplan:

|  |  |
| --- | --- |
| Name of the block | Size (um2) |
| Anatop | |
| R-2R DAC (8 inverters + 8 resistors) | 21.184 |
| Comparator (2) | 493.824 |
| CMOS Sample and hold | 648.648 |
| Digtop | |
| SAR logic + Clock generator | 200 |
| Total Area | 1363.656 |

**[Offset Calibration Techniques]**

As the comparator is built as a multi-stage amplifier, multi-stage offset correction technique, would be the most useful.

[**Conclusion and Future Work**]

SNR computation needs to capture other noise sources apart from the quantization noise. Offset calibration techniques need to realized and tested. The performance of the SAR needs to improve in terms of power consumed for the effective number of bits.