Device: NMOS transistor.

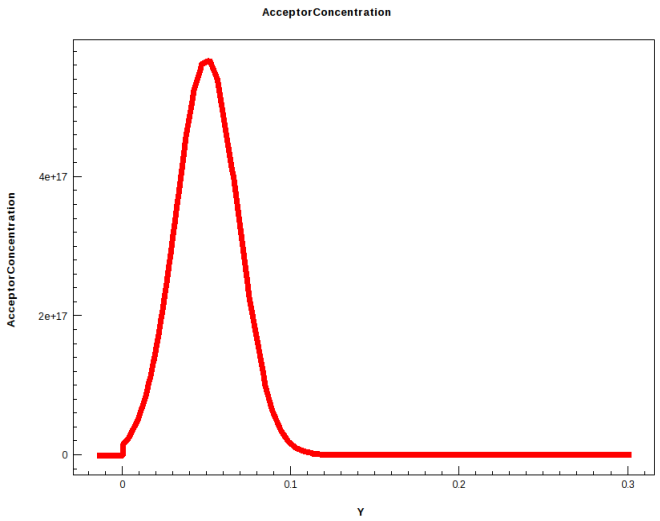
Oxide thickness: 8.4nm
Poly doping: 1e+20
Gate length: 120nm (Nominal)
Source/Drain Length: 100nm
Peak Body Doping: 0.6e+18
Source/Drain Peak Doping: 3e+20

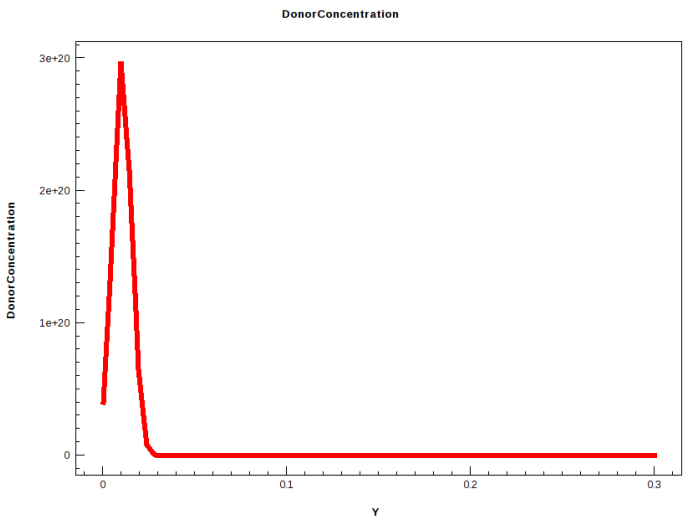
The doping profiles for the body, source and drain were chosen as below. Hand calculations were made to obtain the approximate body doping to get the required threshold voltage. At higher drain voltage, the threshold voltage is lower due to drain induced barrier lowering, as shown in Fig.3. The body doping was adjusted to meet the V_{thsat} specification.

Leakage current is found to increase exponentially with decrease in the gate oxide thickness. For this design, the leakage current is 14nA/um. However, this could be reduced by increasing the oxide thickness, as shown in Fig. 4. On the contrary, I_{ON} specification can be met easily at lower oxide thickness, as it increases the C_{ox}. Here, $I_{ON} = 400\mu A/\mu m$.

The threshold voltage was found to reduce, with reduction of gate length. This can be attributed to the source/drain charge sharing. In the depleted region near the source and the drain, no gate voltage is required to deplete the channel. The worst case for which can be seen at a gate length of 40nm, where $V_{TLin} < 0$. V_{thsat} is even lower due to DIBL, which is more pronounced in short channel devices. The transconductance g_m increases at lower lengths as it varies invresely with Length. This effect is compunded by the reduction in V_{th} of the device too. Subsurface punch through also, to certain extent increases the drain current at higher drain voltages.

A MOS CV curve demonstrates the traversal of the device from accumulation to depletion to inversion at gate ramp rate of 1V/s.





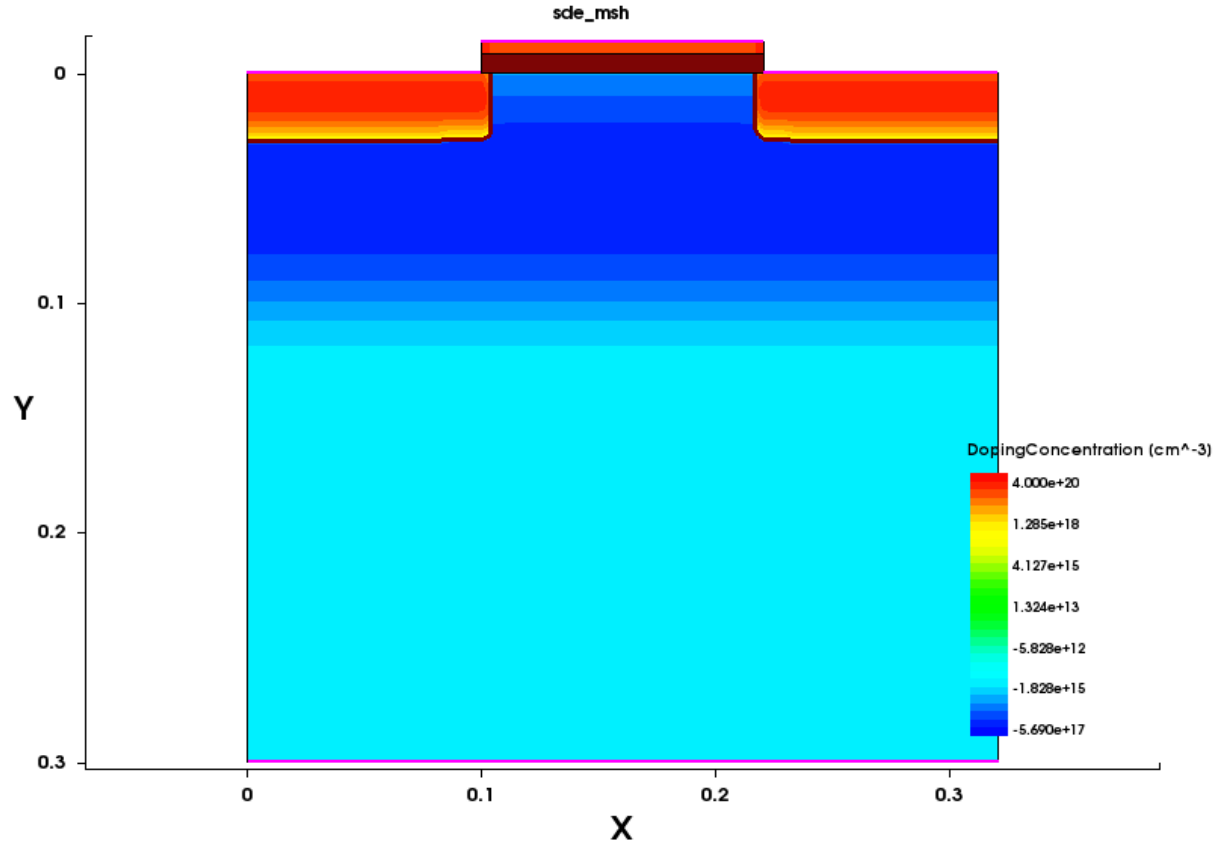


Figure 1: Device Structure

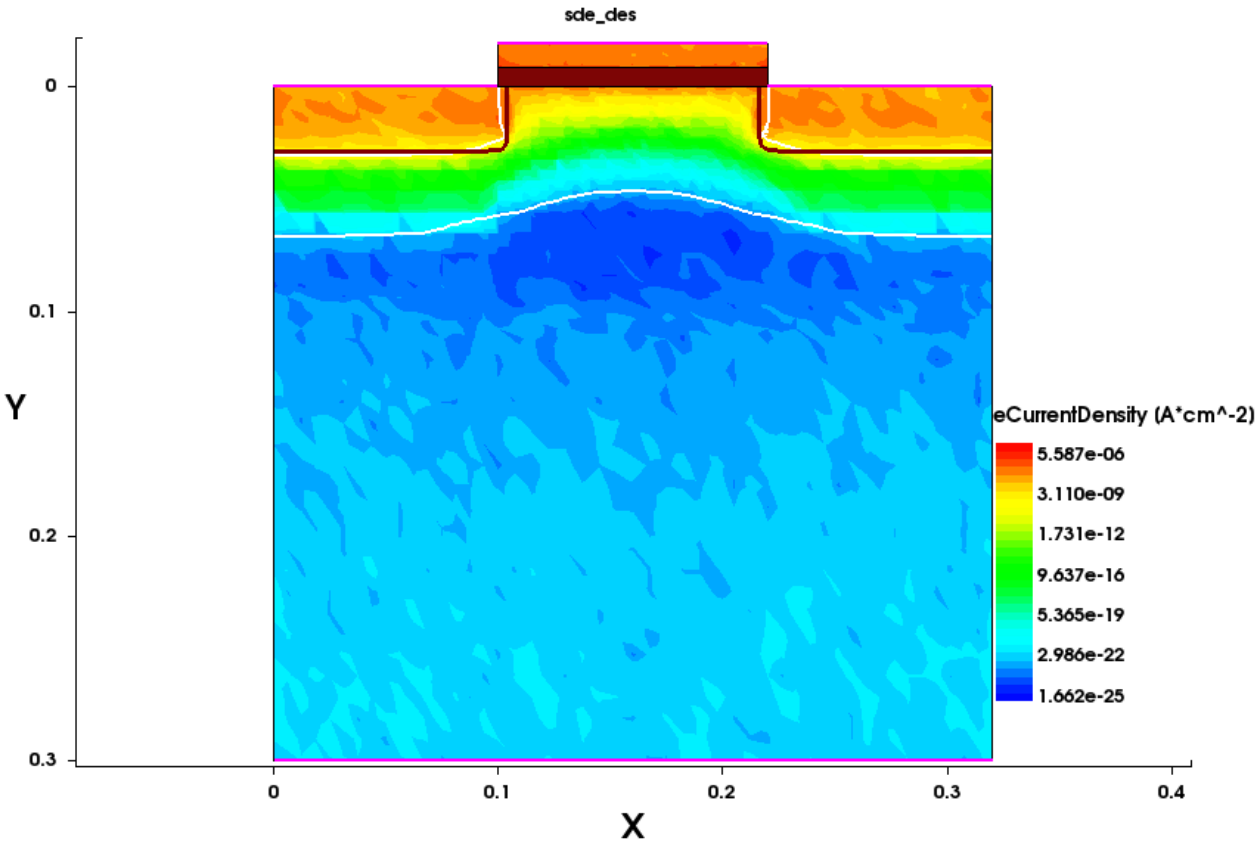


Figure 2: Electron density at inversion Vgs=Vds=1.5V

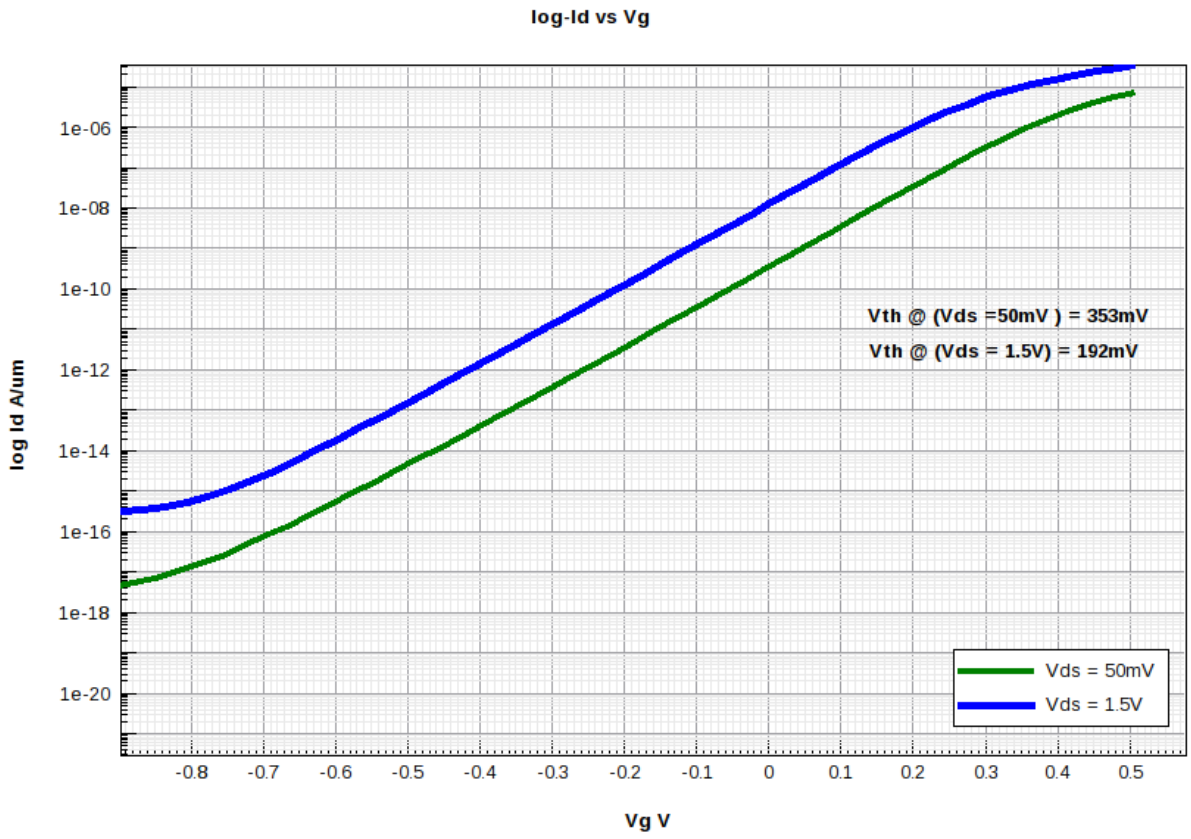
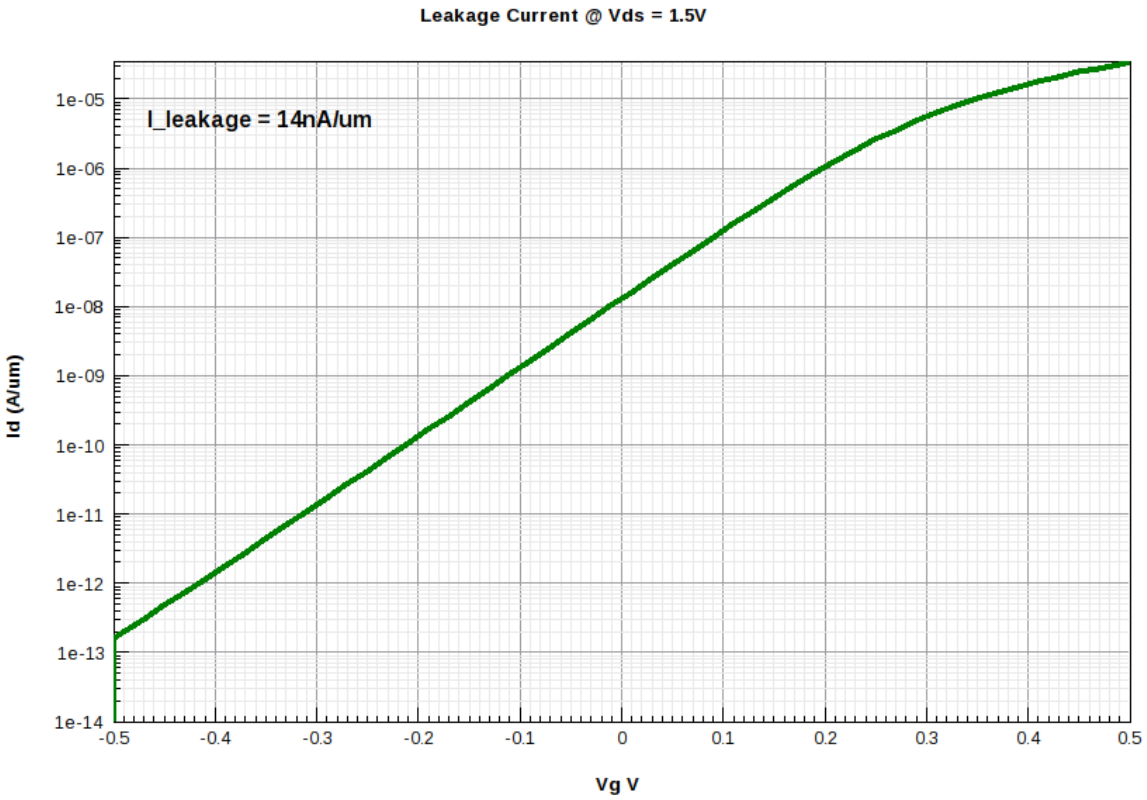
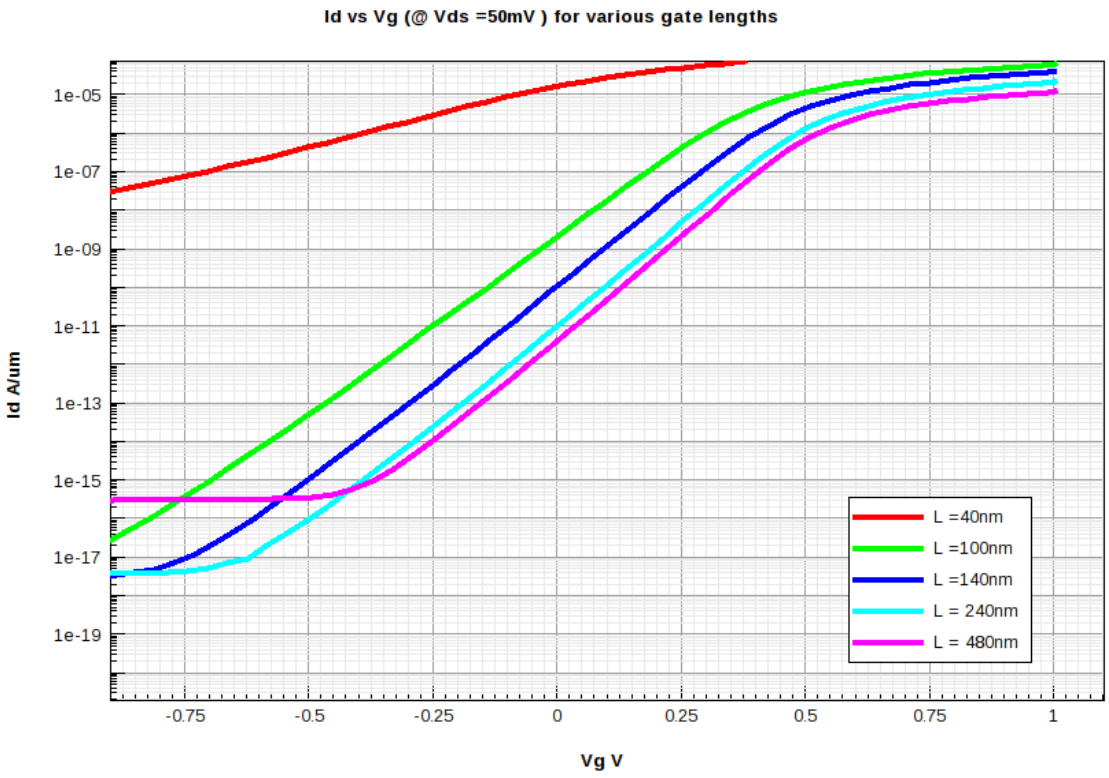
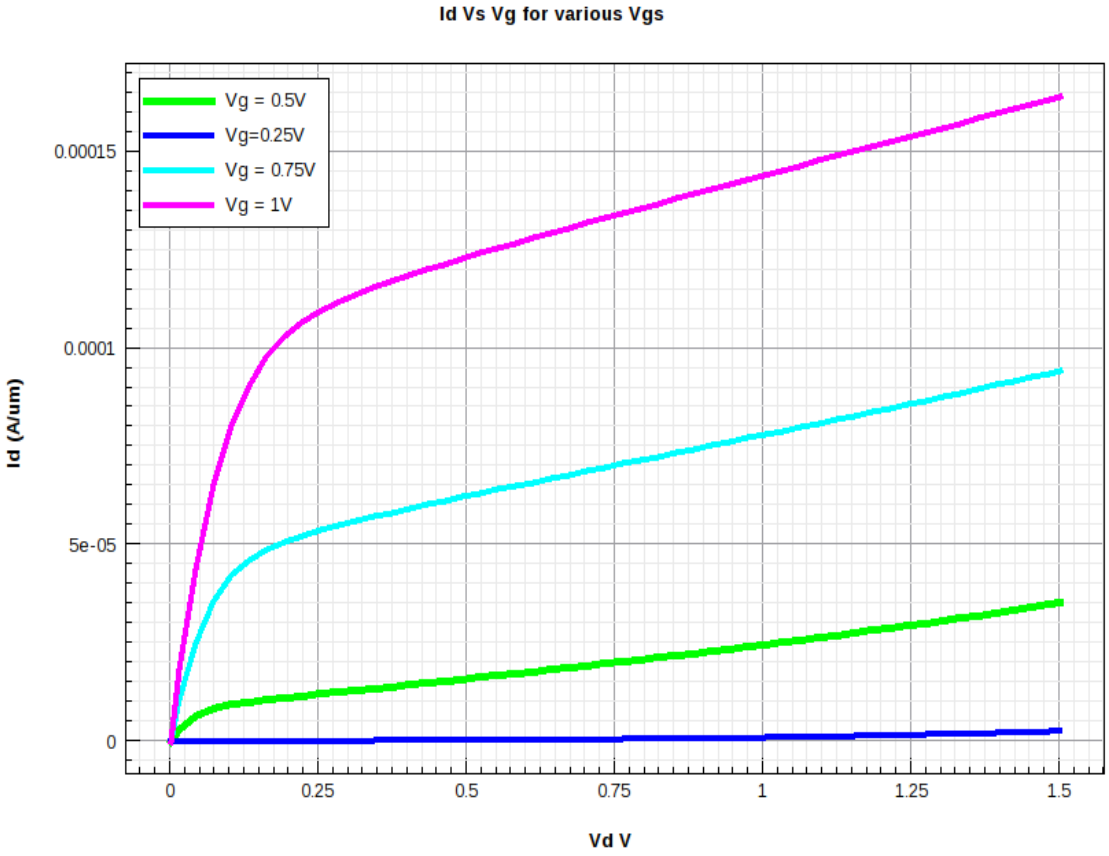
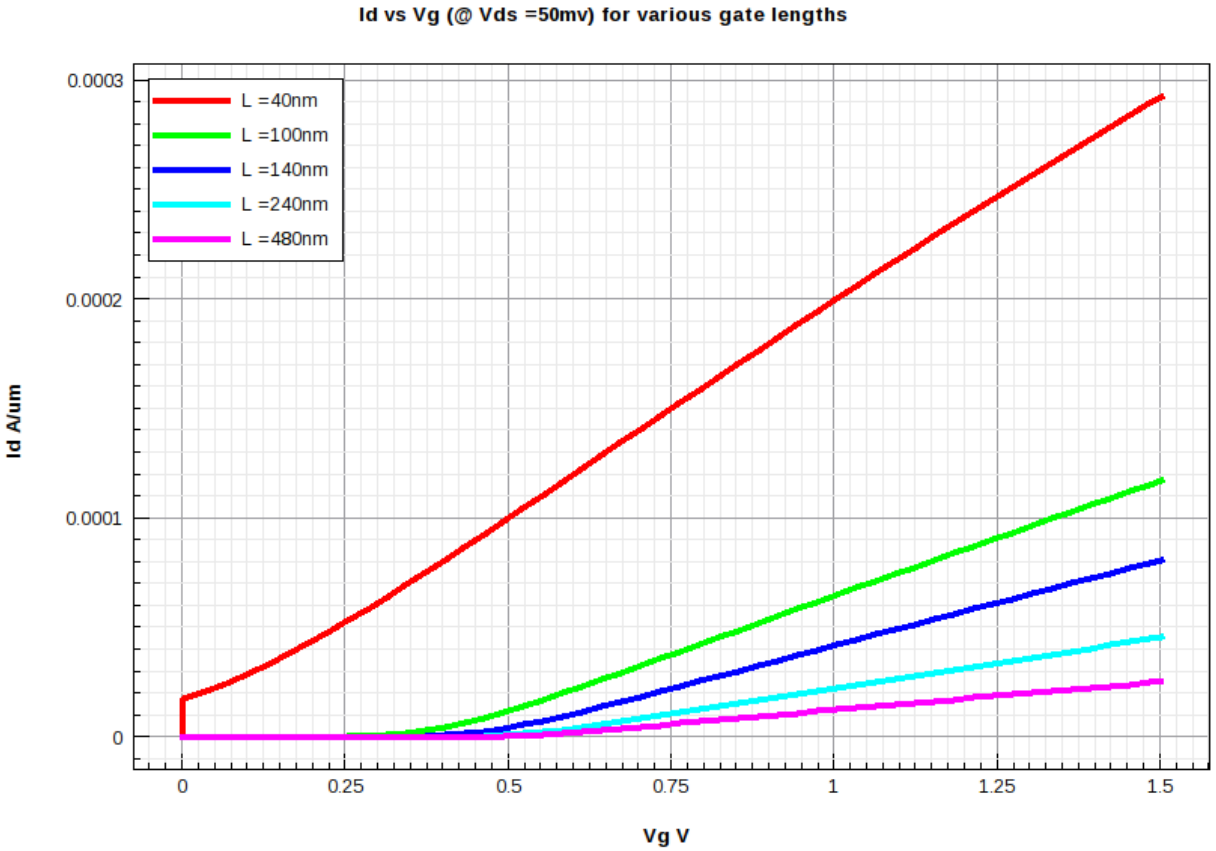


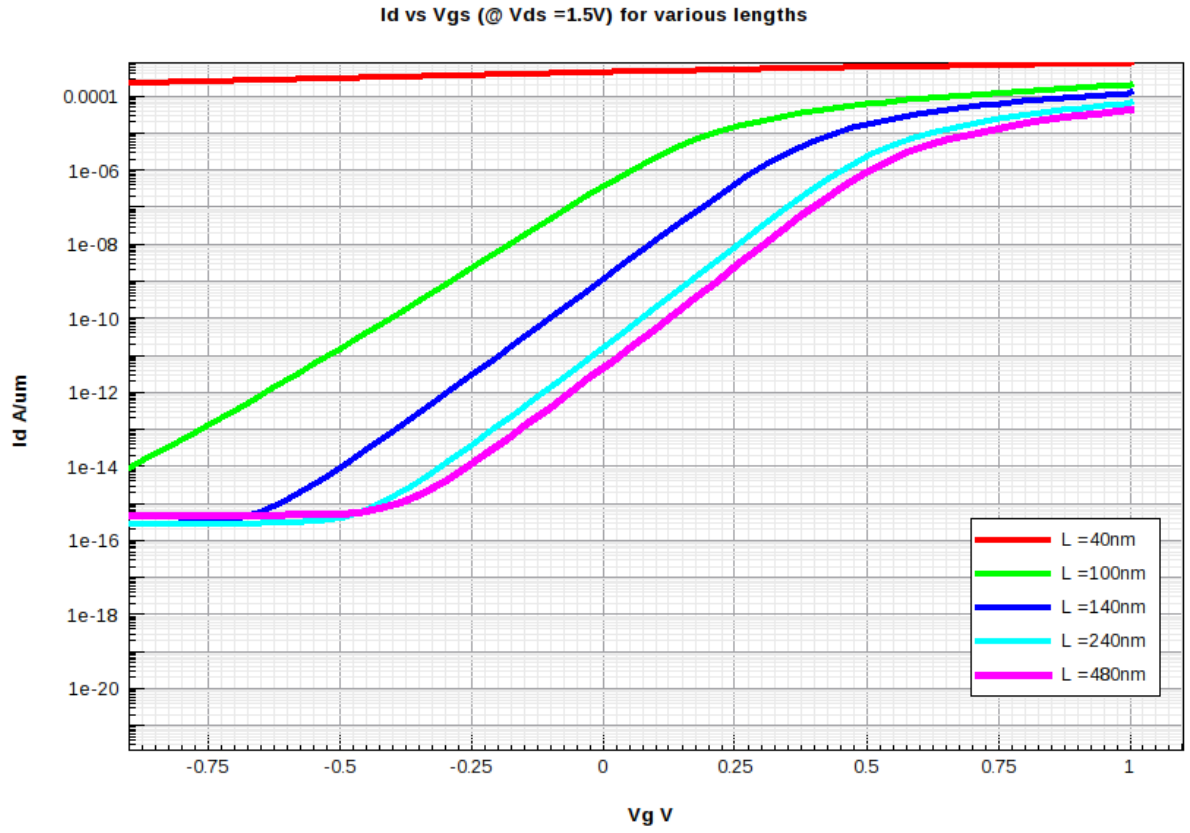
Figure 3: Threshold voltage at higher drain voltages is lower.

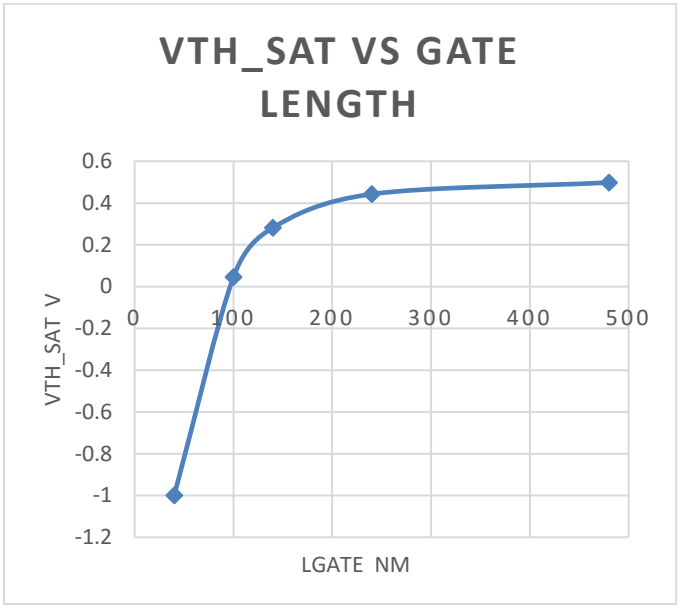


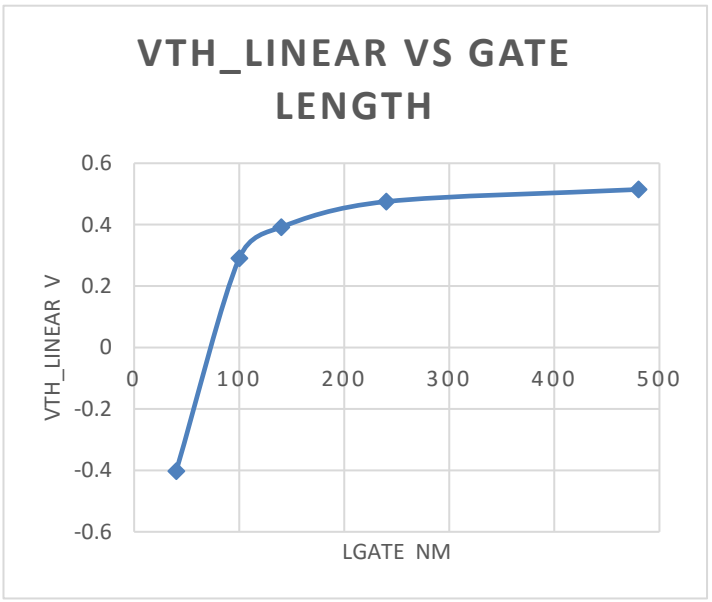

Id vs Vg (@ Vds =50mV) for various gate lengths
Id A/um
1e-05
1e-07
1e-09
1e-11
1e-13
1e-15
1e-17
1e-19
-0.75
-0.5
-0.25
0
0.25
0.5
0.75
1
Vg V
L =40nm
L =100nm
L =140nm
L = 240nm
L = 480nm

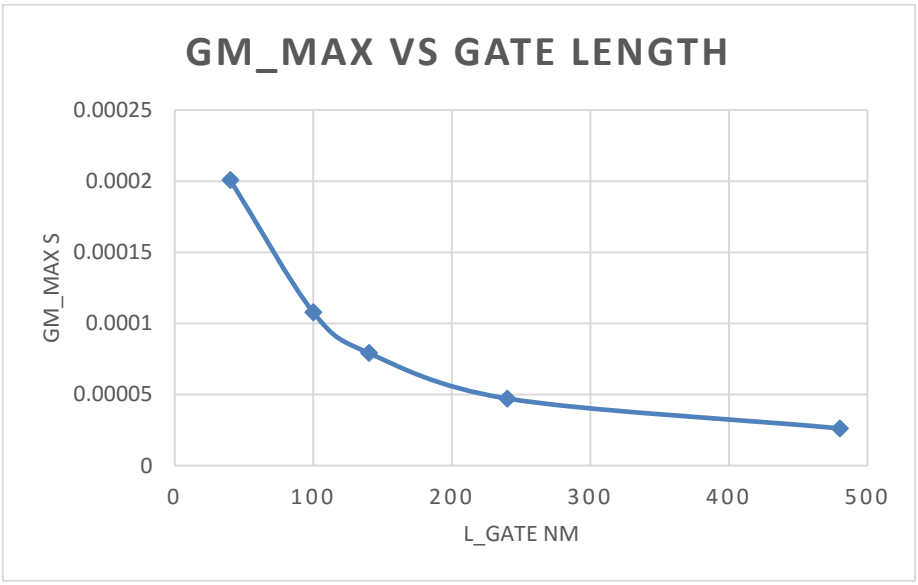

Id Vs Vg for various Vgs
Id (A/um)
0.00015
0.0001
5e-05
0
0
0.25
0.5
0.75
1
1.25
1.5
Vd V
Vg = 0.5V
Vg=0.25V
Vg = 0.75V
Vg = 1V


Id vs Vg (@ Vds =50mv) for various gate lengths
L =40nm
L =100nm
L =140nm
L =240nm
L =480nm
0.0003
0.0002
0.0001
0
Id A/um
0
0.25
0.5
0.75
1
1.25
1.5
Vg V


Id vs Vgs (@ Vds =1.5V) for various lengths
0.0001
1e-06
1e-08
1e-10
1e-12
1e-14
1e-16
1e-18
1e-20
Id A/um
-0.75
-0.5
-0.25
0
0.25
0.5
0.75
1
Vg V
L =40nm
L =100nm
L =140nm
L =240nm
L =480nm


VTH_SAT VS GATE LENGTH
VTH_SAT V
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
-1.2
0
100
200
300
400
500
LGATE NM


VTH_LINEAR VS GATE LENGTH
VTH_LINEAR V
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
0
100
200
300
400
500
LGATE NM


GM_MAX VS GATE LENGTH
GM_MAX S
0.00025
0.0002
0.00015
0.0001
0.00005
0
0
100
200
300
400
500
L_GATE NM

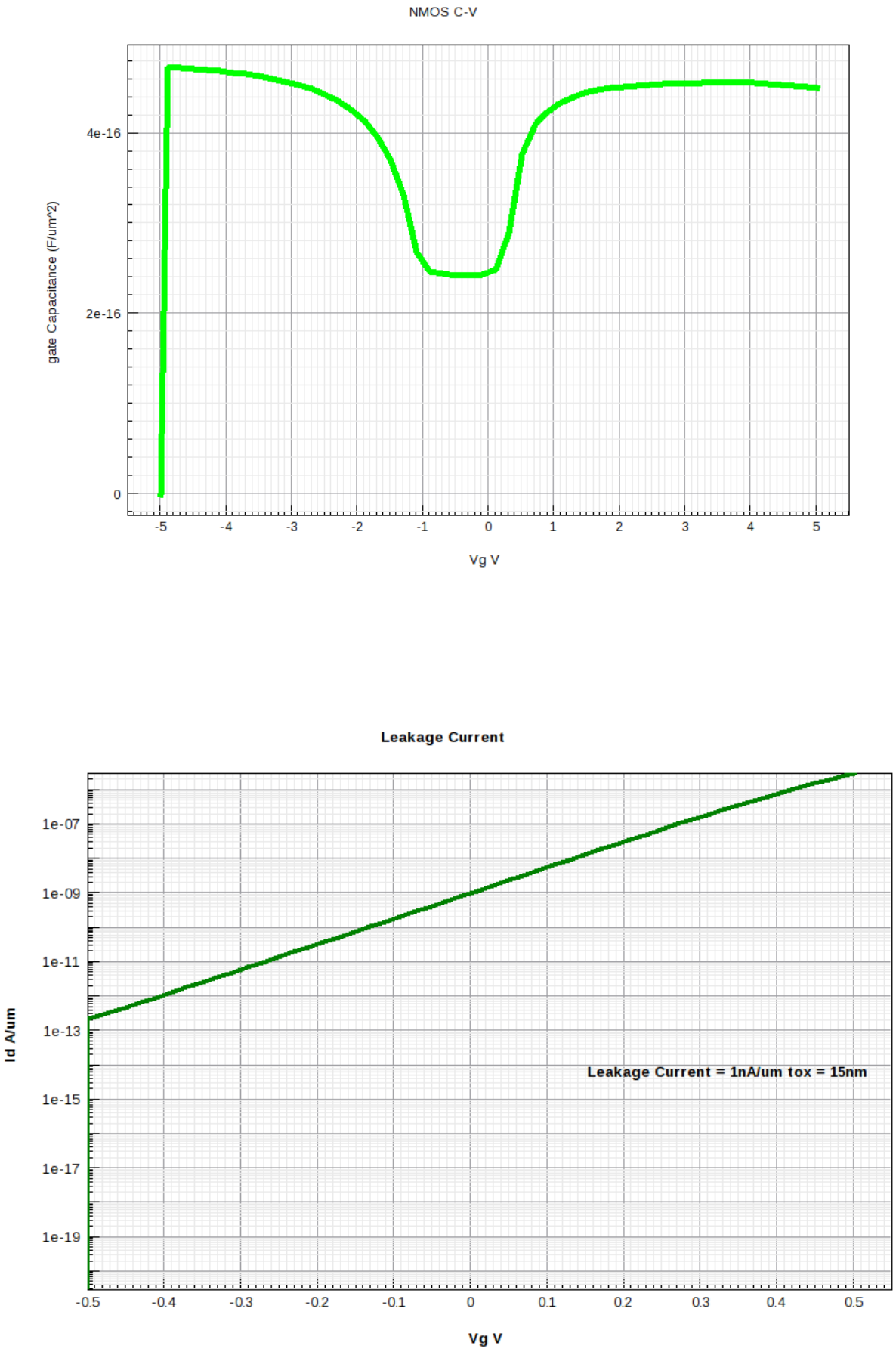


Figure 4: Reduction in leakage current, with increased gate oxide thickness.