

Fig. 4.15 A 3-Input HTL NAND Gate Driving N Similar Gates

The propagation delay time is adversely affected due to large resistance values. It is as high as hundreds of nano-seconds. The temperature sensitivity of the HTL gate is considerably less than that of DTL (Prob. 4.12).

4.8 TRANSISTOR-TRANSISTOR LOGIC (TTL)

The transistor-transistor logic (TTL) is the most successful bipolar logic which was evolved in the 1960s and has survived for more than four decades. TTL families use transistors, both to perform logic functions and to provide high output drive capability.

The NAND gate is the basic TTL logic circuit. Figure 4.16 shows a 3-input TTL NAND gate driving N similar gates. It uses a multiple-emitter transistor T_1 . The number of inputs (fan-in) to the gate is same as the number of emitters fabricated during its manufacturing.

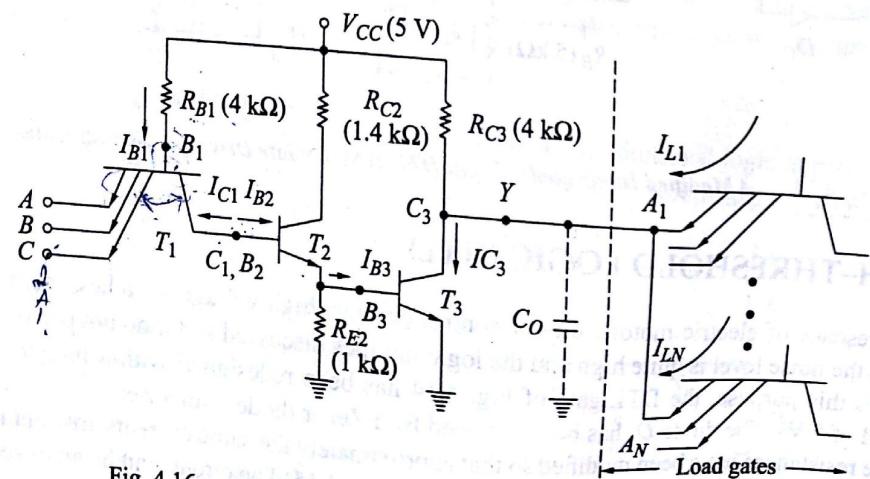


Fig. 4.16 A 3-Input TTL NAND Gate Driving N Similar Gates

4.8.1 Operation of TTL NAND Gate

Let us assume that the load gates are not present and the voltages for logic 0 and 1 are $V_{CE,sat} \approx 0.2$ V and $V_{CC} = 5$ V respectively.

The following voltages are assumed for $p-n$ junction (diode operation) and transistors.

$p-n$ junction: Voltage across a conducting diode = 0.7 V
Cut-in voltage $V_r = 0.6$ V

Transistor: Cut-in voltage $V_r = 0.5$ V
 $V_{BE,sat} = 0.8$ V
 $V_{CE,sat} = 0.2$ V

Condition I At least one input is LOW. The emitter-base junction of T_1 corresponding to the input in the LOW state is forward-biased making voltage at B_1 , $V_{B1} = 0.2 + 0.7 = 0.9$ V. For base-collector junction of T_1 to be forward-biased, and for T_2 and T_3 to be conducting, V_{B1} is required to be at least $0.6 + 0.5 + 0.5 = 1.6$ V. Hence, T_2 and T_3 are OFF.

Since T_3 is OFF, therefore $Y = V(1) = V_{CC}$.

Figure 4.17(a) illustrates the circuit corresponding to this condition.

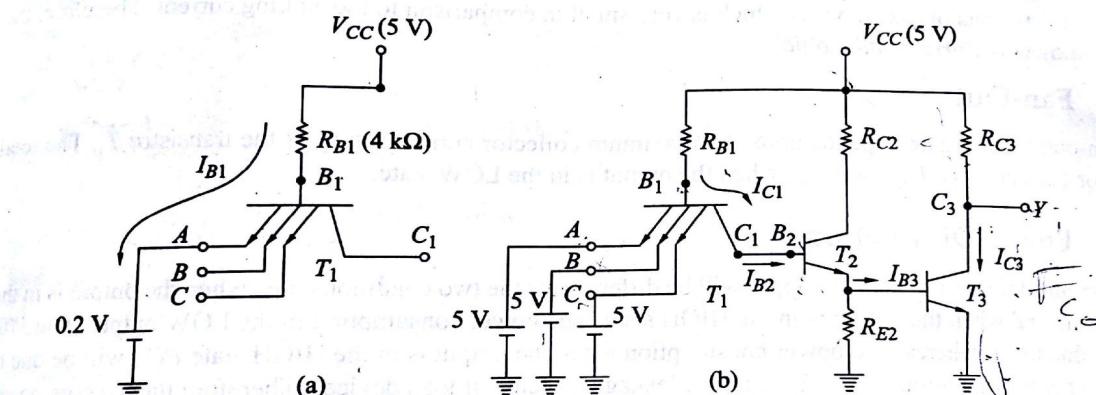


Fig. 4.17 Circuits Illustrating the Operation of TTL NAND Gate. (a) Atleast One of the Inputs is LOW
(b) All the Inputs are HIGH

Condition II All inputs are HIGH. The emitter-base junctions of T_1 are reverse-biased. If we assume that T_2 and T_3 are ON, then $V_{B2} = V_{C1} = 0.8 + 0.8 = 1.6$ V. Since B_1 is connected to V_{CC} (5 V) through R_{B1} , the collector-base junction of T_1 is forward-biased. The transistor T_1 is operating in the active inverse mode, making I_{C1} flow in the reverse direction. This current flows into the base of T_2 driving T_2 and T_3 into saturation. Therefore, $Y = V(0) \approx 0.2$ V.

Figure 4.17(b) Illustrates the circuit corresponding to this condition.

The above operation shows that the gate of Fig. 4.16 operates as a NAND gate. From conditions I and II, it appears that T_1 is acting as back-to-back diodes. The importance of T_1 will become clear from condition III.

Condition III Let the circuit be operating under condition II when one of the inputs suddenly goes to $V(0)$. The corresponding emitter-base junction of T_1 starts conducting and V_{B1} drops to 0.9 V. T_2 and T_3 will be turned off when the stored base charge is removed. Since $V_{C1} = V_{B2} = 1.6$ V, therefore the collector-base

4.2.1 Speed of Operation

The speed of a digital circuit is specified in terms of the propagation delay time. The input and output waveforms of a logic gate are shown in Fig. 4.1. The delay times are measured between the 50 per cent voltage levels of input and output waveforms.

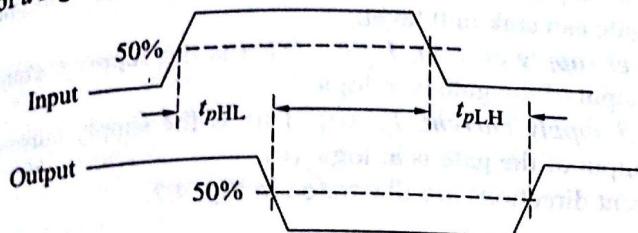


Fig. 4.1 Input and Output Voltage Waveforms to Define Propagation Delay Times

There are two delay times: t_{pHL} , when the output goes from the HIGH state to the LOW state and t_{pLH} , corresponding to the output making a transition from the LOW state to the HIGH state. The propagation delay time of the logic gate is taken as the average of these two delay times.

4.2.2 Power Dissipation

This is the amount of power dissipated in an IC. It is determined by the current, I_{CC} , that it draws from the V_{CC} supply, and is given by $V_{CC} \times I_{CC}$. I_{CC} is the average value of $I_{CC}(0)$ and $I_{CC}(1)$. This power is specified in milliwatts. It is known as static power dissipation, i.e., the power consumed by the circuit when input signals are not changing.

4.2.3 Figure of Merit

The figure of merit of a digital IC is defined as the product of speed and power. The speed is specified in terms of propagation delay time expressed in nanoseconds.

$$\text{Figure of merit} = \text{propagation delay time (ns)} \times \text{power (mW)}$$

It is specified in pico joules ($\text{ns} \times \text{mW} = \text{pJ}$)

A low value of speed-power product is desirable. In a digital circuit, if it is desired to have high speed, i.e. low propagation delay, then there is a corresponding increase in the power dissipation and vice-versa.

4.2.4 Fan-Out

This is the number of similar gates which can be driven by a gate. High fan-out is advantageous because it reduces the need for additional drivers to drive more gates.

4.2.5 Current and Voltage Parameters

The following currents and voltages are specified which are very useful in the design of digital systems.

High-level input voltage, V_{IH} : This is the minimum input voltage which is recognised by the gate as logic 1.

Low-level input voltage, V_{IL} : This is the maximum input voltage which is recognised by the gate as logic 0.

High-level output voltage, V_{OH} : This is the minimum voltage available at the output corresponding to logic 1.

Low-level output voltage, V_{OL} : This is the maximum voltage available at the output corresponding to logic 0.

High-level input current, I_{IH} : This is the minimum current which must be supplied by a driving source corresponding to 1 level voltage.

Low-level input current, I_{IL} : This is the minimum current which must be supplied by a driving source corresponding to 0 level voltage.

High-level output current, I_{OH} : This is the maximum current which the gate can sink in 1 level.

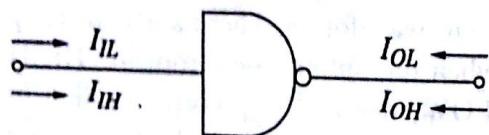


Fig. 4.2 A Gate With Current Directions Marked

Low-level output current, I_{OL} : This is the maximum current which the gate can sink in 0 level.

High-level supply current, $I_{CC}(1)$: This is the supply current when the output of the gate is at logic 1.

Low-level supply current, $I_{CC}(0)$: This is the supply current when the output of the gate is at logic 0.

The current directions are illustrated in Fig. 4.2.

4.2.6 Noise Immunity

The input and output voltage levels defined above are shown in Fig. 4.3. Stray electric and magnetic fields may induce unwanted voltages, known as *noise*, on the connecting wires between logic circuits. This may

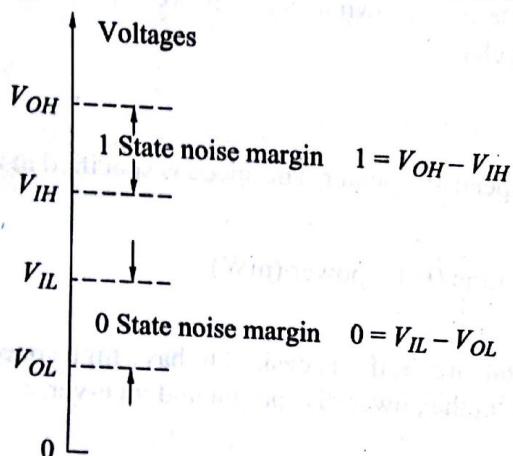


Fig. 4.3 Voltage Levels and Noise Margins of ICs

approaches the propagation delay time of the circuit and respond. Under this condition, a large pulse amplitude would be required to produce a change in the circuit very short duration. This is referred to as *ac noise margin* and is substantially greater than the dc noise pulse width.

cause the voltage at the input to a logic circuit to drop below V_{IH} or rise above V_{IL} and may produce undesired operation. The circuit's ability to tolerate noise signals is referred to as the *noise immunity*, a quantitative measure of which is called *noise margin*. Noise margins are illustrated in Fig. 4.3.

The noise margins defined above are referred to as *dc noise margins*. Strictly speaking, the noise is generally thought of as an a.c. signal with amplitude and pulse width. For high speed ICs, a pulse width of a few microseconds is extremely long in comparison to the propagation delay time of the circuit and therefore, may be treated as d.c. as far as the response of the logic circuit is concerned. As the noise pulse width decreases and the pulse duration is too short for the circuit to respond. Under this condition, a large pulse amplitude would be required to produce a change in the circuit very short duration. This is referred to as *ac noise margin* and is substantially greater than the dc noise pulse width.

4.2.7 Operating Temperature

The temperature range in which an IC functions properly must be known. The accepted temperature ranges are: 0 to +70 °C for consumer and industrial applications and -55 °C to +125 °C for military purposes.

4.2.8 Power Supply Requirements

The supply voltage(s) and the amount of power required by an IC are important characteristics required to choose the proper power supply.

4.2.9 Flexibilities Available

Various flexibilities are available in different IC logic families and these must be considered while selecting a logic family for a particular job. Some of the flexibilities available are:

1. *The breadth of the series:* Type of different logic functions available in the series.
2. *Popularity of the series:* The cost of manufacturing depends upon the number of ICs manufactured. When a large number of ICs of one type are manufactured, the cost per function will be very small and it will be easily available because of multiple sources.
3. *Wired-logic capability:* The outputs can be connected together to perform additional logic without any extra hardware.
4. *Availability of complement outputs:* This eliminates the need for additional inverters.
5. *Type of output:* Passive pull-up, active pull-up, open-collector/drain, and tristate. These will be explained in subsequent sections.

4.3 RESISTOR-TRANSISTOR LOGIC (RTL)

The resistor-transistor logic was the most popular form of logic in common use before the development of ICs. RTL circuits consist of resistors and transistors and was the earliest logic family to be integrated. Although RTL has become obsolete now, because of its simplicity and for historical reasons, it is proper to devote some attention to it and introduce some of the important concepts, useful for all types of gates, through this. The basic RTL gate is a NOR gate as shown in Fig. 4.4. For the sake of simplicity, a two-input NOR gate driving N similar gates is shown in the figure, which can be extended to accommodate a larger number of inputs. The number of input terminals is referred to as the *fan-in*.

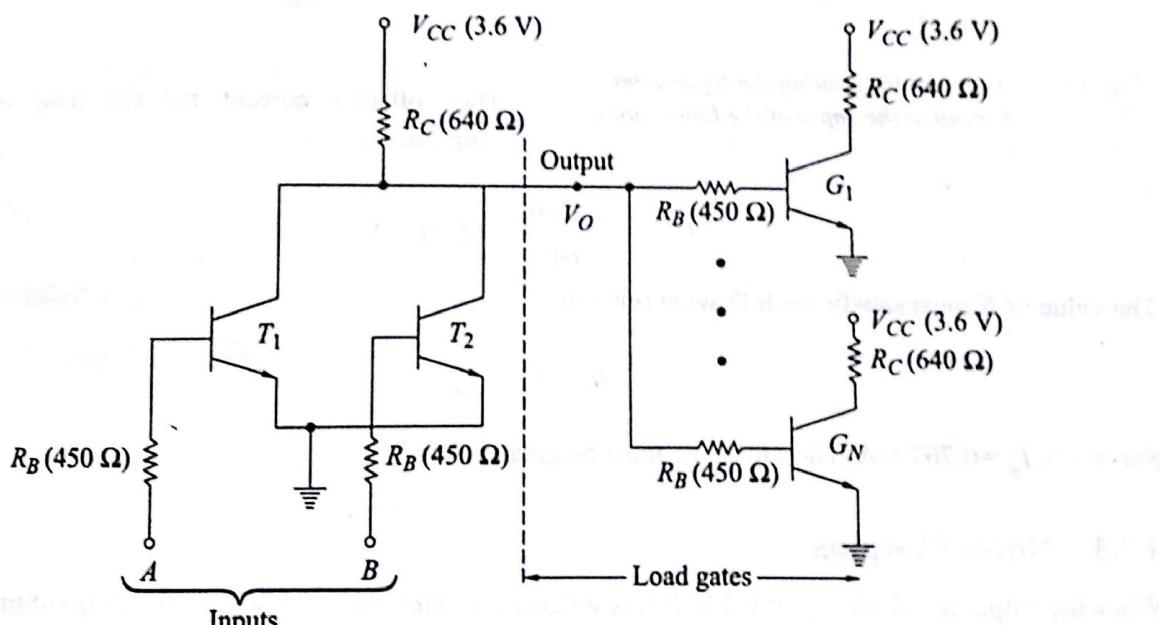


Fig. 4.4 A 2-input RTL NOR Gate Driving N Similar Gates

4.3.1 Logic Operation

Inputs representing the logic levels are applied at A and B terminals. The voltage corresponding to LOW level should be low enough to drive the corresponding transistor to cut-off. Similarly, the input voltage corresponding to HIGH level should be high enough to drive the corresponding transistor to saturation. If both the inputs are LOW, transistors T_1 and T_2 are cut-off and the output is HIGH. A HIGH level on any input will drive the corresponding transistor to saturation causing the output to go LOW. The LOW (0) level output voltage is $V_{CE,sat}$ of a transistor (~ 0.2 V) and the HIGH (1) level output voltage depends on the number of gates connected to the output. This causes the output voltage to be variable and is a deciding factor for the fan-out of the gate.

4.3.2 Loading Considerations

If all the inputs to the gate are LOW, the output is HIGH and if the gate is not driving any other gate, i.e. no load is connected, the output voltage will be slightly less than V_{CC} (there is voltage drop across the common collector resistor due to I_{CO} of T_1 and T_2).

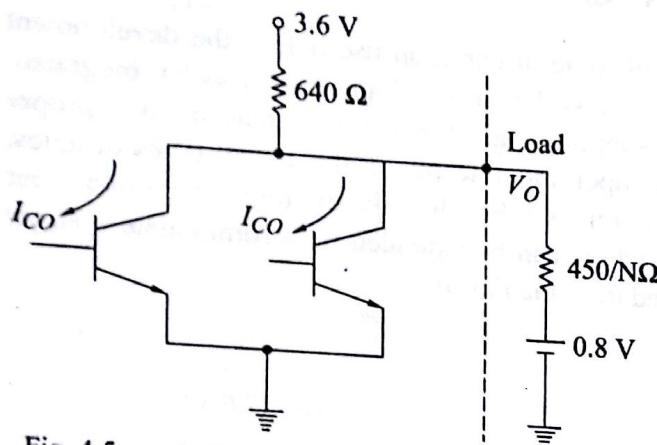


Fig. 4.5 A Circuit Illustrating the Equivalent Circuit at the Input of the Load Gates

When N similar gates are being driven, the load will be equivalent to a resistor of value $450/N$ ohms in series with a voltage source of 0.8 V (being the voltage between base and emitter of a transistor in saturation). The relevant portion of the circuit is shown in Fig. 4.5.

The base current for each load transistor is

$$I_B = \left(\frac{3.6 - 0.8}{640 + \frac{450}{N}} \right) \cdot \frac{1}{N} = \frac{2.8}{640N + 450} \quad (4.1)$$

The collector current for the load transistor in saturation is

$$I_{C,sat} = \frac{3.6 - 0.2}{640} = 5.31 \text{ mA} \quad (4.2)$$

The value of N must satisfy the following relation,

$$h_{FE} \cdot I_B \geq I_{C,sat} \quad (4.3)$$

For $N = 5$, $I_B = 0.767$ mA. Therefore, h_{FE} must be greater than 7.

4.3.3 Noise Margins

When the output is in 0 state $V_o = 0.2$ V. If this voltage becomes about 0.5 V (cut-in voltage of transistor), the load transistor comes to conduction which causes malfunction of the circuit. Hence, the logic 0 noise margin $\Delta V_o \approx 0.3$ V.

The logic 1 noise margin depends upon the number of gates being driven. For $N = 5$,

$$V_o = \frac{90}{90+640} \times (3.6) + \frac{640}{90+640} \times (0.8) = 1.14 \text{ V} \quad (4.4)$$

for $h_{FE} = 10$, the total base current required for load transistors to be driven into saturation will be $5 \times \left[\frac{9.31}{10} \right] \text{ mA}$ and the corresponding V_o must be 1.04 V. Therefore, the noise margin for 1 level is $\Delta V = 1.14 - 1.04 = 0.1 \text{ V}$.

4.3.4 Propagation Delay Time

The propagation delay time is also affected by the number of gates it drives. When the output of the gate is in LOW state all the load transistors are cut-off and the base-emitter junction of each of these transistors appears to be a capacitor, C . When the output has to change from LOW to HIGH level due to changes at the input, it will do so with a time constant given by

$$\left(640 + \frac{450}{N} \right) NC = (640N + 450) C \quad (4.5)$$

The resistance in the collector circuit pulls up the output voltage from LOW to HIGH level and hence is known as the *pull-up resistor*. It is passive pull-up in this case in contrast to an *active pull-up* which can be used to decrease the propagation delay time. Active pull-up will be discussed later.

4.3.5 Current Source Logic

The gate supplies current to the load transistors when in 1 level, whereas the leakage-current (reverse-saturation base current) of load transistors flow through T_1 or T_2 in 0 level. Since the source current is much greater than the sink current, it is known as *current source logic*.

4.3.6 Wired-Logic

If the outputs of the gates are connected together as shown in Fig. 4.6, the output Y is given by

$$\begin{aligned} Y &= Y_1 \cdot Y_2 \\ &= \overline{A+B} \cdot \overline{C+D} \\ &= \overline{A+B+C+D} \end{aligned}$$

Connection which is referred to as *wired-AND* or *implied-AND*. Operation can be seen in Prob. 4.3.

and it is in the range of 0.1 to 0.7 pJ. The silicon area required is very small and packing density in the range 120 to 200 gates per square millimetre have been realised.

4.6 DIODE-TRANSISTOR LOGIC (DTL)

The diode-transistor logic is somewhat more complex than RTL but because of its greater fan-out and improved noise margins it has replaced RTL. Its main disadvantage is slower speed and because of this it was modified and emerged as transistor-transistor logic (TTL) which is the most popular logic family today, as far as small- and medium-scale ICs are concerned. Although TTL has completely replaced DTL, for historical reasons as well as for better appreciation of TTL circuit, it is worthwhile discussing the details of DTL.

DTL circuit using discrete components was made using input diodes and a transistor inverter (NOT), which was modified for integrated circuit implementation as shown in Fig. 4.12.

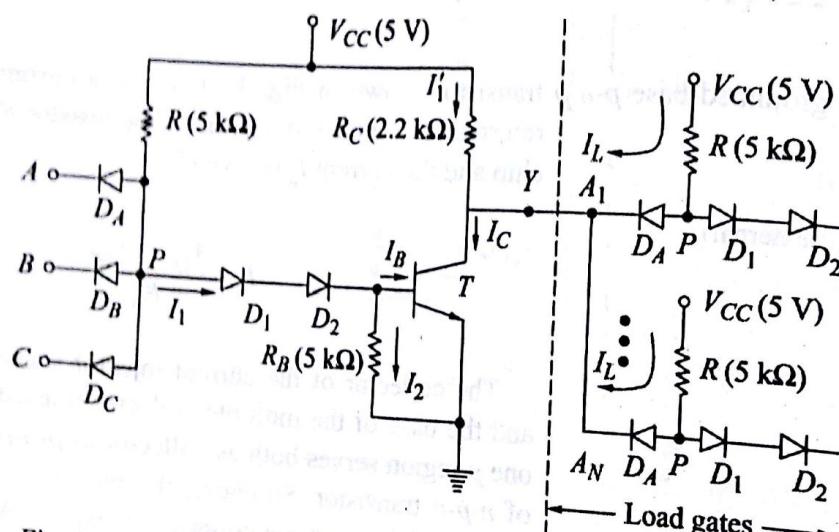


Fig. 4.12 A 3-Input DTL NAND Gate Driving N Similar Gates

4.6.1 Operation of DTL NAND Gate

The basic DTL gate is a NAND gate. A 3-input NAND gate driving N similar gates is shown in Fig. 4.12. The input diodes D_A , D_B , and D_C conduct through the resistor R , if the corresponding input is in the LOW state, while corresponding to HIGH state the diode is nonconducting. Therefore, if at least one of the inputs is LOW, the diode connected to this input conducts and the voltage V_p at point P is one diode drop above the low level voltage at the input. The voltage V_p should be such as to keep T in cut-off. Therefore, the output of T is V_{CC} . On the other hand, if all the three inputs are in HIGH state, the input diodes are cut-off and consequently current flowing from V_{CC} through R should be sufficient to drive T in saturation. Therefore, the output of T is $V_{CE,sat}$.

If we consider the voltages corresponding to logic 1 and 0 as V_{CC} and $V_{CE,sat}$ respectively, this circuit performs NAND operation. The following example illustrates the loading (fan-out) considerations and the noise-margins.

Example 4.1

For the DTL NAND gate of Fig. 4.12 calculate (a) fan-out (b) noise-margins, and (c) average power, P , dissipated by the gate. The diode and transistor parameters are:

Diode: Voltage across a conducting diode = 0.7 V

Cut-in voltage $V_p = 0.6$ V

Cut-in voltage $V_j = 0.5$ V

Transistor: $V_{BE,sat} = 0.8$ V

$V_{CE,sat} = 0.2$ V

$h_{FE} = 30$

Solution

(a) As discussed above, the logic levels are:

$$\text{LOW level} = V(0) = V_{CE,sat} = 0.2 \text{ V}$$

$$\text{HIGH level} = V(1) = V_{CC} = 5 \text{ V}$$

(i) If all the inputs are HIGH, the input diodes are reverse-biased. Assuming diodes D_1, D_2 to be conducting and T to be in saturation, the voltage $V_p = 0.7 + 0.7 + 0.8 = 2.2$ V.

Writing Kirchhoff's current law (KCL) equation at the base of T ,

$$I_B = I_1 - I_2$$

where

$$I_1 = \frac{V_{CC} - V_p}{R} = \frac{5 - 2.2}{5} = 0.56 \text{ mA}$$

and

$$I_2 = \frac{V_{BE,sat}}{R_B} = \frac{0.8}{5} = 0.16 \text{ mA}$$

which gives a base current $I_B = 0.4$ mA. The collector current (without load gates connected) is

$$I_C = \frac{V_{CC} - V_{CE,sat}}{R_C} = \frac{5 - 0.2}{2.2} = 2.182 \text{ mA}$$

Since $h_{FE} \times I_B = 30 \times 0.4 = 12$ mA is greater than I_C (2.182 mA), it is confirmed that the transistor is in saturation and the output is in LOW state. Now, if N load gates are fed from this gate, the input diodes of the driven gates will conduct through the output transistor T , i.e. T acts as a sink for the current in the input to the gates it drives. Assuming that all the other inputs to each of the load gates are HIGH except the one driven by

T , the current $I_L = \frac{V_{CC} - V_p}{R} = \frac{5 - 0.9}{5} = 0.82$ mA. This current is referred to as *standard load*. The fan-out is given by $I_C \leq h_{FE} I_L$, or $0.82 N + 2.182 \leq 12$ mA or $N < 12$ since N must be an integer. A conservative choice is $N = 10$. The Maximum collector current rating of T must be about 12 mA.

(ii) If at least one of the inputs is LOW, the corresponding input diode conducts and $V_p = 0.2 + 0.7 = 0.9$ V. The minimum voltage required for D_1, D_2 , and T to be conducting is $0.6 + 0.6 + 0.5 = 1.7$ V, which confirms that D_1, D_2 are nonconducting and hence T is cut-off. Consequently, the output voltage is V_{CC} (5 V) if the load gates are not connected.

If the load gates are connected, the input diodes of the load gates are nonconducting, which means the reverse-saturation current of these diodes must be supplied through the collector resistor R_C , which will

4.8.1 Operation of TTL NAND GATE

Let us assume that the load gates are not present and the voltages for logic 0 and 1 are $V_{CE,sat} \approx 0.2$ V and $V_{CC} = 5$ V respectively.

The following voltages are assumed for *p-n* junction (diode operation) and transistors.

- p-n* junction: Voltage across a conducting diode = 0.7 V
 Cut-in voltage $V_f = 0.6$ V
- Transistor: Cut-in voltage $V_r = 0.5$ V
 $V_{BE,sat} = 0.8$ V
 $V_{CE,sat} = 0.2$ V

Condition I At least one input is LOW. The emitter-base junction of T_1 corresponding to the input junction of T_1 to be forward-biased, and for T_2 and T_3 to be conducting, V_{B1} is required to be at least $0.6 + 0.5 + 0.5 = 1.6$ V. Hence, T_2 and T_3 are OFF.

Since T_3 is OFF, therefore $Y = V(1) = V_{CC}$

Figure 4.17(a) illustrates the circuit corresponding to this condition.

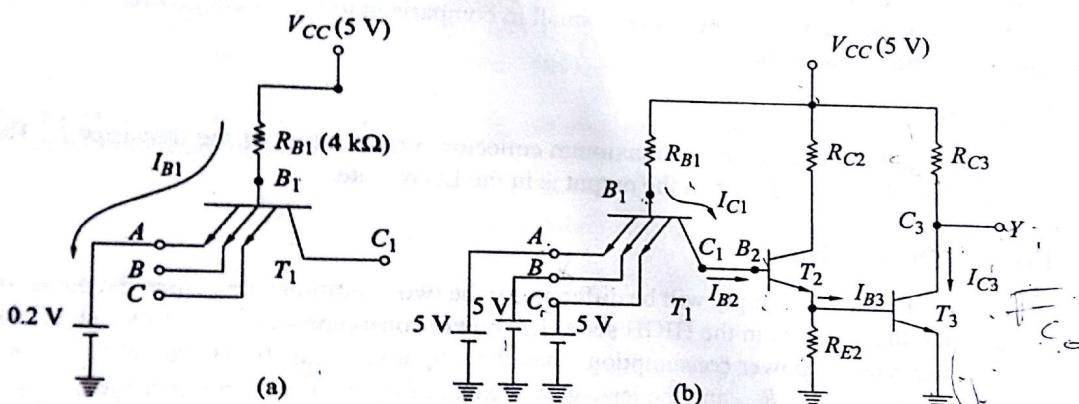


Fig. 4.17 Circuits Illustrating the Operation of TTL NAND Gate. (a) Atleast One of the Inputs is LOW
 (b) All the Inputs are HIGH

Condition II All inputs are HIGH. The emitter-base junctions of T_1 are reverse-biased. If we assume that T_2 and T_3 are ON, then $V_{B2} = V_{C1} = 0.8 + 0.8 = 1.6$ V. Since B_1 is connected to V_{CC} (5 V) through R_{B1} , the collector-base junction of T_1 is forward-biased. The transistor T_1 is operating in the active inverse mode, making I_{C1} flow in the reverse direction. This current flows into the base of T_2 driving T_2 and T_3 into saturation. Therefore, $Y = V(0) \approx 0.2$ V.

Figure 4.17(b) Illustrates the circuit corresponding to this condition.

The above operation shows that the gate of Fig. 4.16 operates as a NAND gate. From conditions I and II, it appears that T_1 is acting as back-to-back diodes. The importance of T_1 will become clear from condition III.

Condition III Let the circuit be operating under condition II when one of the inputs suddenly goes to $V(0)$. The corresponding emitter-base junction of T_1 starts conducting and V_{B1} drops to 0.9 V. T_2 and T_3 will be turned off when the stored base charge is removed. Since $V_{C1} = V_{B2} = 1.6$ V, therefore the collector-base

junction of T_1 is back-biased, making T_1 operate in the normal active region. This large collector current of T_1 is in a direction which helps in the removal of stored base charge in T_2 and T_3 and improves the speed of circuit. The direction of the collector current is same as the current I_{C1} shown in Fig. 4.16. The output voltage is pulled-up by the time constant $\tau = R_{C3} \cdot C_o$. Resistance R_{C3} is known as *pull-up resistor*.

4.8.2 Current Sink Logic

When at least one of the inputs is LOW, current I_{S1} from V_{CC} source flows through the input signal.

$$I_{S1} = \frac{V_{CC} - V_{S1}}{R_{S1}} = \frac{5 - 0.9}{4} \text{ mA} = 1.025 \text{ mA}$$

When all the inputs are HIGH, the emitter-base junctions of T_1 are reverse-biased. Therefore, current drawn from the input source is the reverse saturation current of a *p-n* junction which is very small (a few μA).

When the gate is driving other gates, similar conditions as discussed above will exist at the output of the driving gate. This shows that the load current I_L due to each load gate will flow through the collector of the transistor T_3 , this means the output of the driving gate has to sink its $I_{C3,sat}$ as well as the load currents corresponding to the output in the LOW state. When the output is in the HIGH state, the driving gate sources the leakage currents of load devices which is very small in comparison to the sinking current. Therefore, the TTL is known as *Current sink Logic*.

4.8.3 Fan-Out

The fan-out (N) of a gate depends upon the maximum collector current rating of the transistor T_3 . The total collector current $I_{C3} = I_{C3,sat} + N \cdot I_L$, when the output is in the LOW state.

4.8.4 Power Dissipation

The currents drawn from the V_{CC} supply will be different for the two conditions, i.e., when the output is in the LOW state and when the output is in the HIGH state. The power consumption in the LOW output state $P(0)$ will be due to I_{S1} , whereas the power consumption when the output is in the HIGH state $P(1)$ will be due to the currents flowing through R_{C2} , R_{C3} , and the leakage currents of load devices. Therefore the average power consumption is $\frac{P(0) + P(1)}{2}$

4.8.5 Wired-Logic

If the output of gates are connected together as shown in Fig. 4.13, additional logic is performed. Its detailed operation is given in section 4.6.4.

4.8.6 Propagation Delays

The propagation delays have been discussed in section 4.6.2. The speed of the circuit can be improved by decreasing R_{C3} which decreases the time constant $(R_{C3} \cdot C_o)$ with which the output capacitance charges from 0 to 1 logic level. Such a reduction, however, would increase dissipation and would make it more difficult for T_3 to saturate.

4.8.7 Active Pull-up

It is possible in TTL gates to hasten the charging of output capacitance without corresponding increase in power dissipation with the help of an output circuit arrangement (Fig. 4.18) referred to as an *active pull-up* or *totem-pole* output.

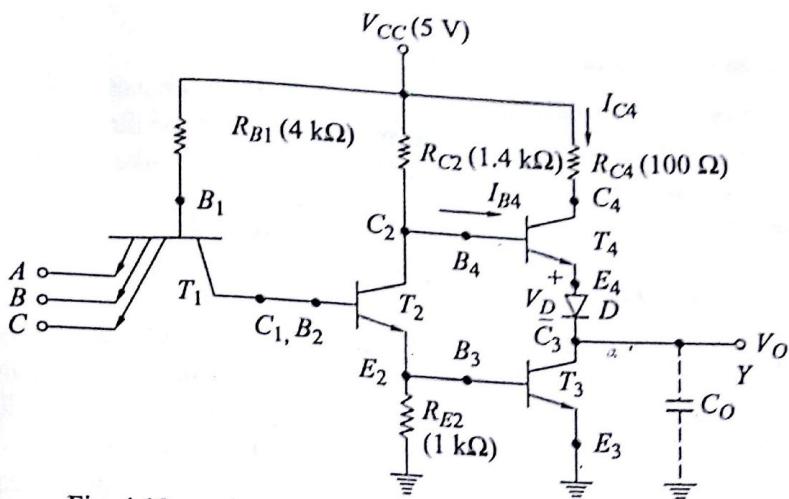


Fig. 4.18 A TTL Gate with Totem-Pole Output Driver

The operation of the circuit can qualitatively be described as: For output Y to be in LOW state, transistor T_4 and diode D are cut-off. When the output makes a transition from LOW to HIGH corresponding to any input going to LOW, transistor T_4 enters saturation and supplies current for the charging of the output capacitor with a small time constant. This current decreases and eventually becomes zero under steady-state condition when $Y = V(1)$.

Diode D is used in the circuit to keep T_4 in cut-off when the output is at logic 0. Corresponding to this, T_2 and T_3 are in saturation, therefore,

$$V_{C2} = V_{B4} = V_{BE3, \text{sat}} + V_{CE2, \text{sat}} = 0.8 + 0.2 = 1.0 \text{ V} \quad (4.8)$$

Since $V_o = V_{CE3, \text{sat}} \approx 0.2 \text{ V}$, the voltage across the base-emitter junction of T_4 and diode D equals $1.0 - 0.2 = 0.8 \text{ V}$, which means T_4 and D are cut-off.

If one of the inputs drops to LOW logic level, T_2 and T_3 go to cut-off. The output voltage cannot change instantaneously (being the voltage across C_o) and because of T_2 going to cut-off, the voltage at the base of T_4 rises driving it to saturation.

As soon as T_2 is cut-off,

$$\begin{aligned} V_{B4} &= V_{BE4, \text{sat}} + V_D + V_o \\ &= 0.8 + 0.7 + 0.2 = 1.7 \text{ V} \end{aligned} \quad (4.9)$$

Therefore,
and

$$I_{B4} = \frac{V_{CC} - V_{B4}}{R_{C2}} = \frac{5 - 1.7}{1.4} = 2.36 \text{ mA} \quad (4.10)$$

$$\begin{aligned} I_{C4} &= \frac{V_{CC} - V_{CE4, \text{sat}} - V_D - V_o}{R_{C4}} \\ &= \frac{5 - 0.2 - 0.7 - 0.2}{0.1} = 39 \text{ mA} \end{aligned} \quad (4.11)$$

Hence, T_4 is in saturation if h_{FE} exceeds $\frac{39}{2.36} = 16.5$.

The output voltage V_o rises exponentially towards V_{cc} with the time constant $= (R_{C4} + R_{CS4} + R_f) C_o$, where R_{CS4} is the saturation resistance of T_4 and R_f is the forward resistance of the diode.

As V_o increases, the base and collector currents of T_4 are decreased and eventually T_4 just comes out of conduction at steady-state. Therefore,

$$V(1) = V_{cc} - V_\gamma(T_4) - V_\gamma(\text{diode}) = 5 - 0.5 - 0.6 = 3.9 \text{ V}$$

Now, if the output is at $V(1)$ and all the inputs go to HIGH, T_2 goes ON. Consequently T_4 and D go OFF and T_1 conducts. The capacitor C_o discharges through T_1 and as V_o approaches $V(0)$, T_3 enters into saturation.

From the above discussion it is clear that the maximum current is drawn from the supply when the output makes a transition from $V(0)$ to $V(1)$ and equals $I_{C4} + I_{B4} = 39 + 2.4 = 41.4 \text{ mA}$.

This current spike generates noise in the power supply distribution system and increases power dissipation in the gate, more so when it is operated at high frequencies.

4.8.8 Wired-AND for Totem Pole Output TTL

Wired-AND connection must not be used for totem-pole output circuits because of the current spike problem discussed above (Prob. 4.16). TTL circuits with open-collector outputs are available which can be used for wired-AND connections.

4.8.9 Open-Collector Output

A circuit with open-collector output is same as the circuit of Fig. 4.16 except for the collector-resistor R_{C3} of T_3 which is missing. The collector terminal C_3 is available outside the IC and the passive pull-up is to be connected externally. Naturally, the advantages of active pull-up are not available in this. Gates with open-collector output can be used for wired-AND operation (Prob. 4.18).

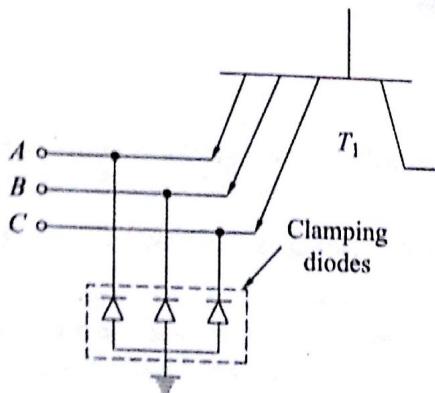


Fig. 4.19 A Portion of a TTL Gate Showing the Clamping Diodes

transitions found in TTL. These diodes shown in Fig. 4.19 clamp the negative undershoot at approximately -0.7 V .

4.8.10 Unconnected Inputs

If any input of a TTL gate is left disconnected (open or floating) the corresponding E-B junction of T_1 will not be forward-biased. Hence, it acts exactly in the same way as if a logic 1 is applied to that input. Therefore, in TTL ICs, all unconnected inputs are treated as logical 1s. However, the unused inputs should either be connected to some used input(s) or returned to V_{cc} through a resistor.

4.8.11 Clamping Diodes

Clamping diodes are commonly used in all TTL gates to suppress the ringing caused from the fast voltage transitions found in TTL. These diodes shown in Fig. 4.19 clamp the negative undershoot at approximately -0.7 V .

4.9 SCHOTTKY TTL

The speed limitation of TTL is mainly due to the turn-off time delays involved in transistors while making transitions from saturation to cut-off. This can be eliminated by replacing the transistors of TTL gate by Schottky transistors (see section 3.6).

With this, the transistors are prevented from entering saturation and hence, there is saving in turn-off time. Schottky TTL gates have propagation delay time of the order of 2 ns which is very small in comparison with the propagation delay time of standard TTL which is of the order of 10 ns. It is a nonsaturating bipolar logic.

4.10 5400/7400 TTL SERIES

TTL 5400/7400 series is the most popular and commonly used series of digital ICs. 7400 devices are used for commercial applications whereas the 5400 devices are used for military applications. The only difference in these two series are in the temperature and the power supply range. The temperature range is 0 °C to 70 °C for the 7400 series and -55 °C to 125 °C for the 5400 series. The supply voltage range is 5 ± 0.25 V for the 7400 series and 5 ± 0.5 V for the 5400 series.

A number of different series of 54 /74- logic family were developed. The series which are currently in production are given in Table 4.2.

Table 4.2 54 / 74- TTL ICs with Numbering Scheme

Series	Prefix	Example
Standard TTL	54-/74-	5400/7400
Schottky TTL	54S-/74S-	54S00/74S00
LOW Power Schottky TTL	54LS-/74LS-	54LS00/74LS00
Advanced Schottky TTL	54AS-/74AS-	54AS00/74AS00
Advanced Low Power	54ALS-/74ALS-	54ALS00/74ALS00
Schottky TTL	54F-/74F-	54F00/74F00
Fast TTL		

Table 4.3 summarises various specifications of 54/74 TTL logic families.

Table 4.3 Specifications of TTL IC Families

Parameter	5400 7400	54S00 74S00	54LS00 74LS00	54AS00 74AS00	54ALS00 74ALS00	54F00 74F00	Units
V_{H}	2	2	2	2	2	2	Volts
V_{L}	0.8	0.8	0.7	0.8	0.8	0.8	Volts
V_{OH}	0.8	0.8	0.8	0.8	0.8	0.8	Volts
V_{OL}	2.4	2.5	2.5	3	3	2.5	Volts
I_{H}	2.4	2.7	2.7	3	3	2.7	Volts
V_{OL}	0.4	0.5	0.4	0.5	0.4	0.5	Volts
I_{OL}	0.4	0.5	0.5	0.5	0.5	0.5	Volts
I_H	40	50	20	20	20	20	μA

(Continued)

- (iii) The low power dissipation series LS, and ALS have minimum power requirement and are used for battery operated circuits. Out of these series ALS series has the minimum propagation delay, therefore it is fast replacing other series.
- (iv) S and AS series have very low propagation delay. The AS series is fast replacing S series because of lower dissipation and propagation delay.
- (v) 74F (FastTTL) family is the most popular choice for new TTL design. It is between 74AS and 74LS in the speed power trade off.

4.11 EMITTER-COUPLED LOGIC (ECL)

Emitter-coupled logic (ECL) is the fastest of all logic families and therefore is used in applications where very high speed is essential. High speeds have become possible in ECL because the transistors are used in difference amplifier configuration, in which they are never driven into saturation and thereby the switching time is eliminated. Here, rather than switching the transistors from ON to OFF and vice-versa, they are switched between cut-off and active regions. Propagation delays of less than 1 ns per gate have been possible in ECL.

Basically, ECL is realised using difference amplifier in which the emitters of the two transistors are connected and hence it is referred to as emitter-coupled logic. A 3-input ECL gate is shown in Fig. 4.21 which has three parts: The middle part is the difference amplifier which performs the logic operation.

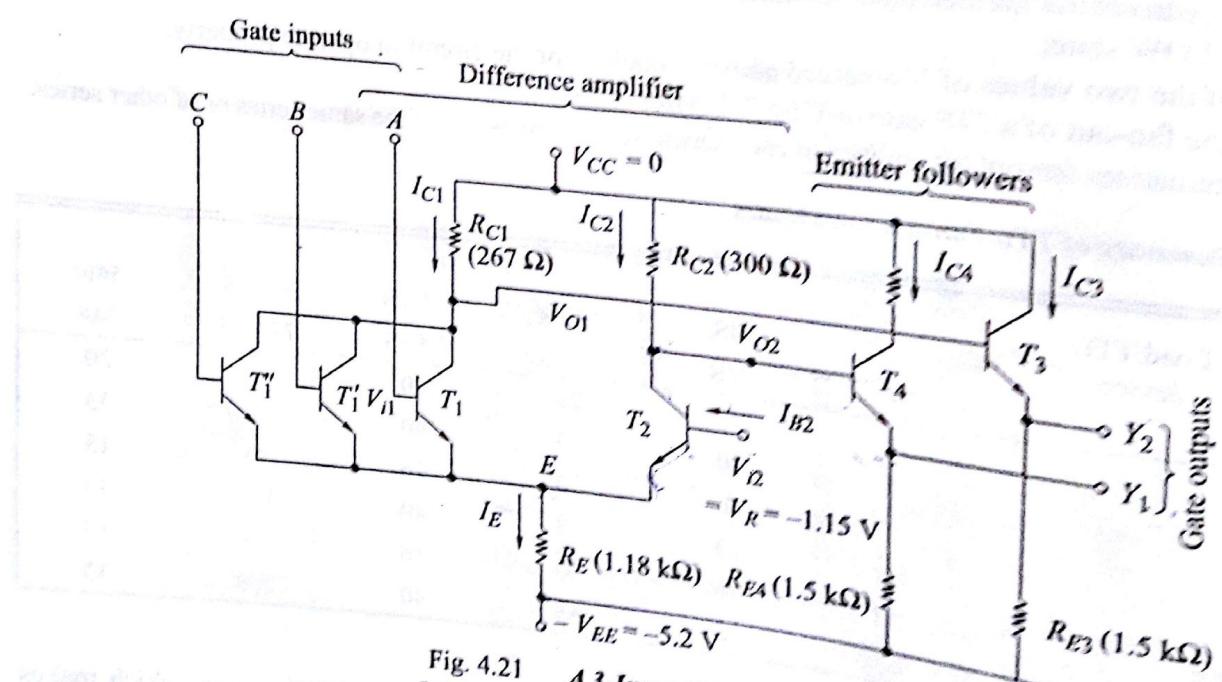


Fig. 4.21 A 3-Input ECL OR/NOR Gate

Emitter followers are used for d.c. level shifting of the outputs, so that $V(0)$ and $V(1)$ are same for the inputs and the outputs. Note that two output Y_1 and Y_2 are available in this circuit which are complementary. Y_1 corresponds to OR logic and Y_2 to NOR logic and hence it is named as an OR/NOR gate.

Additional transistors are used in parallel to T_1 to get the required fan-in. There is a fundamental difference between all other logic families (including MOS logic) and ECL as far as the supply voltage is concerned. In ECL the positive end of the supply is connected to ground in contrast to other logic families in which negative end of the supply is grounded. This is done to minimize the effect of noise induced in the power supply (Prob. 4.22), and protection of the gate from an accidental short circuit developing between the output of a gate and ground (Prob. 4.23). The voltage corresponding to $V(0)$ and $V(1)$ are both negative due to positive end of the supply being connected to ground. The symbol of an ECL OR/NOR gate is shown in Fig. 4.22.

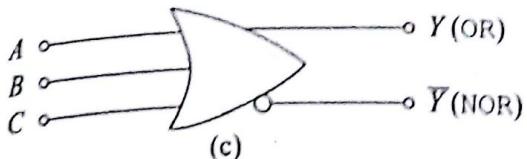


Fig. 4.22 The Symbol for a 3-Input OR/NOR Gate

the supply being connected to ground. The symbol of an ECL OR/NOR gate is shown in Fig. 4.22.

Example 4.2

- (a) Verify that the circuit of Fig. 4.21 performs OR/NOR operations. (b) Show that the transistors in this circuit operate in the active region and not in saturation. (c) Calculate the noise margins. (d) Find the average power dissipated by the gate.

Assume a base-emitter voltage of 0.7 V for a transistor conducting in active region.

Solution

- (a) (i) Assume all inputs to be LOW.

Let us assume that the input transistors T_1 , T'_1 , T''_1 are cut-off and T_2 is conducting in the active region. The voltage at the common emitter is $V_E = V_{B2} - V_{BE2} = -1.15 - 0.7 = -1.85$ V. The current

$$I_E = \frac{V_E - (-V_{BE})}{R_E} = \frac{-1.85 + 5.2}{1.18} = 2.84 \text{ mA}$$

Since $I_{B2} \ll I_{C2}$, therefore $I_{C2} \approx I_E$

$$V_{O2} = -0.3 I_{C2} = -0.3 (2.84) = -0.852 \text{ V}$$

Transistor T_4 will be conducting and the output at $Y_1 = V_{O2} - V_{BE4} = -0.852 - 0.7 = -1.55$ V which is assumed to be $V(0)$.

Therefore, if all the inputs are at $V(0) = -1.55$ V, then the base-to-emitter voltage of the input transistor is

$$V_{BE} = V_B - V_E = -1.55 + 1.85 = 0.3 \text{ V}$$

which is less than the cut-in voltage (0.5 V) of the transistor and hence the input transistors are non-conducting, as was assumed above.

The base and collector of T_3 are effectively at the same potential, hence T_3 behaves as a diode. The current flowing through this diode is approximately 3 mA which corresponds to a voltage of about 0.75 V across the diode. Therefore, the voltage at $Y_2 = -0.75$ V which is assumed to be $V(1)$. This shows that Y_1 and Y_2 are complementary, i.e. $Y_2 = \bar{Y}_1$.

- (ii) Assume at least one input to be HIGH. Corresponding to this the input transistor T_1 is assumed to be conducting and T_2 to be cut-off.

$$\text{Then } V_E = V_B - V_{BE1} = -0.75 - 0.7 = -1.45 \text{ V}$$

Hence, $V_{BE2} = V_{B2} - V_E = -1.15 + 1.45 = 0.3$ V which verifies the assumption that T_2 is cut-off.

The voltage $V_{o1} = -R_{C1} \times I_{C1}$

$$\text{where } I_{C1} = \frac{V_E - (-V_{EE})}{R_E}$$

$$= \frac{(-1.45 + 5.2)}{1.18} = 3.18 \text{ mA}$$

Since the collector current of T_1 is higher than the collector current of T_2 when it is conducting, hence $R_{C1} < R_{C2}$ to get the same voltage levels.

This gives voltage at $Y_2 = -1.55 = V(0)$. The voltage at $Y_1 = -0.75 = V(1)$. From (i) and (ii) above, we see that OR function is performed at Y_1 and NOR at Y_2 . Hence it is an OR/NOR gate. Its voltages corresponding to logic 0 and 1 are -1.55 V and -0.75 V, respectively. The logic swing is 0.8 V.

- (b) From part (a) (i), the voltage between collector and base of T_2 is $V_{C2B} = V_{o2} - V_{I2} = -0.85 + 1.15 = 0.30$ V which shows that the C-B junction is reverse-biased and hence T_2 is operating in its active region.
From part (a) (ii), the voltage between the collector and base of T_1 is

$$V_{C1B} = V_{o1} - V_{I1} = -0.85 + 0.75 = -0.1 \text{ V}$$

This shows that the C-B junction of T_1 is forward-biased but its magnitude is much less than the cut-in voltage and hence T_1 is operating in its active region.

- (c) From part (a)(i), the base-emitter voltage of the input transistors is 0.3 V which is 0.2 V less than the cut-in voltage. Hence the noise margin $\Delta = 0.2$ V.
From part (a) (ii) the base-emitter voltage of T_2 is 0.3 V which again gives a noise margin $\Delta = 0.2$ V. The noise margins are equal and are quite small.

- (d) From part (a) (i),

$$I_{C2} = 2.84 \text{ mA}$$

$$I_{C3} = \frac{5.2 - 0.75}{1.5} = 2.97 \text{ mA}$$

$$I_{C4} = \frac{5.2 - 1.55}{1.5} = 2.43 \text{ mA}$$

$$I_{C1} = 3.18 \text{ mA}$$

$$I_{C3} = 2.43 \text{ mA}$$

$$I_{C4} = 3.97 \text{ mA}$$

Therefore, average $I_E = \frac{2.84 + 3.18}{2} = 3.01$ mA. The total power supply current drain

$$I_{EE} = 3.01 + 2.97 + 2.42 = 8.41 \text{ mA}$$

$$\text{Therefore, the power dissipation } = V_{EE} \cdot I_{EE} = (5.2)(8.41) = 43.7 \text{ mW}$$