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FOURTH SEMESTER

END SEMESTER EXAMINATION [New Scheme] MAY/JUNE 2017

CO/IT-206 COMPUTER ORGANIZATION & ARCHITECTURE

Time: 3:00 Hours Max. Marks: 50

Note: Answer Any **FIVE** questions. All questions carry equal marks.
Assume suitable missing data, if any.

1[a] What is Boolean Algorithm? How many Boolean function can be generated with two variables? Explain it. 5

[b] Design a hardware circuit to implement logical shift, arithmetic shift and circular shift operations. State your design specifications. 5

2[a] Explain in brief how a digital computer system works in a interrupt driven input-output programming. 5

[b] Draw the flow chart of first pass assembler and second pass assembler. Explain its working mechanism. 5

3[a] Give the flow table for register contents used in implementing booth's algorithm for the multiplier = - 6 and multiplicant = + 5. 5

[b] Draw the block digram for the hardware implementation of digital serial, bit parallel BCD subtraction. 5

4[a] Define addressing mode. With the help of example explain different addressing modes. 5

for which the proof holds.

02 Ques...

4 (a) Evaluate the arithmetic statement X = (A+B)*(C+D) using a general register computer with three address, two address and one address instruction format. 5

(b) Explain DMA based data transfer. Give the respective block diagram. 5

5 (a) Explain in brief with the help of a diagram the working of daisy chaining with multiple priority levels and multiple devices in each level. 5

6 (a) Show the memory organization (1024 bytes) of a computer with four 128x8 RAM Chips and 512x8 ROM Chip. How many address lines are required to access memory. 5

(b) Explain in detail the different mappings used for cache memory. Compare them. 5

7 Write short notes:-

[a] CISC and RISC architectures.
[b] Micro program sequencer.
[c] Interrupt and Instruction Cycle.
d) virtual memory

2.5x4