EE214 Serial Adder (Optional)

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You are asked to design a circuit with the following interface:

```
entity SerialAdder is
  port (reset, a,b: in std_logic; s; out std_logic; clk: in std_logic);
end entity;
```

This is supposed to be a sequential circuit with the following behaviour:

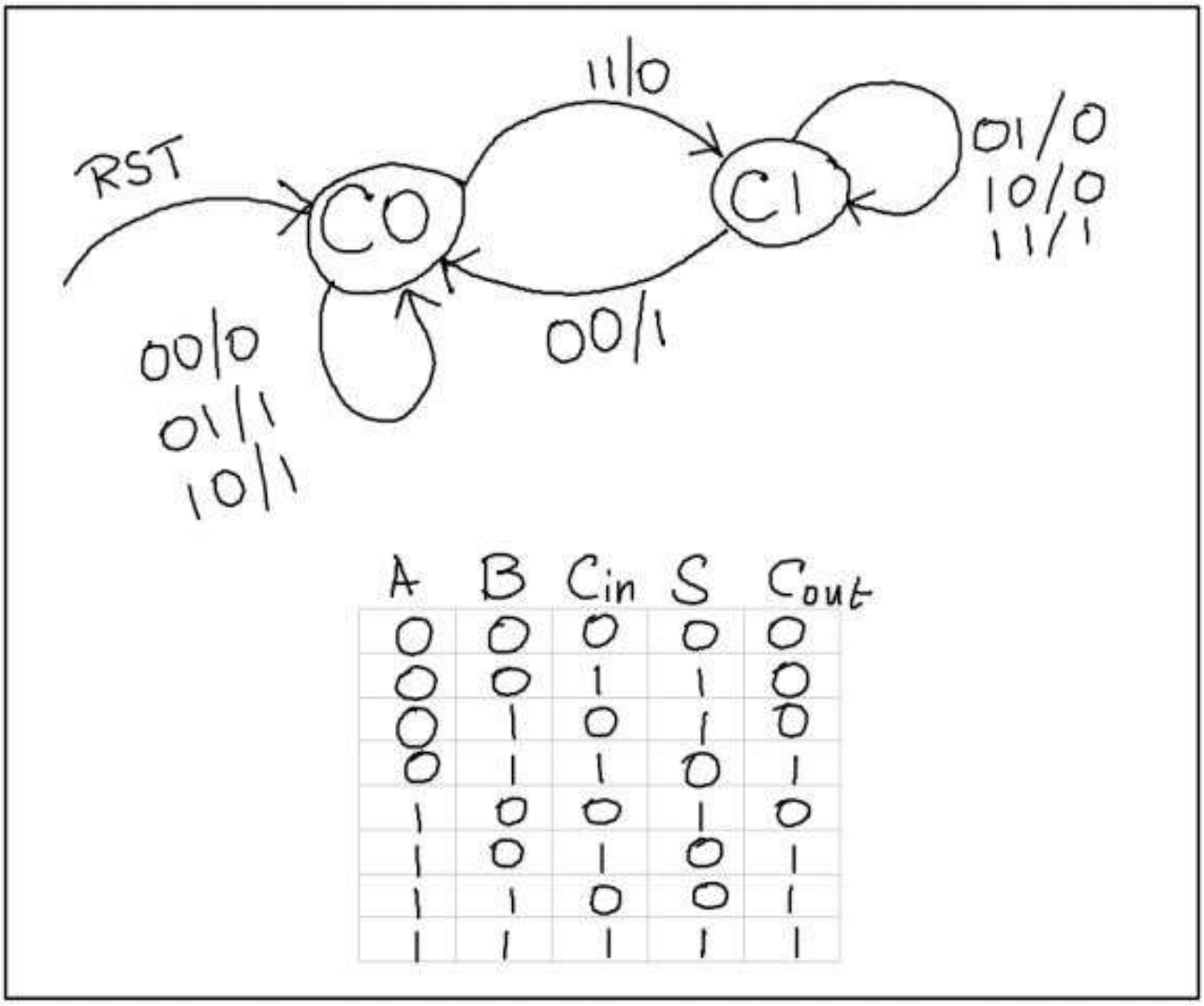
- The clk input is the clock.
- The reset input is used to put the circuit into the initial (reset) state.
- Assume that the circuit is in the initial state at time instant m. Then for any $n \geq m$, the output sequence $\{s(k)\}_{k=m}^{n}$ is related to the input sequences $\{a(k)\}_{k=m}^{n}$ and $\{b(k)\}_{k=m}^{n}$ by the following relation:

```
        a(n) a(n-1) a(n-2) ....   a(m)
+       b(n) b(n-1) b(n-2) ....   b(m)
-------------------------------------
=       s(n) s(n-1) s(n-2) .....  s(m)
```

  Thus, the output sequence can be thought of as a sum of the input sequences.

1. Show that this circuit can be implemented by a Mealy finite state machine (draw the state transition graph) (5 marks)
2. Describe an architecture for your design (in VHDL) (5 marks).
3. Generate a trace-file to test your design. The input sequence must ensure that all states and transitions are visited during the test (5 marks).
4. Perform simulation and scan chain. Show results to your TA (5 marks).

- **Serial Adder State Diagram and Truth Table**



A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure1 : State Diagram

This design uses Mealy state machine. There are 2 states --> C0 state and C1 state. When inputs are 00,01,10 then the machine remains in the same state. Output is 0, 1, 1 respectively.

If the state is C0 and the input is 11 the machine changes it state to C1 and output is 0.

If the machine is in C1 state and input is 01, 10, 11 it remains in the same state. And the output is 0, 0, 1 respectively.