EE214: Homework (Wednesday Batch)

Wadhwani Electronics Lab, IIT Bombay

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Please complete the following assignments before your next lab turn, as these designs will be used in next in-Lab experiment.

1. (a) Review Behavioural Architecture Description in VHDL including conditional signal assignment, select signal assignment, process block, if-then-else and for loop.
   (b) Watch Prof. Dinesh Sharma's lectures on Behavioural Description
   (c) Complete the following description of **1-bit left shifter** in VHDL using conditional signal assignment. (When S = '1', then Y should be 1-bit left shifted version of X. When S = '0', Y should be same as X)

```
library ieee;
use ieee.std_logic_1164.all;

entity ShiftLeftByOne is
    port (X: in std_logic_vector(7 downto 0);
          S: in std_logic;
          Y: out std_logic_vector(7 downto 0)
          );
end entity ShiftLeftByOne;

architecture Easy of ShiftLeftByOne is
begin
Y(7) <= ___ when ____ else ____;
.......
.......
.......
end Easy;
```

   (d) Simulate the above design in Modelsim and validate its functionality using the given Tracefile.
   NOTE: TRACEFILE format
   Input{S X7 X6 X5 X4 X3 X2 X1 X0} Output{Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0} MASK{11111111}

2. (a) Complete the following description of **8-bit adder** in VHDL using process block.

```
library ieee;
use ieee.std_logic_1164.all;

entity add_8bit is
    port (
        A: in std_logic_vector(7 downto 0);
        B: in std_logic_vector(7 downto 0);
        sum: out std_logic_vector(7 downto 0);
        carry_out : out std_logic
    ) ;
end add_8bit;

architecture Beh of add_8bit is

begin
    add : process(_______)
    variable sum_var : std_logic_vector(7 downto 0):= (others=>'0');
    variable carry_prop : std_logic_vector(8 downto 0):= (others=>'0');
    begin
        for i in _______ loop
            .........
            .........
        end loop;
        sum <= sum_var;
        carry_out <= carry_prop(8);
```

```
    end process ; -- add
end Beh ; -- Beh
```

(b) Simulate the above design in Modelsim and validate its functionality using the given Tracefile.
NOTE: TRACEFILE format
Input{A7 A6 A5 A4 A3 A2 A1 A0 B7 B6 B5 B4 B3 B2 B1 B0} Output{carry_out sum7 sum6 sum5 sum4 sum3 sum2 sum1 sum0} MASK{111111111}