

EE 214: Digital System Design Lab

Instructor: Prof. Maryam Shojaei

Course Overview

- ❑ EE 214 lab course complements EE 224 theory course.
- ❑ Basic knowledge of logic gates, combinational circuits, flip flops, counters and registers is expected.
- ❑ Learning objectives are as follows.
 1. Design, description, simulation and synthesis of digital subsystems using VHDL and subsequently their implementation on CPLD.
 2. Validation of the designs using scan chain environment.

Lab Timing

The class is divided in two batches:

Batch A (Wednesday)
(For B.Tech. students)

Batch B (Thursdays)
(For DD students)

Lab Organization

- ❑ We shall use Microsoft Teams and the Moodle for the lab instructions.
- ❑ Experiments will be done individually.
- ❑ **The lab kit** containing the following items is shipped to your address.
 - Krypton (a CPLD board)
 - TIVA-C board (a microcontroller board)
 - A bootable pendrive with necessary software installed
 - Accessories

Lab Organization

- Recorded training videos on the Quartus, Krypton and scan chain will be shared with you.
- You **must** ship the working kit back to us **within 3 days** after the lab end semester exam. The grades will be kept on hold till we receive the lab kit.
- The instructions for the acknowledgement of receipt of the lab kit and returning back the kit will be posted on the moodle.

The Lab Kit

- Wadhwani Lab Staff have been working very hard to prepare, test, pack and ship the lab kits for you so that you do not miss hands-on experience even under these special conditions of online semester.



The Lab Kit

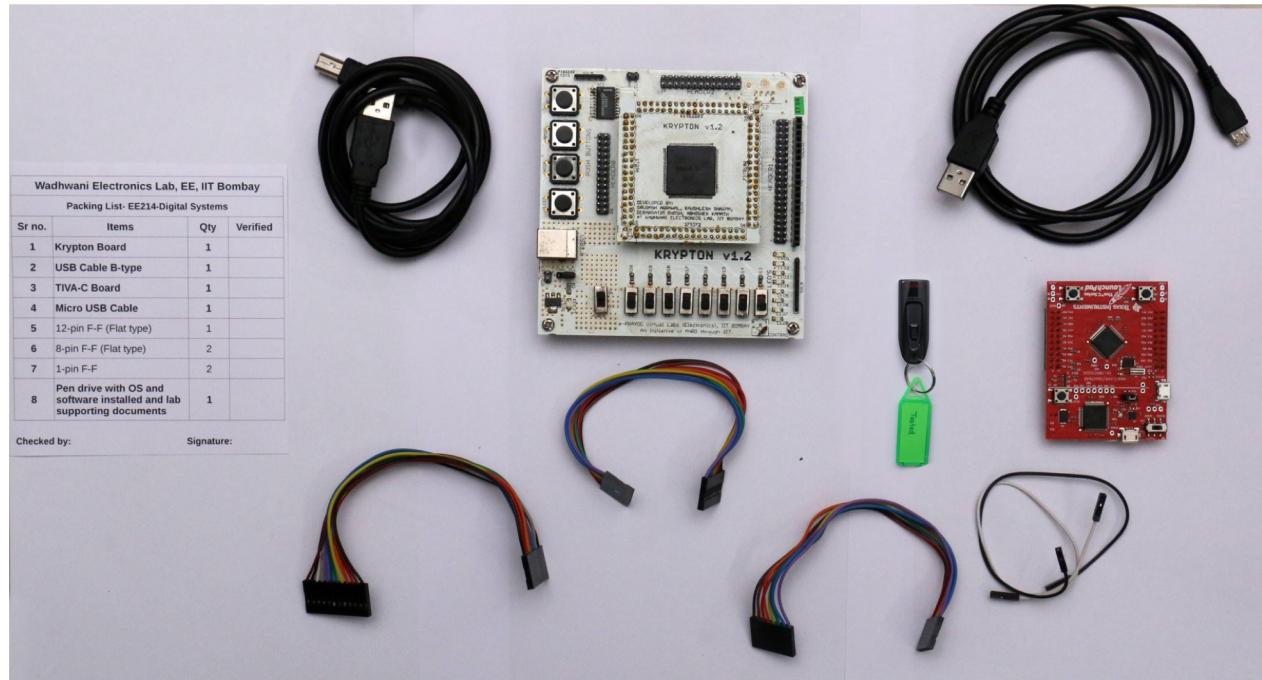
- You thank Wadhwani Lab Staff only by working hard proactively and honestly :-)



Amit, Sadanand, Shahin, Rabiya, Ankur, Suraj, Varsha, Mahesh, Sandesh, Swapnil

The Lab Kit

- The Krypton has been designed, developed and hand-soldered in WEL by very dedicated lab RAs and the lab staff!
- WEL is thankful to SriJATI Lab and Texas Instruments for their generous donation of TIVA-C boards for Digital Systems Lab.
- Please respect all by careful handling the kit items during the experiments.
- **Do not experiment with the kit unless we run the session on “Using the lab kit” for you!**



Lab Activities

- This is the first time we are running the lab online.
- Most of the lab sessions will require you to complete pre-lab work ahead of a live lab-session. This needs proper time management from your side.
- Some lecture videos by senior professors will be uploaded for background theory.
- We shall also conduct quizzes to test your understanding during the semester. So please remain in sync!!

Lab Activities

- Most of the lab sessions are designed such that you complete the work in the given lab slot itself provided you are well prepared.
- You must demonstrate your work to the TA before you sign-off and submit your report on moodle interface.
- Please do not copy the solutions/reports. You will get 0 points for that experiment if you attempt to cheat .

Report Submission for the Lab Experiment

- The simulation and scan chain verification demo should be presented to the TA during the lab session.
- The zipped VHDL project and the report to be uploaded before you sign off the online lab session.
- The entire report should be uploaded individually.
- Save a backup of your results and codes on the cloud or pen-drive.

Attendance

- ❑ Attendance is **mandatory**.
- ❑ If you can not attend a lab session for some genuine reasons, please inform your TA and the instructor in advance.
- ❑ In such situations complete your work before the next lab turn and upload the report/VHDL code/results.

Grading policy

- Online lab performance (experiments) : 25 %
- Reports/VHDL code/Experiment results : 25%
- Quizzes : 20 %
- Midsem : 15 %
- Endsem : 15 %



End of Presentation