Problem statement

Design, a logic circuit for generating the 3-bit sequence given below. Note that, the first value in the sequence should appear at output on reset and the next sequence in subsequent clock cycles.

$\overline{\text{Up}}$/Down (UD) input bit is used to choose the direction e.g. UD =0 then output should be in sequence shown else in reverse sequence.

The first output in the given sequence is the output in the reset state, the outputs are represented by D0-D7 in the timing diagram but each one of them will be a 3-bit number in your question.

D0 always represents the reset state's output.

The actual sequence for which you have to design FSM will be **sent by e-mail.**
Following example illustrates a sequence for your understanding.

Note that following sequence is not your question sequence and it's only an example.

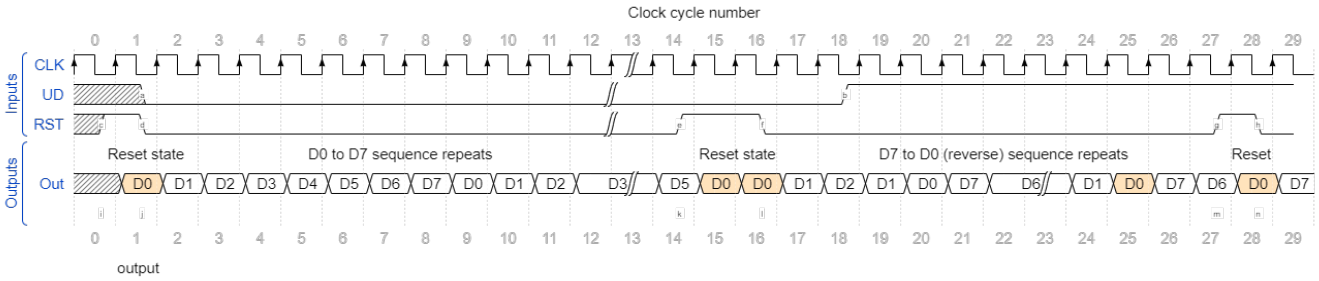
Reset = 1

Forward sequence UD=0

Representation	... D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1 ...
Expected output sequence (3-bit for each output D0 to D7)	... 3	4	5	2	3	6	0	7	1	4	5	2 ...

Reverse sequence UD=1

check below timing diagram:



Submit your pen-paper design images on Moodle well before the **deadline1**.

Tracefile Format:
UD Reset CLK<space>OUT 3-BITS(MSB- LSB)<space>Mask bits

Map your Design to Krypton as shown below:

Krypton Pin	Design IO
LED 1 (Pin_58)	output(2)MSB
LED 3 (Pin_55)	output(1)
LED 5 (Pin_52)	output(0)LSB
1 Hz (Pin 18)	clock input
Sw1 (Pin_48)	inputs UD
Sw8 (Pin_39)	input Reset