Experiment: 4-bit Adder

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## Overview of the experiment:

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| The purpose of the experiment was to design a 4-bit ripple carry adder, implement the design using VHDL, and simulate the design using Quartus.  The approach, design and results have been discussed below. |

## Approach to the experiment:

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| The design first adds the LSB from both the numbers, their resultant will be the LSB of the output bit. The carry then generated should be added to the next set of bits. This is done till all the 4 bits are added. |

## Design document and VHDL code if relevant:

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| Ripple Carry: The ripple carry adder performs bit-wise addition of each of the bits of the inputs. It uses Full Adders to add the bits and the carry from the previous set of bits. The carry is set to 1 for the addition of LBSs.  Initialize Carry = 0  For i from 0 to 3:  A(i) + B(i) + Carry(i) = Out(i) + Carry(i+1)  The output will be Out and Carry(4) |

## RTL View:

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## DUT Input/Output Format:

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| Input: <A3A2A1A0B3B2B1B0><space><CoutS3S2S1S0><space><Mask-bits>  Output: <A3A2A1A0B3B2B1B0><space><CoutS3S2S1S0>  Example testcases:  **Input:**  00001011 01011 11111  00001100 01100 11111  00001101 01101 11111  00001110 01110 11111  00001111 01111 11111  **Output:**  00001011 01011  00001100 01100  00001101 01101  00001110 01110  00001111 01111 |

## RTL Simulation:

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## Gate-level Simulation:

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## Krypton board\*:

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| Map the logic circuit to the Krypton board and attach the images of the pin assignment and output observed on the board (switches/LEDs). |

## Observations\*:

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| You must summarize your observations, either in words, using figures and/or tables. |

## References:

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| Nil |

\* To be submitted after the tutorial on ”Using Krypton.