Experiment 0: Combinational Circuits 1

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## Overview of the experiment:

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| The experiment was to count the number of set bits in an 8-bit input. The purpose of this experiment was to familiarize with logic design and implementation in VHDL, and simulation using Modelsim-Altera in Quartus.  The experiment was performed using the Full Adder implementation from the previous lab as well as a new file set\_bit\_counter which uses 7 FA instances to add all the input bits and outputs a 4-bit vector.  The report contains |

## Approach to the experiment:

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| The number of 1 in the input will be equal to the sum of all the input bits.  7 Full-Adders (FA) (which were designed in the previous lab) were used to add each of the 8 bits and output a 4-bit vector depicting the final sum of all the bits. The first 4 FA were used to add all the 8 bits and get the first bit of the output. The Carry from each of these FA were then added using 2 more FA to produce the second bit. The Carry from the last 2 FA were then again added using one FA which would produce the last 2 bits of the output. |

## Design document and VHDL code if relevant:

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| set\_bit\_counter: This involves 7 instances of FA (Full Adder) which add all of the input bits and output 4 bits which correspond to the final output. The first 4 FA sum all the individual bits together to decide the LSB of the output. The carries from these FA are then added using 2 more FA to find the second bit. The carries produced are then finally added to get the remaining 2 MSB.  The full adder entity-architecture was taken from the design in previous lab. |

## RTL View:

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## DUT Input/Output Format:

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| <MSB to LSB>  Input: <x7x6x5x4x3x2x1x0><space><y3y2y1y0><space><mask-bits>  Output: <y3y2y1y0>  Where xi are the input bits, yi are the output bits.  Some testcases from the tracefile:  **Input:**  00010111 01000 11111  00011000 01001 11111  00011001 01010 11111  00011010 01011 11111  00011011 01100 11111  00011100 01101 11111  **Output:**  00010111 01000  00011000 01001  00011001 01010  00011010 01011  00011011 01100  00011100 01101 |

## RTL Simulation:

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## Gate-level Simulation:

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## Krypton board\*:

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| Map the logic circuit to the Krypton board and attach the images of the pin assignment and output observed on the board (switches/LEDs). |

## Observations\*:

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| You must summarize your observations, either in words, using figures and/or tables. |

## References:

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| Nil |

\* To be submitted after the tutorial on ”Using Krypton.