

# UART Project Report

Team Name: Diode Destroyers

## Team Members:

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## Objective:

To design and verify a robust UART (Universal Asynchronous Receiver-Transmitter) module in Verilog for serial communication, implementing internal loopback to ensure bit-perfect data transmission and reception.

## UART Frame Format (8N1):

- Start Bit:** 1 bit (Logic Low)
- Data Bits:** 8 bits (LSB first)
- Parity:** None
- Stop Bit:** 1 bit (Logic High)

## Baud Rate Calculation:

For a **50 MHz** system clock and **9600 Baud**:

- **Transmitter (TX):**  $50,000,000 / 9600 = 5208$  cycles.
- **Receiver (RX):** Needs 16x oversampling.  $50,000,000 / (9600 * 16) = 325$  cycles.

## TX FSM Diagram:

- **IDLE:** Wait for wr\_enb.
- **START:** Pull tx line Low for 1 baud period.
- **DATA:** Shift out 8 bits of data.
- **STOP:** Pull tx line High; return to IDLE.

## RX FSM Diagram:

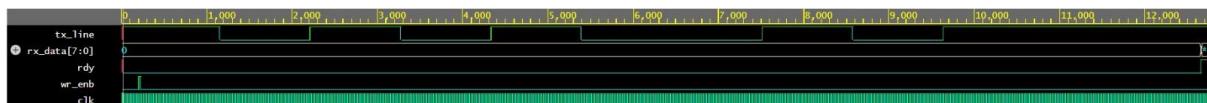
- **IDLE/START:** Wait for falling edge; sample at mid-point (8th tick).
- **DATA:** Sample 8 bits at the center of each bit period (16th tick).
- **STOP:** Verify stop bit and assert rdy signal.

## Testbench Strategy:

A self-checking loopback test was used. The Transmitter output (tx\_line) was fed directly into the Receiver input. The testbench initialized a transmission of 8'hA5 and waited for the Receiver's rdy flag to verify the output data.

## Results & Waveforms:

- **Simulation Result: SUCCESS**
- **Data Transmitted: A5**
- **Data Received: A5**
- **Observation:** The rdy flag asserted exactly after the 10th bit (Stop bit) was processed, confirming timing accuracy



## Conclusion:

The UART module successfully achieved stable 9600 baud communication. The design is modular, scalable for different baud rates, and verified for hardware deployment on a 50 MHz FPGA system.