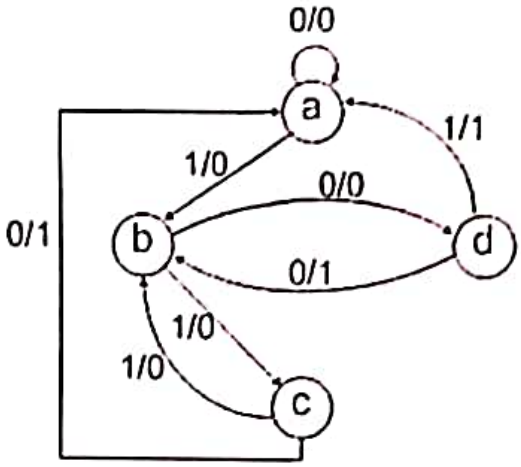
Motilal Nehru National Institute of Technology Allahabad
Department of Electronics & Communication Engineering
End-Semester (Even) Examination (April-2017)
Programme: B. Tech, IV-Semester (ECE and EE)
Subject: Digital Electronics (EC-1402)

Time: 3:00 Hours **Maximum Marks: 60**

NOTE: Attempt all the questions and assume the necessary data if required.

Q1 Design a clocked sequential circuit using T flip-flops for the following state diagram. Use the state reduction if possible. (8)



Q2 (a) A combinational circuit is defined by the functions: (8)

$F_1(A, B, C) = \sum m(3, 5, 6, 7)$ and $F_2(A, B, C) = \sum m(0, 2, 4, 7)$

Implement the circuit using PLA.

(b) Design and implement a BCD to seven segment decoder circuit.

Q3 (a) Design and implement a 4-bit random sequence generator using synchronous sequential circuit. (8)

(b) What is race around condition in a J-K Flip-Flop? Explain how it occurs? Suggest the methods to overcome the race-around difficulty.

Q4 (a) What are the different performance parameters of a logic family and explain them. (8)

(b) Verify the truth table of NAND gate using TTL and CMOS logic family.

Q5 (a) Design and explain the operation of Astable multivibrator. And derive the expression for duty cycle. (8)

(b) With the help of an example explain the design methodologies of a digital VLSI chip and compare them

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Q6 (a) With the help of an example explain the operation of different shift registers. And state their applications. (8)

(b) Design an asynchronous counter with counting sequence as 2, 3, 4, 5, 6, 2, 3 ....

Q7 (a) Realize S-R and D flip-flops using J-K flip-flop. (8)

(b) Design and implement a 2-bit comparator circuit. And also explain its advantages. (4)

Q8 Design a combinational circuit defined by the following three functions:

$F_1 = x'y' + xyz'$

$F_2 = x' + y$

$F_3 = xy + x'y'$

Design a circuit with a decoder and external gates.

END