Department of Computer Science and Engineering
Motilal Nehru National Institute of Technology
End Semester Exam, Computer Organization (CS1403)
B.Tech (IT, CS) IV Semester
Time: 3 Hour, MM:60

Note: There are 5 questions. Attempt any 4. Avoid story telling. Be crisp and concise while answering questions.

1. **Pipelined Datapath**

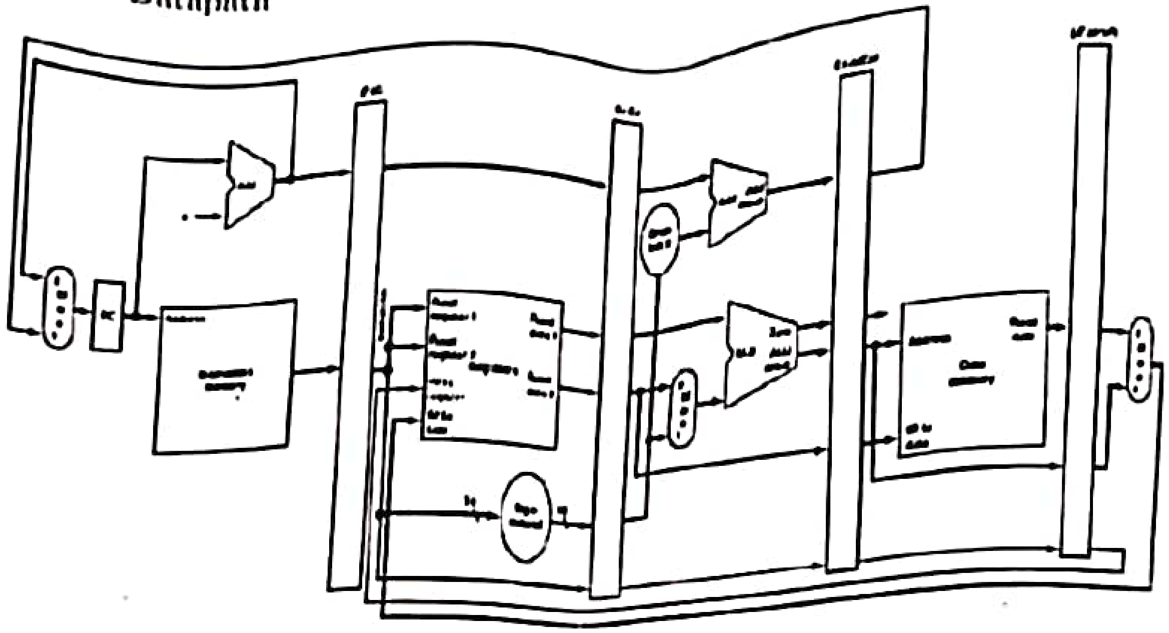

Figure 1: Schematic for Pipeline data-path

(a) Consider the execution of following instruction sequence over datapath given in Figure.1:

```
lw  $t0,  10($t1)
sw  $t3, 20($t4)
add $t5,  $t6,  $t7
sub $t8,  $t9,  $t10
```

Show and explain explicitly the contents of Pipeline Registers (IF/ID, ID/EX, EX/MEM, MEM/WB) after every clock cycle starting from clock cycle 1 to clock cycle 6.

(b) For each of the following sequences of instructions, state: (1) Whether a data hazard exists in the pipelined datapath of Figure.1 (2) If that data hazard necessarily results in a stall, and (3) Which forwarding paths (from the output of which stage to the input of which stage) are necessary to eliminate or minimize the stall.

-
  ```
  lw $s0, 4($s1)
  addi $s2,$s0,10
  ```

-
  ```
  slt $s1,$s2,$s3
  sw $s1,4(4$t0)
  ```

2. Cache Memory:

(a) Suppose a computer has 4-way set associative cache with 64 one word (4 byte) blocks. Given the sequence of byte addresses 8, 64, 96, 128, 64, 96, 256, 192, 24 show the final cache contents and state the numbers of cache hit and miss.

(b) Assuming a cache of 16K blocks and a 32 bit address, find the total number of sets and the total number of tag bits for caches that are direct mapped, two-way and four-way set associative, and fully associative.

(c) Draw a picture showing the organization of a 4-way set associative cache having 1K one word blocks. Show any multiplexers, comparators, gates etc. needed. Show how a 32 bit address is mapped to a cache block.

(d) Differentiate between "read miss" and "write miss" both for instruction and data wherever applicable. What are the different policies to handle them? If it is an instruction "read miss", how it is handled.

3. **Virtual Memory:**

(a) Write 100-150 words essay about your understanding of Virtual Memory.

(b) What modifications you want to make in your essay of part (a) if suppose your machine is running two Virtual Machines (VM) also.

(c) Suppose that a system has a 32-bit(4GB) virtual address space. It has 1GB of physical memory, and uses 1MB pages.(i) How many virtual pages are there in the address space? (ii) How many physical pages are there in the address space? (iii) How many bits are there in the page offset? (iv) How many bits are there in the virtual page number? (v) How many bits are there in the physical page number? (vi) What would be the size of page table?

(d) In part (c) above if you are getting the page table size bigger than physical page size, how this situation can be amicably solved?

4. **Arithmatic and other Freebies**

(a) Draw the optimized Multiplier and Divider hardware discussed in class with appropriate control signals. Observe and write the similarities between these two hardwares. How can we use the same hardware both for multiplication and division. Explain. (Hint: in these hardwares only four elements are there: two registers, one ALU and one abstract control test unit)

(b) Show step by step implementation of 7 ÷ 2 and Booth's multiplication of 3×-2 on the above hardware.

(c) In microprogrammed control unit design of MIPS given in Assignment, explain briefly the role of the following elements:

- Dispatch ROM1 and Dispatch ROM2
- 2 bit Address Control field in microinstruction
- The 4×1 multiplexor.

5. **MIPS and Cache Performance**

(a) Consider the following Array code in C:

```
void shift(int a[], int n){
int i;
for(i=0;i!=n-1;i++)
a[i]=a[i+1];
}
```

(i) Translate this function into MIPS assembly. (ii) Convert this function into pointer-based code (in C). (iii) Translate your pointer-based C code from (ii) into MIPS assembly. (iv) Compare the number of temporary registers (t-registers) needed for your array-based code from (i) and for your pointer-based code from (ii).

(b) Assume for a given machine and program: instruction cache miss rate is 2%, data cache miss rate is 4%, miss penalty is always 40 cycles, CPI of 2 without memory stalls and frequency of load/stores is 36% of instructions.(i) How much faster is a machine with a perfect cache that never misses? (ii) What happens if we speed up the machine by reducing its CPI to 1 without changing the clock rate? (iii)What happens if we speed up the machine by doubling its clock rate, but if the absolute time for a miss penalty remains same?