End-Semester Examination 2015-16
B. Tech. IV Semester (ECE+EE)
Course: Digital Electronics (EC-1402)

Duration: 3 Hours **M. Marks: 60**

Note: Answer all the Questions. Notations have their usual meaning. Assume any suitable data if required.

1(a) Define multiplexer. List the applications of multiplexer. Implement two inputs EX-OR using 2x1 multiplexer. (3)

(b) A combinational circuit is defined by the functions: (7)

$F_1(A,B,C) = \Sigma(3,5,6,7)$

$F_2(A,B,C) = \Sigma(0,2,4,7)$

Implement the circuit with a PLA having three inputs, four product terms, and two outputs.

2(a) What do you mean by Race-around condition? Explain. (3)

(b) Design a sequence generator to generate the sequence ....1011110.... (7)

3(a) Define (i) noise margin (ii) fan-out (iii) figure of merit. (3)

(b) Draw the circuit of a 3-input TTL NAND gate and explain its operation. (7)

4(a) What do you mean by Lock Out problem in synchronous counters? Explain. (3)

(b) Design a mod-5 counter using J-K flip-flops. Incorporate in your design a provision to ensure that if an unused state occurs, the next clock pulse will reset the counter to $Q_2Q_1Q_0 = 000$. (7)

5(a) What is the basic difference between a Johnson counter and a Ring counter? How many states does a 4-bit Johnson counter have? (3)

(b) Design and implement a circuit to convert Excess-3 code to BCD code using NAND gates only. (7)

6(a) Implement the four Boolean functions listed using three half-adder circuits. (3)

$$D = A \oplus B \oplus C$$

$$E = \bar{A}\,B\,C + A\,\bar{B}\,C$$

$$F = A\,B\,\bar{C} + \left(\bar{A} + \bar{B}\right)C$$

$$G = A\,B\,C$$

(b) Design a clocked sequential circuit for the state diagram shown below. Use J-K flip- flops. (7)