End-Semester Examination 2014-15
B. Tech. IV Semester (ECE+EE)
Course: Digital Electronics (EC-1402)

Duration: 3 Hours

M. Marks: 60

**Note: Answer all the Questions. Notations have their usual meaning. Assume any suitable data if required.**

1.(a) What is the basic difference between a Johnson counter and a Ring counter? How many states does a 4-bit Johnson counter have? (3)

(b) Design a sequence generator to generate the sequence ...1101011... (7)

2.(a) A company has four directors, namely A, B, C and D, and their corresponding percentage of shares in the company are 40,30,20 and 10 respectively. The directors are eligible to vote according to their percentage of shares (e.g. A can cast 40 votes; B can cast 30 votes and so on) in the board of directors meeting and two-third majority is required to pass any resolution. Design a combinational circuit to indicate whether a resolution is passed or not. (3)

(b) Design a sequential circuit with J-K flip-flops to satisfy the following state equations: (7)

$$A(t+1) = \bar{A}\bar{B}CD + \bar{A}B\bar{C} + ACD + A\bar{C}\bar{D}$$

$$B(t+1) = \bar{A}C + C\bar{D} + \bar{A}B\bar{C}$$

$$C(t+1) = C$$

$$D(t+1) = \bar{B}$$

3 (a) Using the conversion method, convert an S-R flip-flop to a J-K flip-flop. (3)

(b) A combinational circuit is defined by the functions: (7)

$$F_1(A,B,C) = \Sigma(3,5,6,7)$$

$$F_2(A,B,C) = \Sigma(0,2,4,7)$$

Implement the circuit with a PLA having three inputs, four product terms, and two outputs.

4.(a) What is the basic difference between ROM and PLA? Draw the logic construction of a 32 X 4 ROM. (1+2)

(b) Design a counter with the following binary sequence: 0, 4, 2, 1, 6 and repeat. Use J-K flip-flops. (7)

5.(a) What is race around problem? How can we avoid this problem? (3)

(b) Draw the circuit of an IC DTL gate and explain its operation. (7)

P.T.O.

6.(a) Realize the following function using a 4 x 1 Multiplexer and external logic gates. Connect variables A and B to the select lines $s_1$ and $s_0$ respectively. (3)

$$F(A, B, C, D) = \sum(0, 2, 4, 6, 8, 12, 14).$$

(b) Design a clocked sequential circuit for the state diagram shown below. Use J-K flip- flops. (7)