Prakhar Diwan

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Education

Indian Institute of Technology Bombay **Jul '18 - Aug '23**
Dual Degree (Bachelors & Masters of Technology) in Electrical Engineering ***CPI: 9.61/10***

- Ranked **3rd** among **78** Dual Degree students in Electrical Engineering Department
- Awarded **Institute Academic Prize**, awarded to the top two students from each department
- Received a **Minor** degree in **Computer Science & Engineering**
- Selected for a fully-funded **Mitacs Globalink** research internship at **École Polytechnique de Montréal, Canada**
- Granted the **DAAD-WISE** Scholarship for research work at **University of Tübingen, Germany**
- Among **16 out of 1000+** students granted **branch change** to Electrical Engineering Department
- Secured an All India Rank **540** in **JEE-Main** and **99.69** percentile in **JEE-Advanced** among **2.3 Lakh** candidates

Publications

Lichen: Leveraging Coupled Heterogeneity **Best Paper Award Nominee**
38th International Conference on VLSI Design and 24th International Conference on Embedded Systems (VLSID 2025)

HIDC: Heterogeneous-ISA Dynamic Core
26th IEEE International Conference on High Performance Computing & Communications (HPCC 2024)

MIST: Many-ISA Scheduling Technique for Heterogeneous-ISA Architectures
37th International Conference on VLSI Design and 23rd International Conference on Embedded Systems (VLSID 2024)

Research Experience

Heterogeneous-ISA Polymorphic Architectures for Energy Efficiency **Jun '22 - Jul '23**
Guide: Prof. Virendra Singh, Electrical Engineering, IIT Bombay *Masters Thesis*

- Conducted detailed literature survey on **heterogeneous** and **reconfigurable** multicore architectures
- Analysed PPA impact of ISA and microarchitectural heterogeneity using **Gem5** simulator and **McPAT**
- Devised morphing and migration methods to leverage diversity in **ISA** (ARM & x86) and **execution semantics**
- Achieved **50%** reduction in energy delay product over **heterogeneous-ISA CMP** for **SPEC** benchmarks

Increasing Energy Efficiency of 1D CNN Accelerator **May '21 - Aug '21**
Guide: Prof. Oliver Bringmann, Computer Science, University of Tübingen *Research Internship*

- Implemented intra-inference controller for power gating memory macros in **SystemVerilog**
- Achieved **16.25%** reduction in power consumption by use of **computational sprinting** on accelerator
- Developed a **Huffman encoder** in **Python** for weight compression and neural network training framework
- Designed a **scalable Huffman decoder** for encoded weights stored in memory with compression rate of **16.67%**

Software Model for IITB-AI/ML Accelerator **May '21 - Oct '21**
Guide: Prof. Madhav P. Desai, Electrical Engineering, IIT Bombay *Research Project*

- Collaborated on developing a model for hardware accelerator in **C** for high-level synthesis (**HLS**) and verification
- Integrated point-wise unary operators in model with support for various data types and tensor configurations

Non-invasive Extraction of Body Vitals | Epocare, Mumbai **May '20 - Jul '20**
Awarded recommendation letter from CEO Deepak Kumar for outstanding contribution *R&D Internship*

- Analysed and implemented core image processing algorithms in **MATLAB** for product's medical imaging platform
- Developed a module to measure **SpO2**, **breathing** and **heart** rate based on **Sophia** method using RGB video of wrist

Automatic Image Segmentation **Oct '19 - Aug '20**
Guide: Prof. Vikram Vishal, Earth Sciences, IIT Bombay *Research Project*

- Extracted 16 features for each pixel of SEM images for classification into 4 classes of materials
- Created the image data set for training and testing segmentation model by precise labelling of pixels
- Implemented Random Forest and a modified pre-trained U-Net model for the segmentation task

Technical Skills & Interests

HDLs & Programming: Verilog, SystemVerilog, C/C++, Python, MATLAB, LaTeX, Assembly, Embedded C
Interests: Digital Design, Computer Architecture, Machine Learning, Quantum Computing

Professional Experience

Texas Instruments India

Senior Digital Design Engineer **Feb '25 - Present**

- Owned digital calibration and correction systems for three **high-speed ADCs** with diverse analog architectures
- Mentored junior engineers on RTL design and verification workflows, strengthening team capabilities
- Partnered with cross-functional analog, firmware and lab teams to drive device closure across multiple products

Digital Design Engineer **Aug '23 - Jan '25**

- Designed datapath blocks and feedback loops in **SystemVerilog** to maintain ADC SNR across PVT corners
- Integrated ARM Cortex R5 core into calibration system to estimate and apply corrections for optimal ADC performance
- Utilized **cocotb** to rapidly build fully automated and regressable tests in **Python**, accelerating verification cycles
- Collaborated with DFT and PD teams to drive synthesis and timing closure using Cadence **Genus** and **Tempus**
- Analysed power, performance and area tradeoffs for design approaches using Cadence **Joules** and **Voltus**

Projects

Neural Networks on FPGA for Image Classification **Jan '22 - May '22**

- Designed an artificial neural network (ANN) with 2 hidden layers for classification on CIFAR-10 dataset
- Automated RTL generation for ANN from its description using **Python**-based **HLS** flow
- Performed simulation-based verification of the design by giving images as inputs through testbench

Pipelined RISC Processor **Jan '21 - May '21**

- Designed a **16**-bit, **8**-register, **5-stage pipelined RISC** processor based on a 15-instruction custom ISA
- Described the design using **Verilog**, synthesized it using **Intel Quartus** and verified the design using **ModelSim**
- Implemented data and control **hazard mitigation** unit and **data forwarding** unit for improving performance

Matching Pairs Game on 8051 Microcontroller **Jan '21 - May '21**

- Developed a **real-time** platform for matching pairs game (Concentration game) in **Embedded C** using μVision IDE
- Generated pseudo-randomness for shuffling hidden numbers after each game using 4-bit linear feedback shift register
- Used **UART** to send input via keyboard to the 8051 micro-controller & displayed game state using LCD screen

Matrix Vector Product Unit **Sep '20 - Dec '20**

- Achieved **5.8x** overall speedup over baseline for matrix vector multiplier described in **Aa** (AHIR assembly) language
- Optimized the dot product module by applying **loop-unrolling** for partial products to reduce its latency
- Parallelized the computation of output vector elements by using **2** instantiations of the dot product module

Hyperloop IITB | Technical Team Project **Oct '19 - Jul '20**

- Part of Hyperloop IITB, a multi-disciplinary team of 50 students, involved in designing and building a **functioning** prototype pod for **SpaceX Hyperloop** pod competition
- Reached the final stage of Arizona State University's **Desert Hyperloop** Competition
- Implemented **sensor-fusion algorithm** for location estimation of the pod, utilizing IMUs and fiducial sensors
- Designed a basic model of **navigation system** in **Simulink** for the pod, crucial for safe braking

Teaching & Leadership

Graduate Teaching Assistant **Jul '22 - May '23**

- Responsible for **managing logistics** and helping the professor in ensuring smooth functioning of the courses
- Assisting in evaluation of assignments, take-home exams, project and conducting tutorials for a batch of **90+** students

Department Academic Mentor **Jun '20 - Jun '23**

- Mentored **ten sophomores** on various aspects including their **academic** and **extra-curricular** pursuits at institute
- Acted as a point of contact to provide **guidance** and **support** during the online COVID semesters
- Contributed towards the **DAMP-blog** by writing course reviews, providing students deeper insight into courses

Extracurriculars

◇ Completed **German A1 level** certification offered by **Goethe-Institut**, New Delhi, India.
◇ Learned about option pricing models through **FinSearch** program organized by **Finance Club**, IIT Bombay.
◇ Participated in **Quantum Computing** workshop organized by **IBM** and Institute Technical Council, IIT Bombay.
◇ Conducted beginner English teaching sessions for mess workers of Hostel 7 under **Adult Literacy Program** of NSS.
◇ Created educational videos of secondary level in Hindi to aid students under **Online Learning Initiative** of NSS.
◇ Successfully completed **Cyclothon**, a cycling marathon event organized by Techfest, IIT Bombay.