Prakhar Diwan | **180100083**
Electrical Engineering | **Dual Degree (B.Tech. + M.Tech.)**
Indian Institute of Technology Bombay | **Gender: Male**
Specialization: Microelectronics and VLSI | **DOB: 05/08/2000**

Examination	University	Institute	Year	CPI / %
Graduation	IIT Bombay	IIT Bombay, Mumbai	2023	9.61
Intermediate	CBSE	Campion School, Bhopal	2018	91.0 %
Matriculation	CBSE	Narayana Vidyalayam, Nagpur	2016	97.6 %

SCHOLASTIC ACHIEVEMENTS

- Ranked 4^{th} among **78** Dual Degree students in **Electrical Engineering** Department, IIT Bombay [2022]
- Completed a **Minor** degree from **Computer Science and Engineering** Department, IIT Bombay [2019-22]
- Received **Institute Academic Prize**, awarded to the top two students from each department annually [2021-22]
- Selected for a fully-funded **Mitacs Globalink** research internship at **École Polytechnique de Montréal, Canada** [2022]
- Granted the **DAAD-WISE** Scholarship for research work at **University of Tübingen, Germany** [2021]
- Secured an All India Rank **540** in **JEE-Main** and **99.69** percentile in **JEE-Advanced** among **2.3 Lakh** candidates [2018]

PROFESSIONAL & RESEARCH EXPERIENCE

Digital Design Engineer | **Texas Instruments, Bangalore**
High Speed Data Converters Team [Aug '23 - Present]
- Modeled and analysed a 2-stage **pipelined** ADC with flash offset, flash noise and DAC mismatch errors in **Python**

Heterogeneous ISA Polymorphic Architectures for Energy Efficiency **Masters Thesis**
Guide: Prof. Virendra Singh, Electrical Engineering, IIT Bombay [June '22 - July '23]
- Conducted detailed literature survey on **heterogeneous** and **reconfigurable** multicore architectures
- Analysed PPA impact of ISA and microarchitectural heterogeneity on **SPEC2006** suite using **Gem5** simulator and **McPAT**
- Formulated morphing and migration strategies to leverage heterogeneity in **ISA** (ARM & x86) and **execution semantics**
- Concluded **50%** reduction in Energy Delay Product over state of the art **heterogeneous ISA CMP** for **SPEC2006** suite

Increasing Energy Efficiency of 1D CNN Accelerator **Research Internship**
Guide: Prof. Oliver Bringmann, Computer Science, University of Tübingen [May '21 - Aug '21]
- Implemented power management controller for intra-inference **power gating** of memory macros in **SystemVerilog**
- Achieved **16.25%** reduction in power consumption by analysis of **computational sprinting's** effect on accelerator
- Developed a **Huffman encoder** in **Python** for weights & integrated it within the training framework of neural network
- Designed a **scalable Huffman decoder** for encoded weights stored in memory with effective compression rate of **16.67%**

Software Model for IITB-AI/ML Accelerator **Research Project**
Guide: Prof. Madhav P. Desai, Electrical Engineering, IIT Bombay [May '21 - Oct '21]
- Worked in team to develop software model (in **C**) of hardware accelerator for high-level synthesis (**HLS**) and verification
- Added point-wise unary operators to software model with support across different data types and tensor configurations

Non-invasive extraction of body vitals through video processing | **Epocare, Mumbai** **Software Internship**
Awarded recommendation letter from CEO Deepak Kumar for outstanding contribution [May '20 - July '20]
- Analysed and implemented core image processing algorithms in **MATLAB** for product's medical imaging platform
- Developed a module to measure **SpO2**, **breathing** and **heart** rate based on the **Sophia** method using RGB video of wrist

ACADEMIC PROJECTS

Pipelined IITB-RISC Processor | Processor Design [Jan '21 - May '21]
Guide: Prof. Virendra Singh, Electrical Engineering, IIT Bombay Course Project
- Designed a **16**-bit, **8**-register, **5-stage pipelined RISC** processor based on a custom ISA consisting of **15** instructions
- Described the design using **VHDL**, synthesized it using **Intel Quartus** and verified the design using **ModelSim**
- Implemented data and control **hazard mitigation** unit and **data forwarding** unit for improving performance

Neural Networks on FPGA for Image Classification | VLSI Design Lab [Jan '22 - May '22]
Guide: Prof. Sachin Patkar, Electrical Engineering, IIT Bombay Course Project
- Designed & trained an artificial neural network (ANN) consisting 2 hidden layers for classification task on CIFAR-10 dataset
- Automated generation of a **synthesizable VHDL** model for ANN from its description using **HLS** flow created in **Python**
- Performed simulation-based verification of the design by giving images as inputs through testbench using **ModelSim**

System level Design of PLL & Phase Detectors | High Speed Interconnects [Jan '22 - May '22]
Guide: Prof. Shalabh Gupta, Electrical Engineering, IIT Bombay Course Project
- Implemented & characterized a **Hogge** phase detector for **5 Gbps** pseudo-random bit sequence (data) and **5 GHz** clock
- Designed an integer-**16** PLL using **3-state** phase & frequency detector for generating **2 GHz** clock from **125 MHz** input
- Described the components in **VerilogA** and simulated the circuits using **ANSYS** Electronic Desktop environment

Matrix Vector Product Unit | Algorithmic Design of Digital Systems [Sep '20 - Dec '20]
Guide: Prof. Madhav P. Desai, Electrical Engineering, IIT Bombay Course Project
- Achieved **5.8x** overall speedup over baseline for matrix vector multiplier described in **Aa** (Algorithm assembly) language
- Optimized the dot product module by applying **loop-unrolling** for partial products to reduce its latency
- Parallelized the computation of output vector elements by using **2** instantiations of the dot product module

Matching Pairs Game | Microprocessors Lab [Jan '21 - May '21]
Guide: Prof. Saravanan Vijayakumaran, Electrical Engineering, IIT Bombay Course Project
- Developed a **real-time** platform for matching pairs game (Concentration game) in **Embedded C** using μVision IDE
- Generated pseudo-randomness for shuffling hidden numbers after each game using 4-bit linear feedback shift register
- Used **UART** to send input via keyboard to the 8051 micro-controller & displayed game state using LCD screen

Modeling Target-Receptor Binding in Biosensors | Biosensors & BioMEMS [Jan '22 - May '22]
Guide: Prof. Pradeep Nair, Electrical Engineering, IIT Bombay Course Project
- Implemented **Markov Chain Monte Carlo** model of target-receptor binding in biosensors using **MATLAB**
- Simulated the model, analysed the pre-saturation measurements & made novel comparisons with Langmuir kinetics

Temperature Sensing for Water Geyser | Electronic Design Lab [Jan '21 - May '21]
Guide: Prof. Joseph John, Electrical Engineering, IIT Bombay Course Project
- Designed a **temperature sensing** and **display system**, supporting temperatures from 0°C to 100°C with 0.1°C precision
- Implemented the system with **minimal cost** requirements on a two-layered printed circuit board using **Eagle**
- Interfaced 3 common-anode 7-segment displays with the 3.5 digit A2D converter (ICL 7107) for **cost-effective** display

Mathematical Modelling of Wire-EDM | Insulation Diagnostics Lab, IIT Bombay [Dec '19 - Jan '20]
Guide: Prof. S. V. Kulkarni, Electrical Engineering, IIT Bombay Winter Internship
- Developed a mathematical model of **Wire-Electrical Discharge Machine** using **MATLAB Simulink**
- Simulated and validated the model and its subparts: Servo Motion control, EDM Process model & Pulse generator

POSITIONS OF RESPONSIBILITY

Graduate Teaching Assistant | Courses: Algorithmic Design of Digital Systems & Microprocessors [Jul '22 - May '23]
- Responsible for **managing logistics** and helping the professor in ensuring smooth functioning of the course
- Assisting in evaluation of assignments, take-home exams, project and conducting tutorials for a batch of **90+** students

Department Academic Mentor | Electrical Engineering Department, IIT Bombay [Jun '20 - Jun '23]
*Part of a 40+ member team selected from **100+** aspirants based on rigorous interviews and peer reviews*
- Mentored **ten sophomores** on various aspects including their **academic** and **extra-curricular** pursuits at institute
- Acted as a point of contact to provide **guidance** and **support** during the **online COVID** semesters
- Contributed towards the **DAMP-blog** by writing course reviews, providing students deeper insight into courses

TECHNICAL SKILLS & INTERESTS

HDLs & **Programming**	C++, C, Python, MATLAB, VHDL, Verilog, SystemVerilog, Assembly, Embedded C
Software Packages	Keil μVision, Intel Quartus, ModelSim, GNURadio, NgSpice, ANSYS EDT, AutoCAD
Interests	Computer Architecture, Digital VLSI Design, RTL Design, Machine Learning, HLS

RELEVANT COURSES

VLSI	VLSI Design, CMOS Analog VLSI, Foundation of VLSI CAD, VLSI Design Lab, Testing and Verification of VLSI Circuits, VLSI Technology, High Speed Interconnects
Computer Architecture	Advanced Topics in Computer Architecture, Processor Design, Microprocessors, Computer Architecture for Performance and Security
Computer Science	Logic for CS, Operating Systems, Data Structures and Algorithms, Introduction to ML
Miscellaneous	Data Analysis & Interpretation, Probability & Random Processes

EXTRACURRICULARS

- Completed the **German A1 level** certification offered by **Goethe-Institut**, New Delhi, India [2021]
- Learned about option pricing models through **FinSearch** program organized by **Finance Club** of IIT Bombay [2021]
- Participated in **Quantum Computing** workshop organized by Institute Technical Council of IIT Bombay [2020]
- Conducted beginner English teaching sessions for mess workers of Hostel 7 under **Adult Literacy Program** of NSS [2019]
- Created educational videos of secondary level in Hindi to aid students under **Online Learning Initiative** of NSS [2018]
- Successfully completed **Cyclothon**, a cycling marathon event organized by **Techfest**, IIT Bombay [2018]