

Design And Analysis of StrongARM Comparator

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by

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Declaration

I declare that this written submission reflects my views in my own words and where others' ideas or words have been used, I have properly cited and referenced the original sources. I further declare that I have followed all principles of academic honesty and integrity and that i have not faked or falsified any notion,data,facts,sources in my work. And I know that violation of the above will be caused for disciplinary action by the institute and result in penalties from the sources that not been properly cited or from whose permission was not obtained when required.

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Abstract

A StrongARM Latch configuration became popular because it has zero static power consumption in the circuit. Dynamic comparators are basically used in Analog to digital converters. Dynamic comparators are basically considers parameters like speed, offset voltage, power consumption and noise. Differences between original and modified StrongARM latch topologies will help us to verify the differences in the operation. Comparators are expected to achieve high speed and less power but there is a trade off between power and speed. Since noise's effects are also a major issue, noise analysis is done using the traditional method, which is laborious and time-consuming.

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Chapter 1

Introduction

The StrongARM Latch has a wide applications in analog and mixed signals mainly use a sense Amplifier, Comparators or a latch with high sensitivity. For getting a high speed and low power, there is a need of such comparator which help to satisfies the requirements. Comparator compares the input current or input voltages , Which gives the result like that input which dominates get High and other one sets to low its like digital outputs '0' and '1'.The binary values 1 and 0 are better stored at the output nodes when the inverters are coupled back to back.In scaled CMOS technology, designing a comparator circuit that strikes a balance between power, and speed is crucial.

The basic structure of StrongARM obeserve this circuit in digital Equipment corporation, but its structure was introduced by Toshiba's Kobayashi et al.[[1]].

For Implementing this we are working on 180nm CMOS technology with a VDD of 1.8 V.We will first doing the transient analyses of the operation in various phases, than we look for the power dissipation in the circuit and offset calculation.

As we are using 180nm technology but in papers it was impemented in 28nm technology when V_{th} is low for the transistor which shows the high speed operation of the circuit. but in 180nm the V_{th} is quite high because V_{th} is around 0.5 v that causes the transistor operation slow and causes a delay in the circuit. The StrongARM Latch is operated in three modes:

1. Precharge Mode
2. Amplification Mode

3. Regenerative Mode

As the clock goes high the Circuit is in the precharging mode in this mode all the capacitors are at the output nodes is precharged to V_{DD} and When clock goes low the circuit is in Regenerative mode the output of one node reached to V_{DD} and other reached to Gnd.

Dynamic Comparators are used to attain high speed with low power consumption.Dynamic comparators have zero static power , So our main focus is to improve the speed of operation without affecting power.

And In Chapter 3 we will see the various operations in detailed manner. we will see why strong arm latch configuration have zero static power.

Chapter 2

Literature Survey

We begin our study by studying about comparators and its working depend on simple operation that if $V_{in+} > V_{in-}$ than it provides high output and when $V_{in+} < V_{in-}$ then it provides low output.

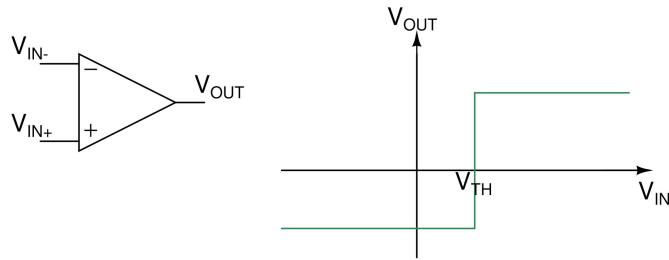


Figure 2.1: Basic Comparator Operation

We are studying the advantages of StrongARM Latch [1] configuration and how dynamic comparators are become popular.

Dyanamic comparator are known for attaining high speed and less power consumption. And we are studying StrongARM Latch [1] comparator design and its operations. it became popular because it has 3 main advantages :

1. Zero Static power consumption.
2. it produces rail to rail outputs directly.
3. its input reffered offset is arise from the input differential pair due to the mismatches in the input transistor.

Our main aim is to increase the speed of comparator. for making it high speed comparator we have to reduce threshold voltage V_{th} of the transistors . so for reducing the threshold voltage

we have two options, first is to use that CMOS technology which have less V_{th} but we are using 180nm technology in which V_{th} is around 0.5V and other option is to use transistor with Body Biasing method of transistor. But reducing V_{th} cause leakage current increases that also lead to poor the operation, So therse is a tradeoff between High speed and good operation of comparator. The StrongARM Latch is operated in three modes:

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Dynamic Comparators are used to attain high speed with low power consumption. Unlike static operating amplifiers, a standard single tail comparator is needed to increase speed and decrease power usage. The back-to-back inverter circuit is a component of the pre-amplifier circuit.

we were rigorously analyse the working of StongARM Comparator in further chapters and we will study the 4 phase operation of strongARM latch, power consumption , Input reffered offset calculations and current calculations in Amplification Mode after this we will see a example of strongARM Latch.

Chapter 3

The StrongARM Latch Comparator

Comparators are utilized extensively and have a wide range of uses in analog circuits. The StrongARM Latch configuration consist of Differential pair circuit with Switching transistor to see the operation in different modes. We will starts our study from the operations.

3.1 Operations

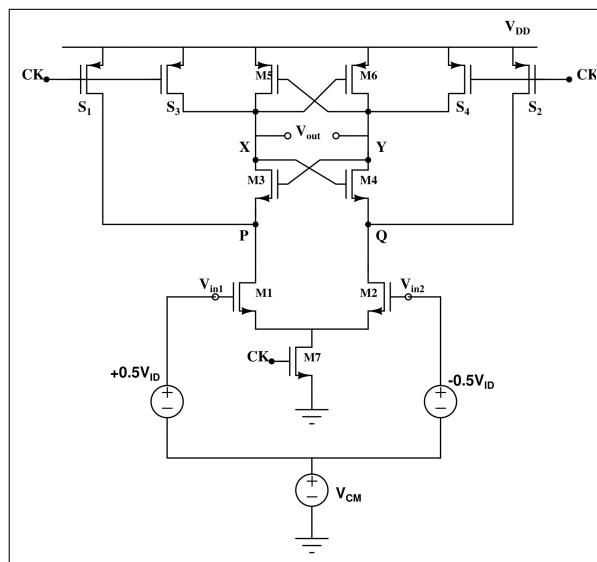


Figure 3.1: Modified StrongARM Latch [1].

The latch that is shown in Figure 3.1 is consist of M1–M2 differtial pair which is clocked and we have two cross coupled pairs M3–M4 and M5–M6 and also we have 4 switches that we called precharge switches S₁–S₄. With respect to the polarity of inputs the circuit output gives rail to rail outputs at node X and Y. Now we will study the operations in 4 phases.

3.1.1 Reset Phase

In this First Phase operation of StrongARM Latch when Clock is set to low than 4 Pmos switches S1–S4 are activated and precharged the output capacitor to V_{DD} . and M7 is off and which results into M1–M2 becomes off. And the circuit reduces to circuit shown in figure 3.2.

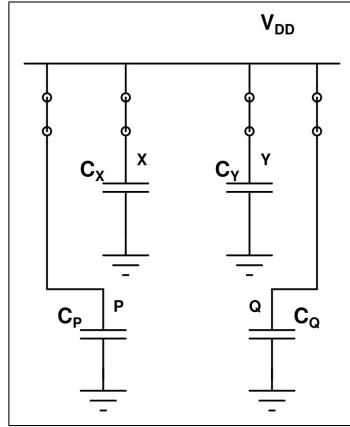


Figure 3.2: Precharge Mode [1].

3.1.2 Amplification Mode

When Clk gets high , S1–S4 goes Off and M7 becomes ON , M1–M2 is input defferential pair which able to drawing a current from difference inputs. And initially C_P, C_Q, C_X and C_Y are charged to V_{DD} that will result to M3–M6 transistor remains Off.

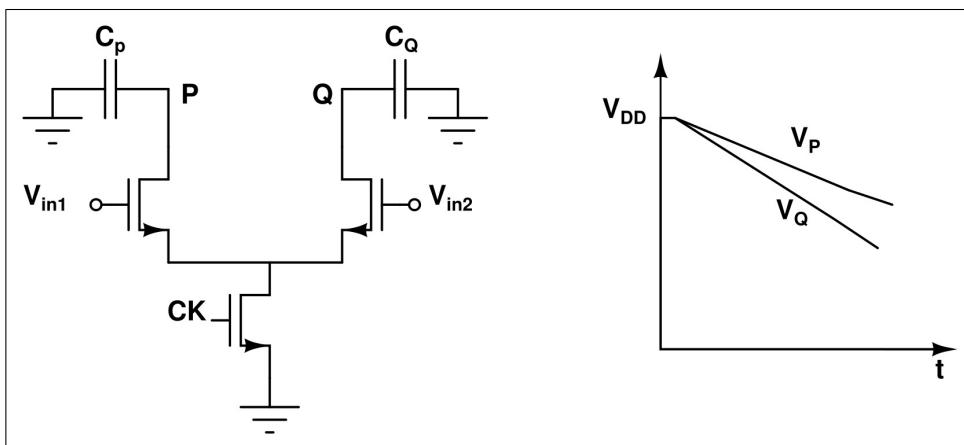


Figure 3.3: Amplification mode [1].

The Current that flows in M1 and M2 is directly propotional to $|V_{IN1} - V_{IN2}|$ and also this current flows in the output capacitance that are connected to node P and Q which result

$|V_P - V_Q|$ to increase which gives amplification or voltage gain. Now calculate the Voltage gain in the amplification mode.

As we Know that, $I = C \frac{dV_c}{dt}$

$$\int_0^{T_s} I.dt = \int_{V_{DD}}^{V_{DD}-V_{th}} C.dV_C \quad (3.1)$$

$$T_s = \frac{C_{p,q} \cdot V_{th}}{\frac{1}{2} I_o} \quad (3.2)$$

Where I_o is the tail current that flows into the M7, V_{th} is the threshold voltage of M3 transistor, $C_{p,q}$ is the equivalent capacitance at nodes P and Q, T_s is the time for Amplification.

$$|V_p - V_q| = g_{m1,2} \frac{|V_{in1} - V_{in2}|}{C_{p,q}} \cdot T_s \quad (3.3)$$

$$A_v = \frac{g_{m1,2} \cdot V_{th}}{\frac{1}{2} I_o} \quad (3.4)$$

3.1.3 Phase 3

As we know from the previous discussion that C_P and C_Q starts discharging, When V_P and V_Q discharges and reduces up to $V_{DD} - V_{th}$ than our circuit goes into third phase of operation.

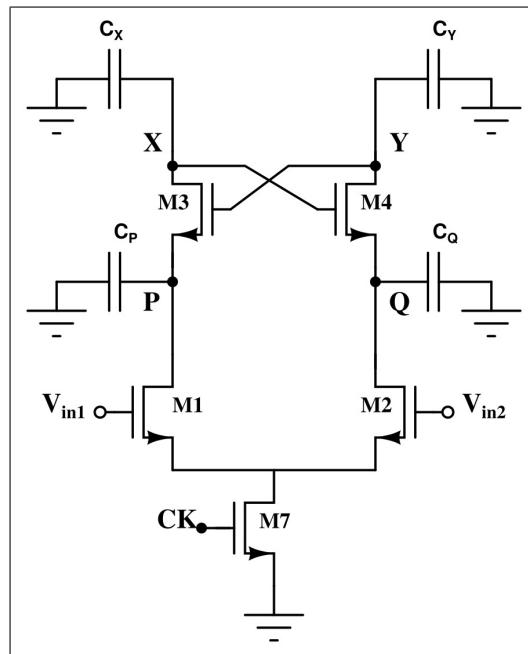


Figure 3.4: 3rd Phase operation [1].

In this phase now current will flow also from cross coupled pair M3–M4. Initially C_x and C_y are charged to V_{DD} , so Still cross coupled pair M5–M6 will be off till the capacitor at C_x and C_y are discharged to $V_{DD} - V_{th,p}$.

3.1.4 Regeneration Phase

As C_x and C_y starts discharging that means nodes V_x and V_y starts reducing when it become $V_{DD} - V_{th,p}$ than Pmos Cross coupled pair M5–M6 turn ON.

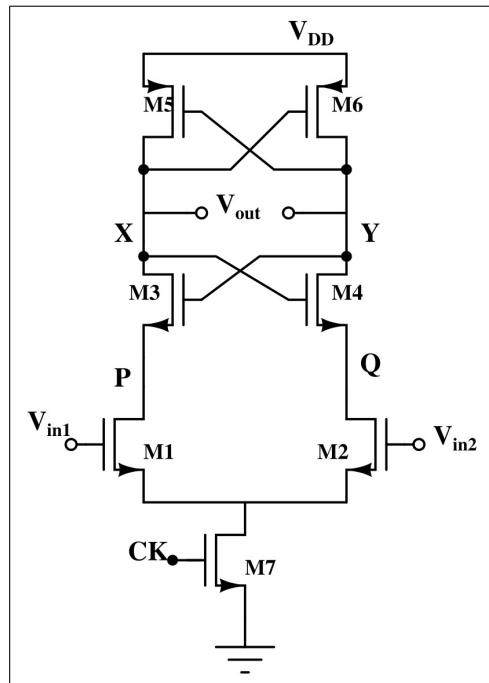


Figure 3.5: Regeneration Phase [1].

And due to positive feedback around M5–M6 will lead to one output back to V_{DD} and other fall towards Zero.

3.1.5 Example

let understand the operation with an Example ,

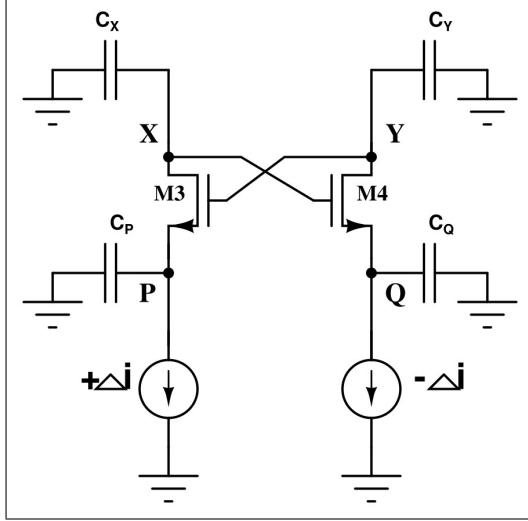


Figure 3.6: Example for Understanding Operations [1].

We have replaced the M1–M2 transistor with ideal current source where on one side current dominates by $+Δi$ and other side current will degraded by $-Δi$ So Capacitor Cp and Cx will be discharged at a faster rate than Cq and Cy. so the summing currents at the 4 nodes:

$$-C_X \frac{dV_X}{dt} = g_{m3}(V_Y - V_P) \quad (3.5)$$

$$-C_Y \frac{dV_Y}{dt} = g_{m4}(V_X - V_Q) \quad (3.6)$$

$$-C_P \frac{dV_P}{dt} = C_X \frac{dV_X}{dt} + Δi \quad (3.7)$$

$$-C_Q \frac{dV_Q}{dt} = C_Y \frac{dV_Y}{dt} - Δi \quad (3.8)$$

After subtracting the equation 3.6 from Equation 3.5 We get

$$-C_{X,Y} \frac{d(V_X - V_Y)}{dt} = g_{m3,4}(-V_X + V_Y - V_P + V_Q) \quad (3.9)$$

Now by intigration of equation 3.7 and 3.8 and joining the results

$$C_{P,Q}(V_Q - V_P) = C_{X,Y}(V_X - V_Y) + 2Δi \quad (3.10)$$

Now by putting the value of equation 3.10 in equation 3.9 then we get

$$C_{X,Y} \frac{d(V_X - V_Y)}{dt} - g_{m3,4}(1 - \frac{C_{X,Y}}{C_{P,Q}})(V_X - V_Y) = -2g_{m3,4} \frac{Δi}{C_{P,Q}} t \quad (3.11)$$

$τ_{rg}$ is the regeneration time constant

$$τ_{rg} = \frac{C_{X,Y}}{g_{m3,4}(1 - \frac{C_{X,Y}}{C_{P,Q}})} \quad (3.12)$$

So in third phase also we will see a small regeneration . And in 4th phase in regeneration in which Cx is discharging at faster rate than Cy so Vx will early drop to $V_{DD} - V_{th,p}$ than M6 will be activated and charged Cy to V_{DD} which lead to that Vy will goes to V_{DD} and if Vy is V_{DD} than M5 will never ON then Cx will discharged completely after some time and reaches to zero . so there is always question in mind of readers that why we are using so many transistor in just simple operation, And why we are using StrongARM Latch configuration.

3.1.6 Transient Plot

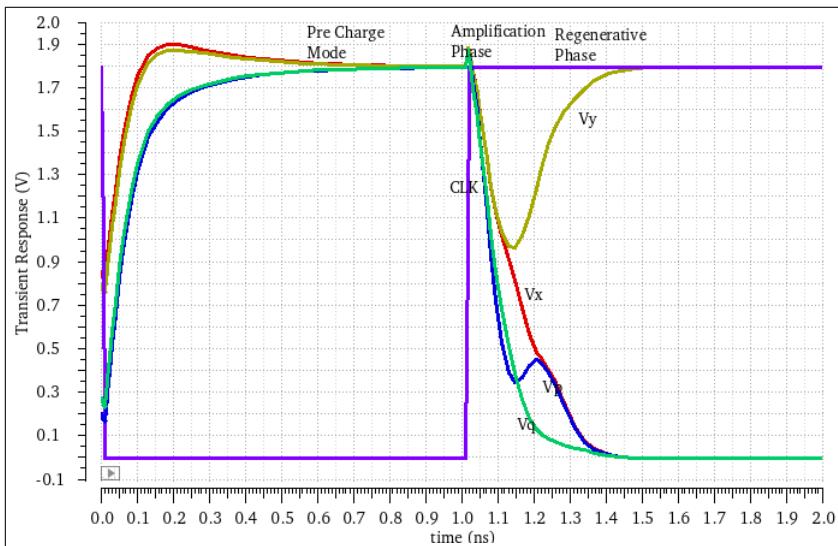


Figure 3.7: Trasient Response of Strong ARM Latch

3.2 Why StrongARM Latch ?

After the phase 4 operation we saw that there dc path cutt-off by M3 – M4 transistor. So, this leads to no static power consumption in the circuit. now let us remove the transistor M3 and M4 then the circuit reduced is shown in figure.

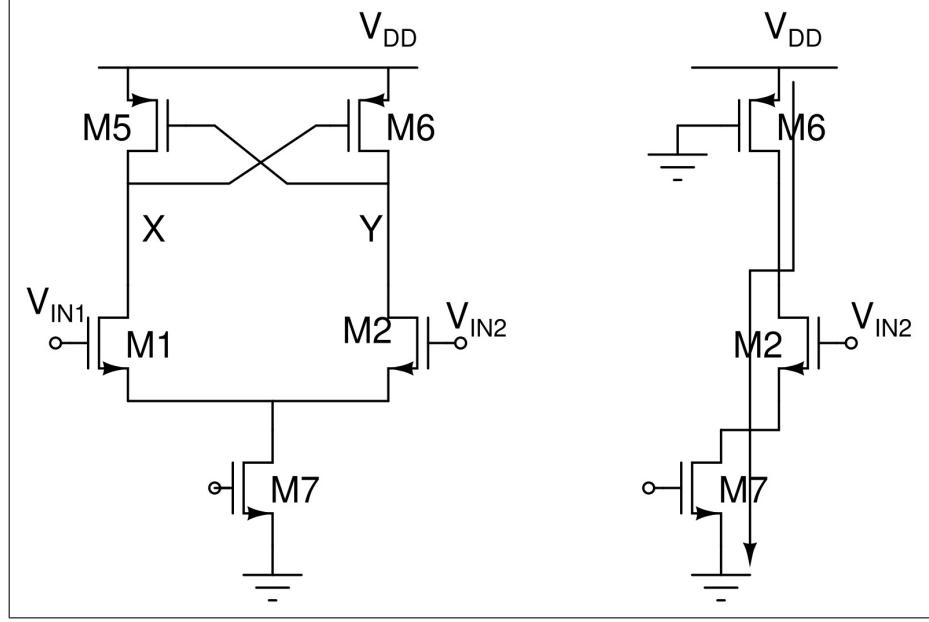


Figure 3.8: Without Nmos cross coupled pair [1].

So we will conclude that that after removing the Nmos cross coupled pair from the circuit it will not not cutoff the DC path than there will not be Static power zero.

3.3 Offset

To function as either a comparator or a sense amplifier, the StrongARM latch needs to attain an appropriately low input-referred offset voltage. During the precharge action M3–M6 are Off iniatially . The mismatches between M3 and M4 in a typical design are split by roughly a factor A_v for input reffered ,those that vary by roughly a factor of ten between M5 and M6. As a result, M1 and M2 start to dominate to input reffered offset. One can produce asymmetry by making $C_P C_Q$,since the amplification mode provides voltage gain through the flow of charge from C_P and C_Q and thus negate the offset of the circuit.

$$V_P = V_{DD} - \frac{g_{m1}(V_{IN1} - V_{IN2})}{2C_P}t - \frac{I_{CM}}{C_P}t \quad (3.13)$$

$$V_Q = V_{DD} + \frac{g_{m2}(V_{IN1} - V_{IN2})}{2C_Q}t - \frac{I_{CM}}{C_Q}t \quad (3.14)$$

Subtracting the equation 3.14 from 3.13 it gives,

$$V_P - V_Q = -\frac{g_{m1,2}}{2} \cdot \frac{C_P + C_Q}{C_P C_Q} (V_{in1} - V_{in2})t + \frac{C_P - C_Q}{C_P C_Q} I_{CM}t \quad (3.15)$$

During Amplification,

$$Offset = \frac{C_P - C_Q}{C_P C_Q} I_{CM} t \quad (3.16)$$

3.4 Power Consumption

The power consumption of the circuit in the signal path is provided by:

$$Power\ Consumption = 2f_{clk}C_PV_{DD}^2 + f_{clk}C_XV_{DD}^2[2] \quad (3.17)$$

As we can say that there is no static Power consumption in StrongARM Latch So we plot the power consumption in one cycle of operation.

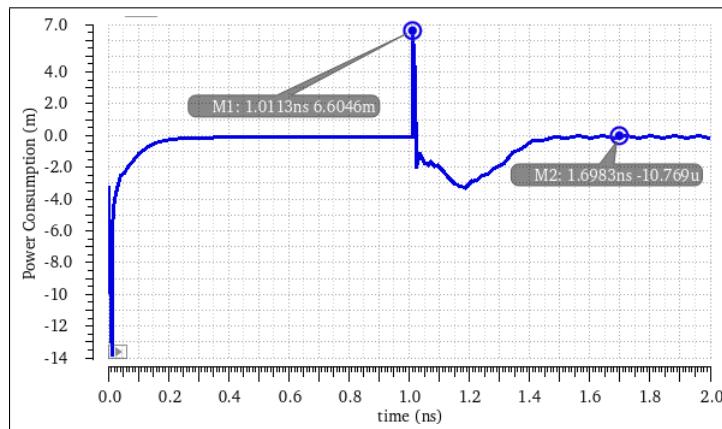


Figure 3.9: Power consumption Plot

Chapter 4

Comparison

As we have scale down the technology we will able to see the difference in the operation of Comparators as the length of the mosfet decreases the threshold voltage also decreases . If Threshold decreases than speed of operation of comparator increases.

	[3]	[3]	[3]
Technology	65nm	180nm	180nm
Supply Voltage	1.2v	1.2v	1.8v
Area	$125\mu m^2$	$392\mu m^2$	$490\mu m^2$
Power Consumption	-	-	6.606mW

Table 4.1: Comparison table for operation in different technology

Chapter 5

Conclusion and Future Work

5.1 Conclusion

The Strong Arm Latch is the main block in Dynamic comparator. We are focusing on how to speed up the operation of Strong ARM latch and also with less power consumption. Designing the comparator with all the specifications is a challenging task because there is a trade-off between speed and the performance.

5.2 Future work

We will study the operations of StrongArm latch but still we need to study in deep the delay of StrongARM Latch and also want to see that due to mismatches what it affect on input referred offset and also see the effect of input referred noise in the StrongARM latch configuration. In a recent paper , it is discussed how to reduce noise in the circuit.

Acknowledgement

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