

Offset cancellation techniques in double tail comparator

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by

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2024

Declaration

I declare that this written submission reflects my views in my own words and where others' ideas or words have been used, I have properly cited and referenced the original sources. I further declare that I have followed all principles of academic honesty and integrity and that i have not faked or falsified any notion,data,facts,sources in my work. And I know that violation of the above will be caused for disciplinary action by the institute and result in penalties from the sources that not been properly cited or from whose permission was not obtained when required.

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Abstract

The idea is to reduce the offset voltage of the latched double tail comparator. Ideally comparators have zero offset voltage but due to mismatch in input transistors which creates offset error and leads to non ideality. Earlier pre-amplifiers are used to reduce the input referred offset but the problem is that it needs high power consumption. so some new architectures introduced to remove the offset error, furthermore there is need of design where the overdrive voltage of the input transistor can be independent of the common mode input. Differences between conventional and modified comparator topologies will help us to verify the differences in the operation.

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Chapter 1

Introduction

Comparators having low power, low offset and have high speed are always in demand. comparator is the main block in the high sensing circuits like analog to digital converters (ADC). Latch type sense amplifiers are very effective comparators. they are expected to achieve high speed decision due to the positive feedback. due to the technology scaling of CMOS transistor, lead to less power consumption and less area.

But the main issue with the comparators have high offset more than 10 mV at 1σ due to the mismatch in the transistors which leads to non ideality. Therefore, many researches are going on for offset cancellation techniques for having a low offset comparator. in many conventional designs pre-amplifiers are used to reduce the input referred offset. using pre-amplifiers are lead to high power consumption because for reducing offset there is a need of wide bandwidth amplifiers. Hence, there is a strong requirement of the technique for reducing the offset without amplifiers. In many literature load capacitances of the comparators are digitally controlled for the reduction of offset voltage.

Dynamic offset cancellation techniques requires negligible static current in latched comparators. And the expectation is that these techniques are tolerant to PVT variations. And in this study first try to understand the core concept of conventional comparator and learn how to find the offset. further will look into the modifications for the offset reduction.

Chapter 2

Literature Survey

We begin our study by studying about comparators and its working depend on simple operation that ideally if $V_{in} > 0$ than it provides high output and when $V_{in} < 0$ then it provides low output as shown in figure 2.1. But in practical cases there is a presence of offset error due to the mismatch in the transistor. Input referred offset is the input at which transition from one logic level to the other logic level. And circuit noise also change the output from one logic to other. As shown in figure 2.1 that at $V_{in} = 2\text{mV}$ the probability of output getting high or low is equal. Hence, the input offset of the comparator is 2 mV.

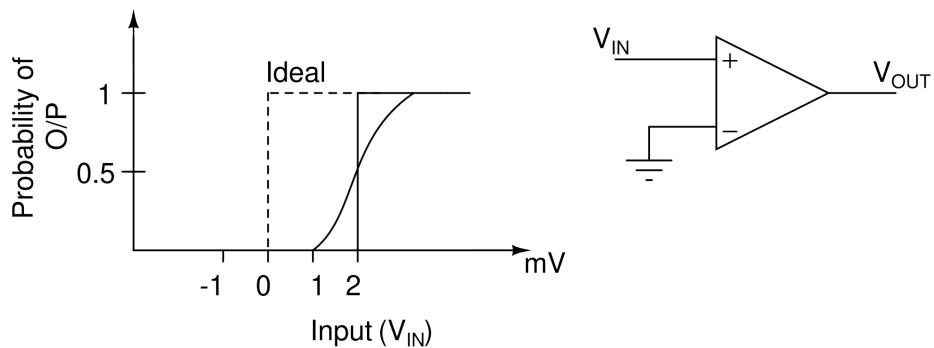


Figure 2.1: Probability of getting high output for the varying input [3]

We are studying the architecture of double tail comparators [2] configuration and how dynamic comparators are becoming popular.

Dynamic comparators are known for attaining high speed and less power consumption. And double tail comparator comprises of two stages, one is pre-amplifier, other is latch stage.

1. The offset arises due to the second stage is reduced by the gain of the pre-amplifier

2. its input referred offset is arise from the input differential pair due to the mismatches in the input transistor.

Aim is to reduce the input referred offset of the comparator for that offset cancellation techniques are used in the pre-amplifier circuit in this study, capacitors are used to cancel the mismatches arises in the input differential pair and also reduce the effect of common mode input to the offset and it also increases the speed of comparator. For designing we are using 180nm technology node and realises the input offset of conventional comparator and the modified comparator. And also see the effect of input common mode variations in the offset. For the operation part of Double tail comparator it is operated in two modes:

1. Reset Mode
2. Regenerative Mode

As the clock goes low the circuit is in the reset mode in this mode the output nodes is reset to Gnd and When clock goes High the circuit is in Regenerative mode the output of one node reached to V_{DD} and other reached to Gnd.

Chapter 3

Offset cancellation techniques in double tail comparators

Dynamic comparators are widely used for high speed operation and less power consumption. Double tail comparators are known for high precision and produces rail to rail outputs. But due to the mismatch in the transistors it have high input referred offset voltage. Now, first look at the conventional double tail comparator which have two phases of operation, reset phase and the regenerative phase.

3.1 Circuit Description

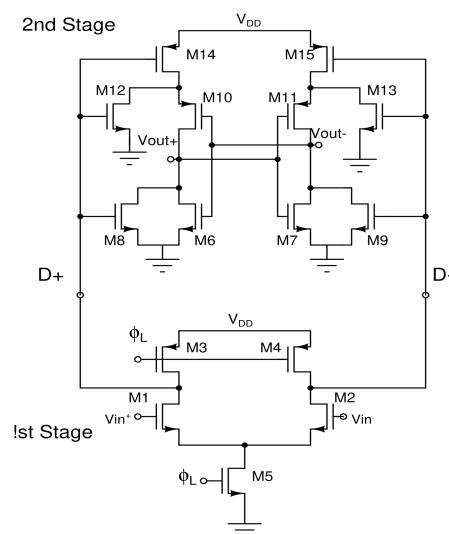


Figure 3.1: Conventional double tail latched comparator [1].

The comparator shown in the above figure is consist of two stages, first stage is a pre-amplifier circuit used for amplification and offset cancellation, second stage is the latch configuration. As shown in Figure 3.1 first stage pre-amplifier is consist of M1–M2 input differential pair which is connected to M3,M4 and M5 which is clocked and the outputs of the first stage D+ and D- is input to the second stage. In the second stage M6,M7,M10 and M11 are cross coupled inverters.

3.2 Operations

3.2.1 Reset Phase

During first Phase operation of double tail comparators as shown in figure 3.1 when $\text{clk}(\phi_L) \rightarrow \text{Low}$, then transistor M3-M4 switch ON and charge the nodes D+ and D- to V_{DD} . And the transistor M8-M9 pulls the output nodes V_{out+} and V_{out-} nodes to the gnd.

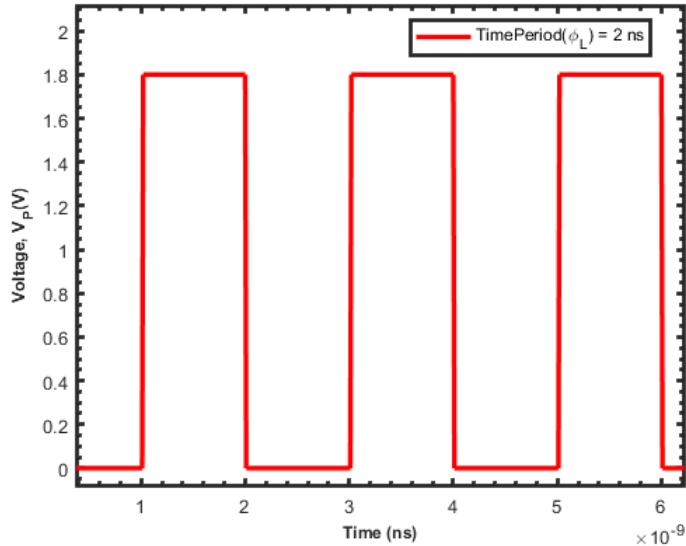


Figure 3.2: Input clock(ϕ_L).

the input clock shown in figure 3.2 have a time period of 2 ns and conversion frequency of 500 MHz

3.2.2 Regenerative Phase

When Clk → high, M3-M4 transistor switched off and the nodes D+ and D- starts discharging and the transistor M8-M9 and M12-M13 gets off while the transistor M14-M15 turns ON and

the latch operation taken place and due to positive feedback around the cross coupled inverters will lead to one output back to V_{DD} and other fall towards Zero.

3.2.3 Example

Now, lets understand it with an example, suppose D_- is discharging at a faster rate than D_+ . Than the transistor M15 will switch on faster than M14 so due to positive feedback it will lead to V_{out-} will lead to V_{DD} and V_{out+} will fall to GND.

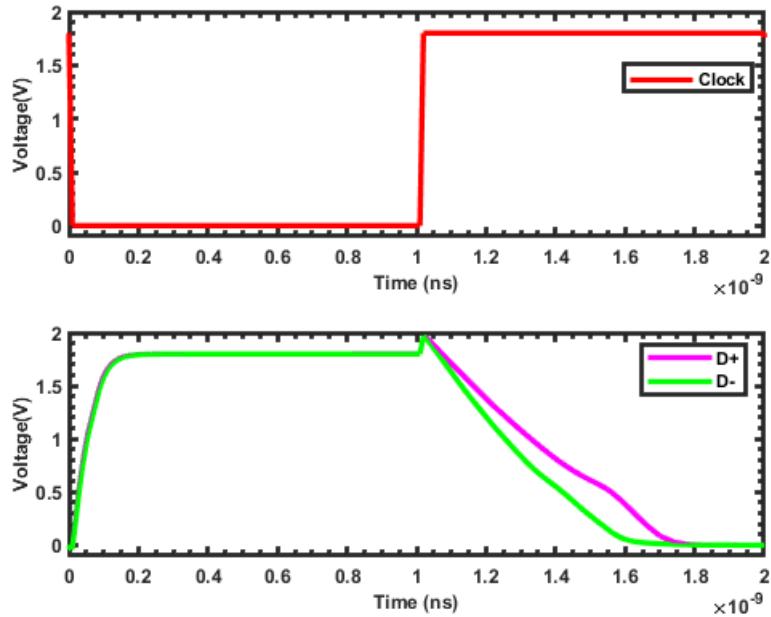


Figure 3.3: Charging and discharging of D_+ and D_-

As from the figure 3.3 transient plot, it is clear to say when ϕ_L is high than D_- is discharging at a faster rate than D_+ for the ramp differential input. And from the figure 3.4 it is observed that as the differential input varies than $V_{out+} - V_{out-}$ changes with the time. When V_{in+} is slightly greater than V_{in-} than D_+ node discharge at a faster rate and V_{out+} reaches to V_{DD} and V_{out-} reaches to GND. Similarly for V_{in-} is slightly greater than V_{in+} than D_- node discharge at a faster rate and V_{out-} reaches to V_{DD} and V_{out+} reaches to GND.

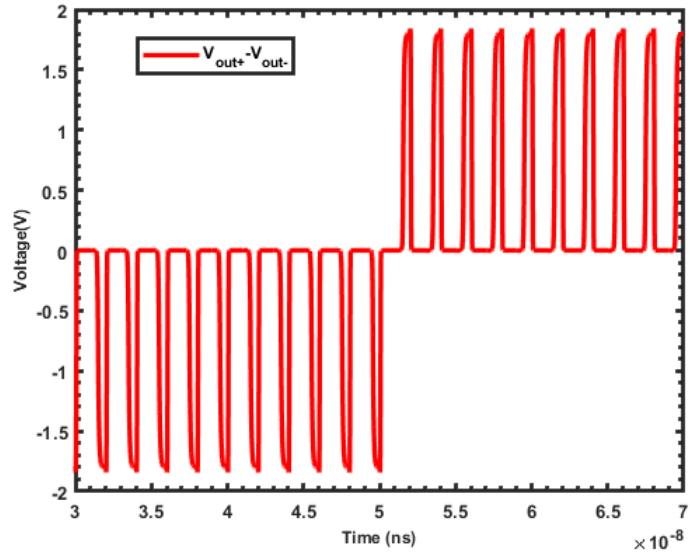


Figure 3.4: $V_{out+} - V_{out-}$ plot vs time

3.3 Offset in conventional model

The conventional comparator has two stages and each stage contribute to the offset error and in 1st stage the offset error arises because of the mismatches in the input transistor M1 and M2. the offset error of the 2nd stage is less because of the gain of the first stage. so offset error arises because of the input transistor dominates.

To find the offset in conventional comparator a monte carlo simulation for 100 runs with both process and mismatch variations. For analysis input common mode voltage V_{CM} is 700mV and differential ramp input is varying from -15mV to 15mV. The output result is shown in figure 3.5

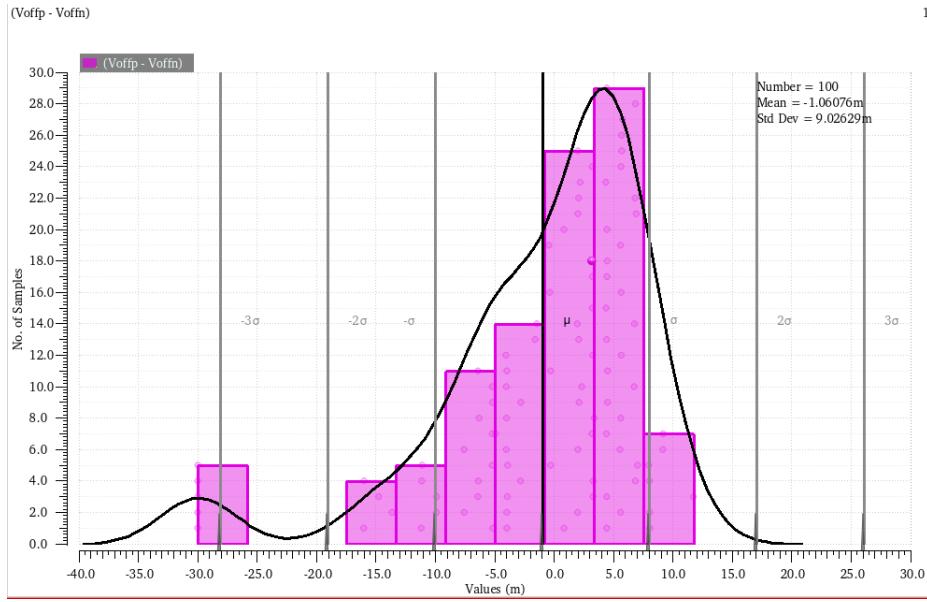


Figure 3.5: Monte carlo simulation for $V_{off}(1\sigma)$

From the above plot, $V_{off}(1\sigma) = 9.062$ mV.

3.4 Modified Comparator

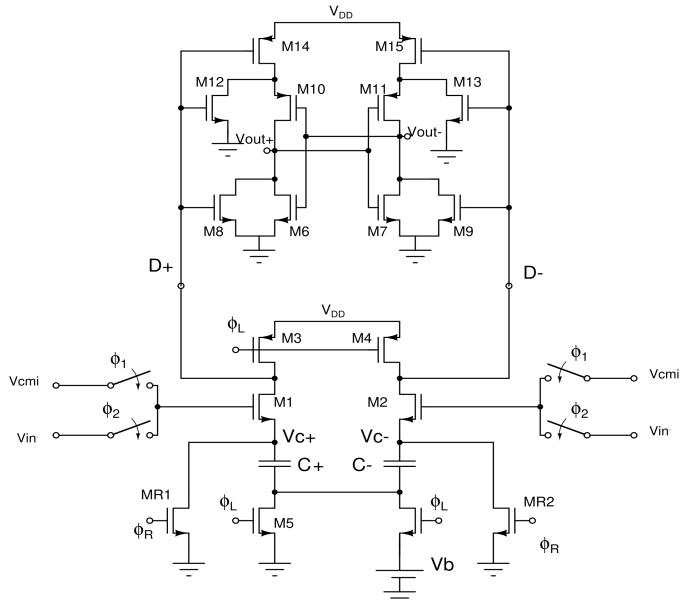


Figure 3.6: Modified double tail latched comparator [1].

Figure 3.6 is the modified comparator which contain two capacitors C_+ and C_- used for cancelling the effect of mismatch of input transistors. And as shown in circuit diagram there are

4 clocks $\phi_1, \phi_2, \phi_L, \phi_R$. Where ϕ_1 and ϕ_2 are the two clocks used for input to the M1-M2 transistor, during ϕ_1 only V_{CM} is applied on M1-M2 and for ϕ_2 , $V_{CM} + V_{diff}$ is applied to gate of M1-M2. ϕ_R is input to the transistor MR1-MR2 which is used to discharged the capacitor.

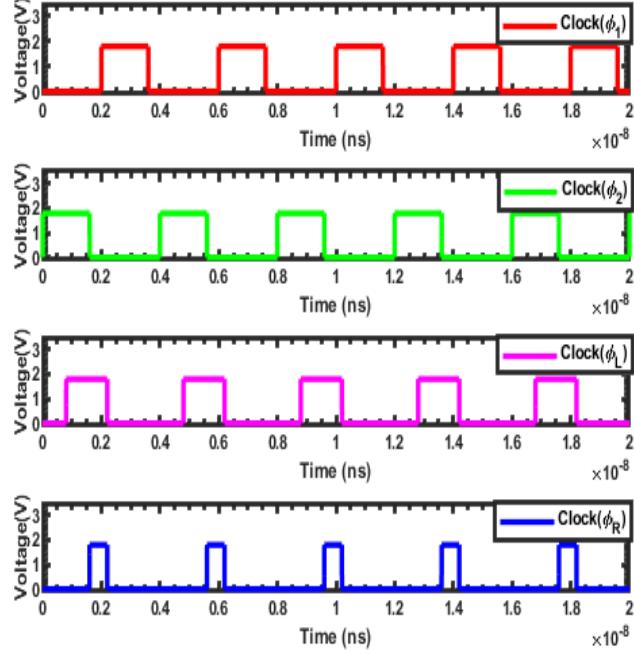


Figure 3.7: Clocks ϕ_1, ϕ_2, ϕ_3 and ϕ_4

Above plot shows the clocks ϕ_1, ϕ_2, ϕ_3 and ϕ_4 . For the analysis, During phase (ϕ_1), V_{CM} is the input to M1 and M2. Bottom plate of capacitor C+ and C- connected to the V_b . so the capacitor charge up to,

$$V_{C+} - V_b = V_{CM} - V_{th1} - V_b \quad (3.1)$$

$$V_{C-} - V_b = V_{CM} - V_{th2} - V_b \quad (3.2)$$

During phase (ϕ_2), $V_{in+} = V_{CM} + \Delta V_{in}$, $V_{in-} = V_{CM} - \Delta V_{in}$ and Bottom plate of capacitor C+ and C- connected to the GND.

$$V_{GS1} - V_{th1} = [(V_{CM} + \Delta V_{in}) - (V_{CM} - V_{th1} - V_b)] - V_{th1} \quad (3.3)$$

$$V_{GS1} - V_{th1} = \Delta V_{in} + V_b \quad (3.4)$$

$$V_{GS2} - V_{th2} = [(V_{CM} + \Delta V_{in}) - (V_{CM} - V_{th2} - V_b)] - V_{th2} \quad (3.5)$$

$$V_{GS2} - V_{th2} = \Delta V_{in} + V_b \quad (3.6)$$

So from the above analysis the threshold voltage mismatch of input transistor can be cancelled. V_b is the bias voltage connected to the bottom plate of the capacitor during phase ϕ_1 .

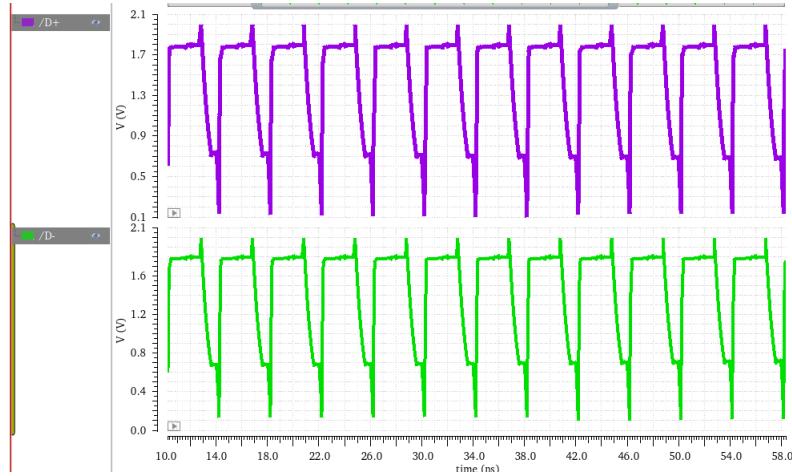


Figure 3.8: D+ and D- nodes charging and discharging

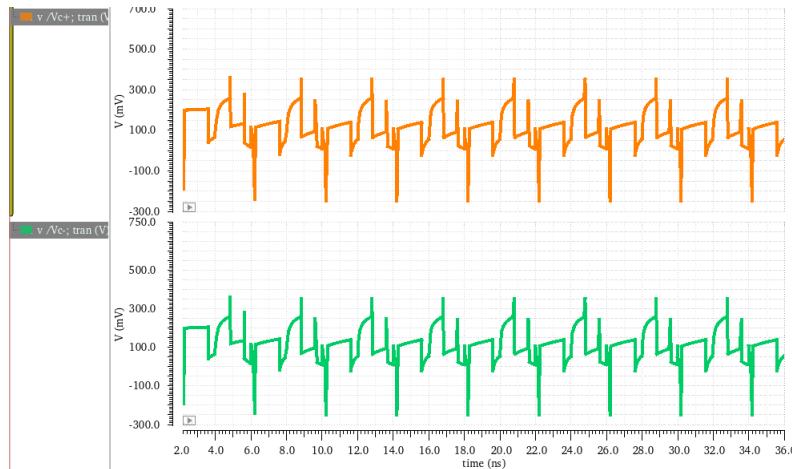


Figure 3.9: Capacitors charging and discharging

3.5 Offset in modified comparator model

To find the offset in modified comparator a monte carlo simulation for 100 runs with both process and mismatch variations. For analysis input common mode voltage VCM is 700mV and differential ramp input is varying from -15mV to 15mV. The output result is shown in figure 3.10

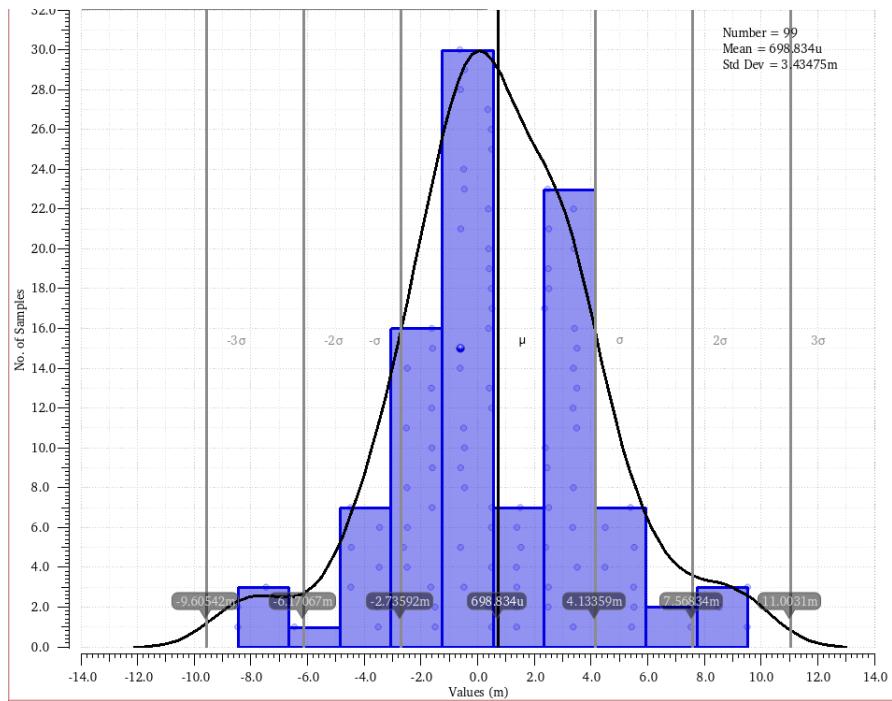


Figure 3.10: Monte carlo simulation for $V_{off}(1\sigma)$

From the above plot, $V_{off}(1\sigma) = 3.4375$ mV.

Now with the variation of bias voltage V_b there is a change in the offset which is shown in the figure 3.11

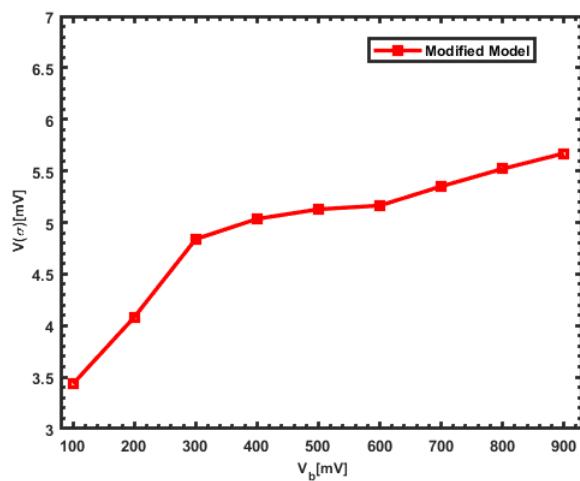


Figure 3.11: variation of $V_{off}(1\sigma)$ for different bias voltage V_b

From the result, at 100 mv bias voltage the offset V_{off} can be minimized.

Chapter 4

Comparison

As in the previous chapter it is analysed that offset is reduced in the modified model. In conventional comparator the input referred offset error is around 10 mV and in modified model the offset error is less around 2 mV. Comparison is shown below in figure 4.1 between the conventional model and modified model $V_{off}(1\sigma)$ with the variation of input common-mode (V_{CM}).

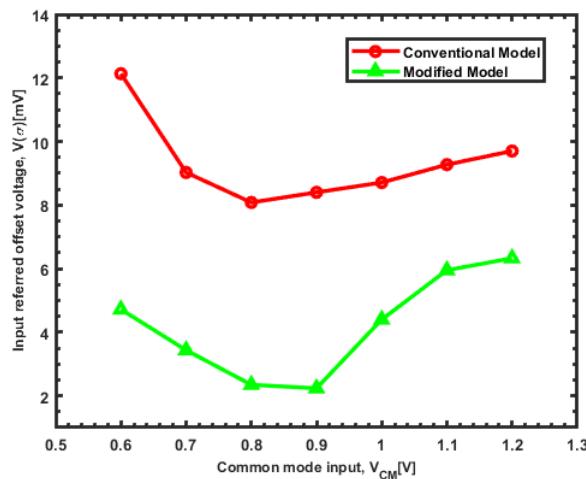


Figure 4.1: variation of $V_{off}(1\sigma)$ for different input common mode (V_{CM})

Chapter 5

Conclusion and Future Work

5.1 Conclusion

The high speed dynamic comparators are affected by the input referred offset. the modified model have negligible static power consumption. And offset error in the conventional comparator is 9.062 mV while in modified comparator the offset error is reduced to 3.437 mV. Also observed the offset error changes with the input common mode V_{CM} in the conventional design but there is less effect of V_{CM} in the offset error.

5.2 Future work

From this thesis, we gets a motivation for understanding the offset reduction techniques in dynamic comparator and in future kickback noise analysis of the comparator and how to reduce the effect of noise contribution in the offset.

Acknowledgement

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