EE532: Device Simulation Lab

Experiment No. 3

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Experiment Name: Design and analysis of 1.5 μm, 500 nm, 180 nm channel length bulk MOSFET using Sentaurus Structure Editor.

This Experiment involves the design and simulation of MOSFET in sentauraus TCAD and further we have to analyse it various results. For design and simulation we are using SDE (command line mode), Sdevice in the SWB environment. First, we created the structure of MOSFET and set the doping of substrate, set the contacts at metal, source, drain and body side, Meshing at the substrate oxide interface and build the mesh.

The Design Parameters of MOSFET is mentioned in the below table:

Table 1: **Design Parameters for MOSFET**

Parameter	**Value\Type**
Substrate	Silicon
P-type Dopant with concerntration	Boron($1 \times 10^{15} - 1 \times 10^{17}$)
N-type Dopant with concerntration	Phosphhorous($1 \times 10^{17} - 1 \times 10^{20}$)
Source and Drain Doping	Analytical profile placement
Source and Drain Area	150 nm $\times$ 150 nm
Oxide Thickness	20 nm
Gate Metal	Aluminum
Metal Thickness	40 nm
Metal WorkFunction	5 eV

1 Physics Models

The Physics Models use for simulation are mentioned in below table:

Table 2: **Illustration/List of the physical models of MOSFET**

Parameters	**Value/Type**
Band gap and Bandgap narrowing	Effective intrinsic density (no band gap narrowing)
Mobility models	Mobility (Doping Dependance HighFieldSaturation)
Temperature (K)	300
Traps	FixedCharge

2 Device Structure and Meshing of MOSFET

For 1.5μm Channel length:

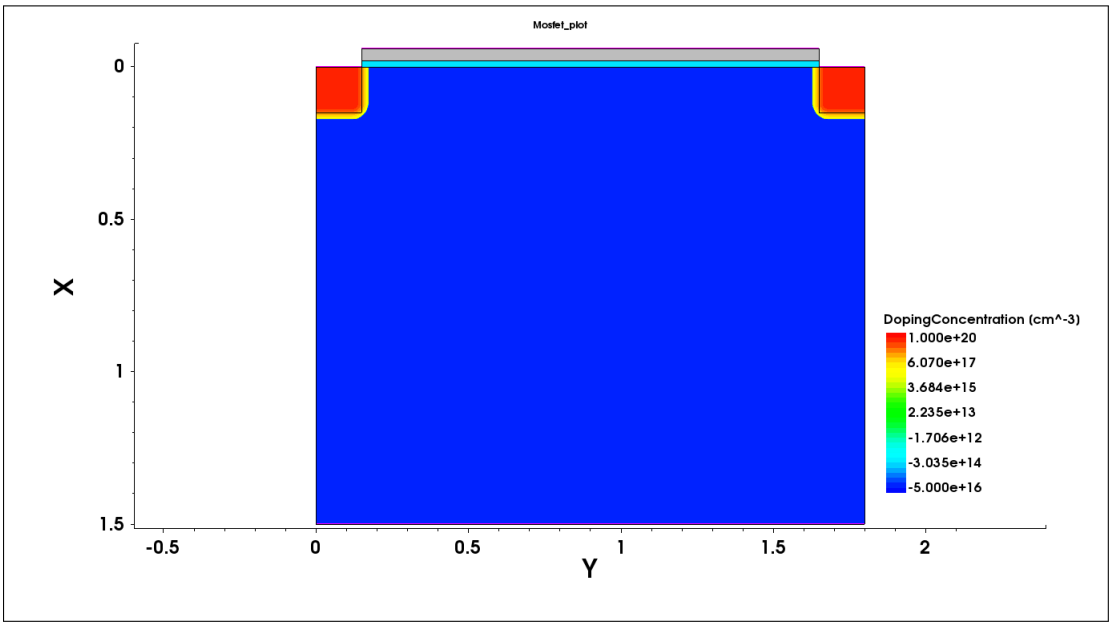

Figure 1: Simulated Structure of MOSFET Device with 1.5μm Channel length

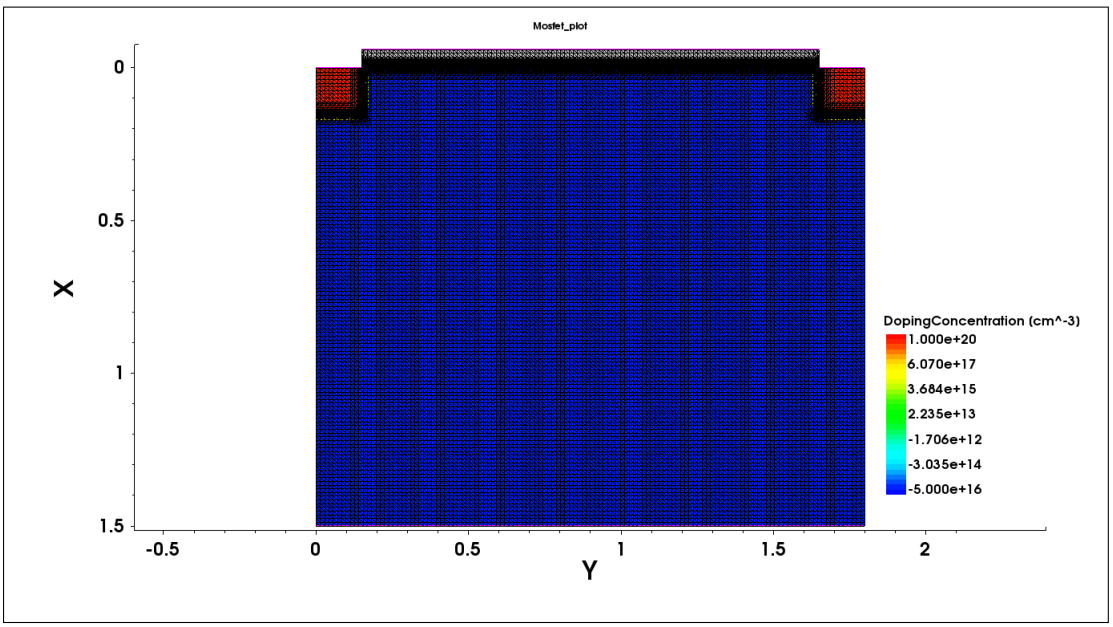

Figure 2: Simulated Structure of MOSFET Device with 1.5μm Channel length with Meshing

For 500 nm Channel length:

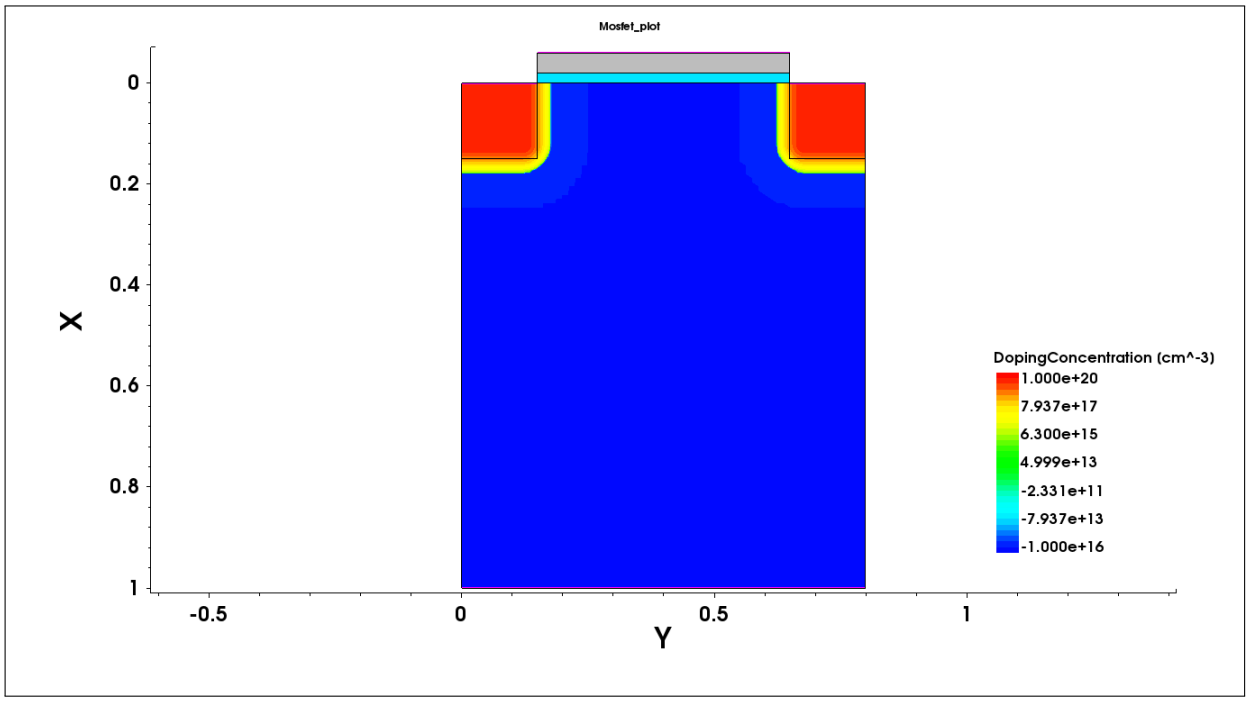

Figure 3: Simulated Structure of MOSFET Device with 500 nm Channel length

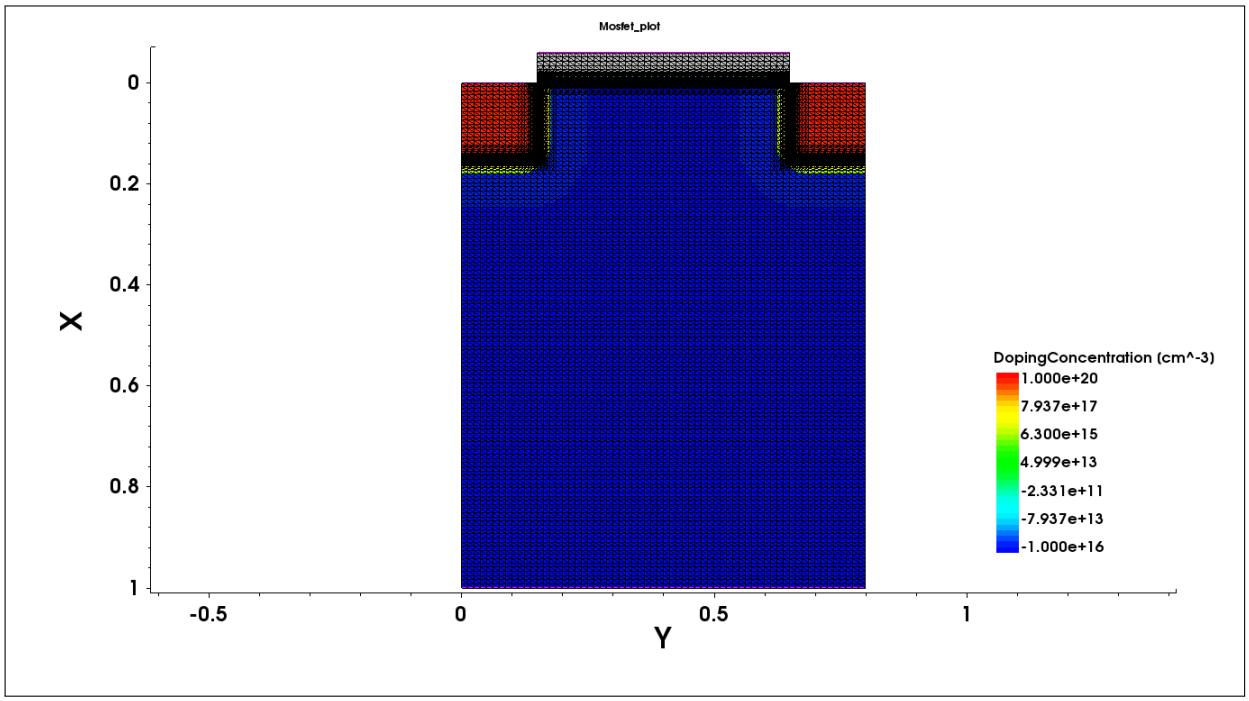

Figure 4: Simulated Structure of MOSFET Device with 500 nm Channel length with Meshing

For 180 nm Channel length:

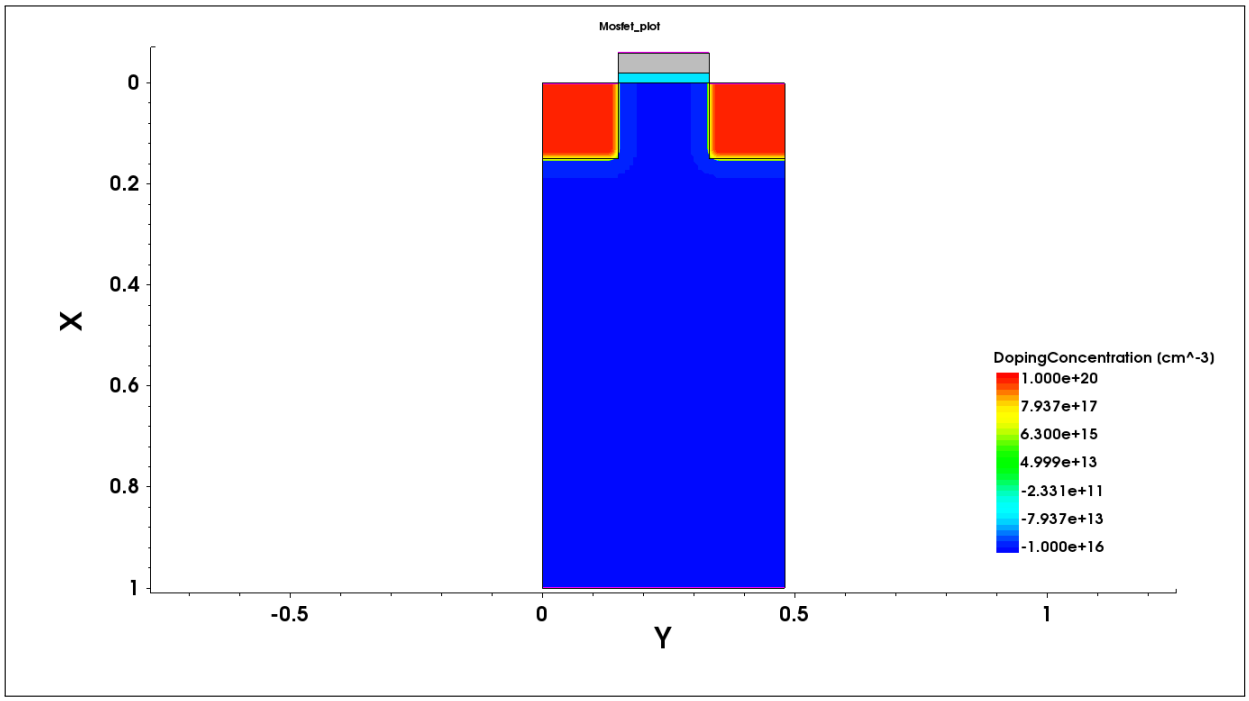

Figure 5: Simulated Structure of MOSFET Device with 180 nm Channel length

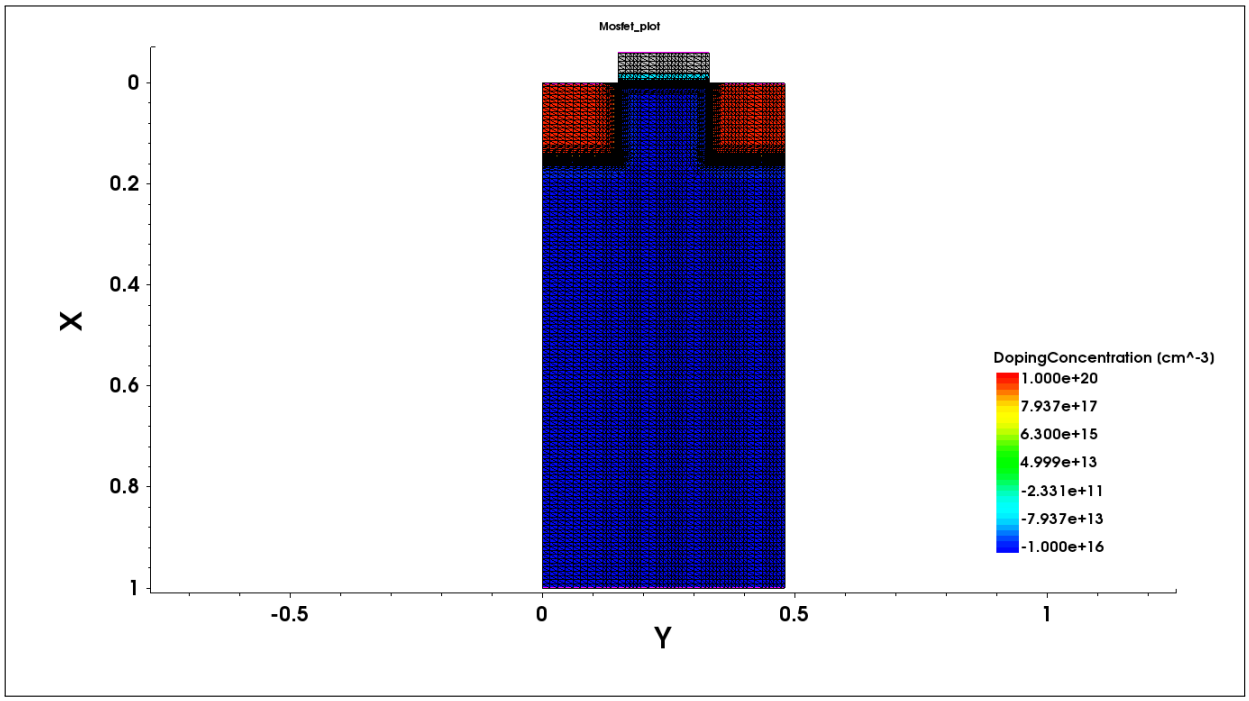

Figure 6: Simulated Structure of MOSFET Device with 180 nm Channel length with Meshing

3 Analysis of MOSFET Device

3.1 Plot and examine the transfer and output characteristics for the three cases

Transfer Characterstics (I_{DS} vs V_{GS}): Typically V_ds is fixed for the I_D vs V_{GS}. The transition from the ON state to the OFF state is gradual

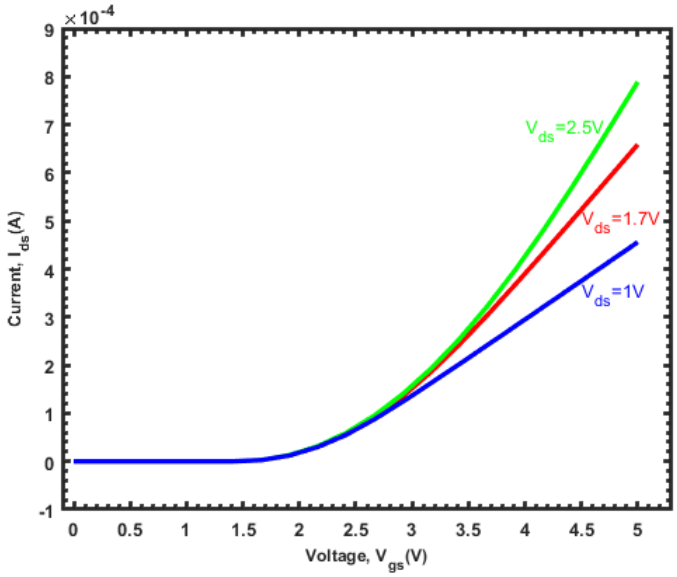

Figure 7: I_{DS} vs V_{GS} with 1.5 μm Channel length

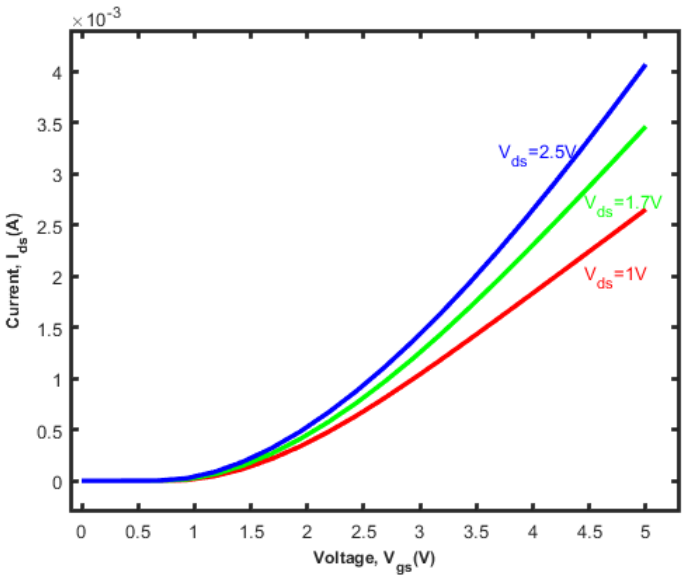

Figure 8: I_{DS} vs V_{GS} with 500 nm Channel length

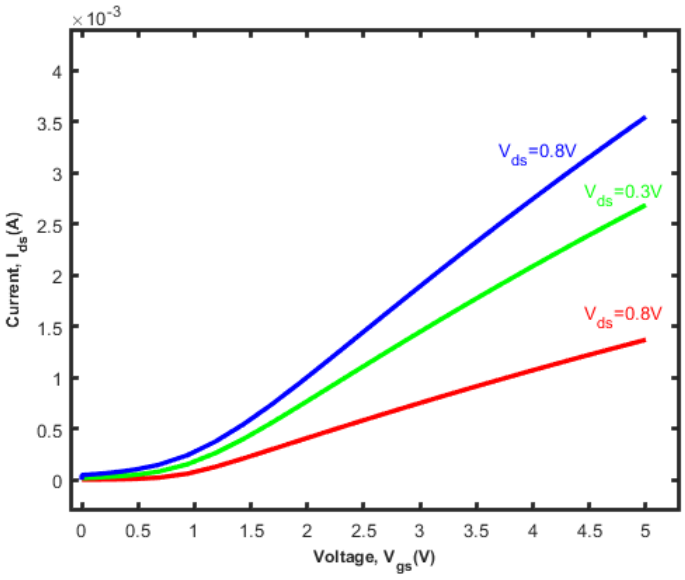

Figure 9: I_{DS} vs V_{GS} with 180 nm Channel length

Output Characterstics (I_{DS} vs V_{DS}):

3.2 Plot energy band diagram for various regions.

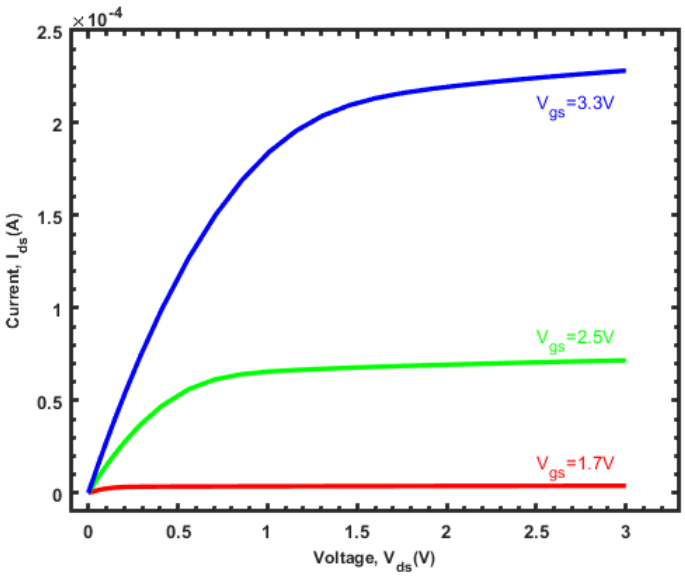

Figure 10: I_{DS} vs V_{DS} with 1.5 μm Channel length

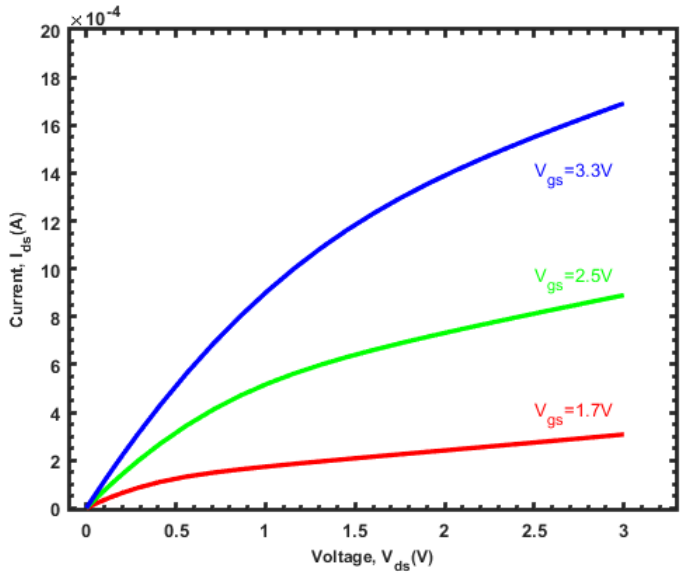

Figure 11: I_{DS} vs V_{DS} with 500 nm Channel length

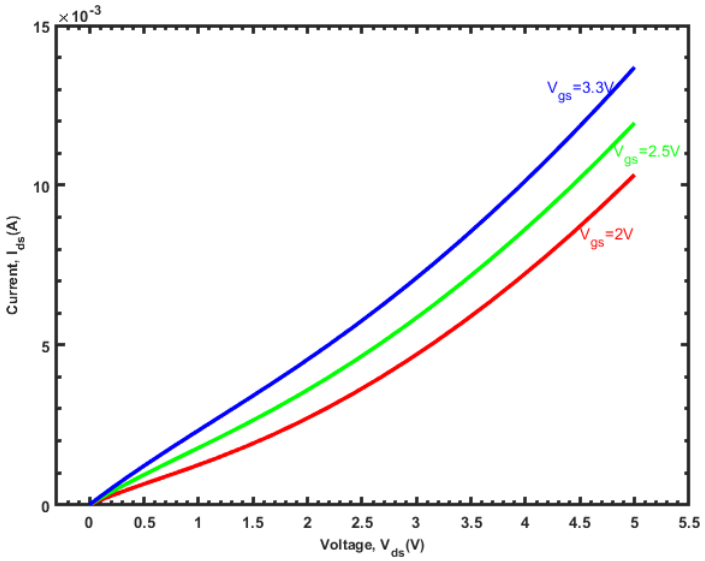

Figure 12: I_{DS} vs V_{DS} with 180 nm Channel length

3.3 Plot energy band diagram for various regions.

First, we have to calculate the value of metal work function ϕ_m. We have p-type substrate. So,
Electron Affinity of silicon (χ_s) = 4.05 eV
E_C - E_i = 0.56 eV
Substrate Doping (N_A) = $5\times10^{16} cm^{-3}$
Intrinsic carrier concentration (n_i) = $1.5\times10^{10} cm^{-3}$
$\frac{KT}{q}$ = 0.0259 V
E_i - E_f = $\frac{KT}{q} Ln(\frac{N_A}{n_i})$ = $0.0259 Ln(\frac{5\times10^{16}}{1.5\times10^{10}})$ = 0.389 eV

$\phi_m = \chi_s$ + (E_C - E_i) + (E_i - E_f) = 4.05 + 0.56 + 0.389 = 5 eV

For C_{OX},
Dielectric Constant of SiO_2 = ϵ_{OX} = 3.9
thickness of SiO_2 (t_{OX}) = 20 nm
ϵ_o=8.85×10^{-12} $\frac{F}{m}$
Oxide Capacitance C_{OX} = $\frac{\epsilon_{OX}\times\epsilon_o}{t_{OX}}$ = 0.172 $\frac{\mu F}{cm^2}$

For C_{DEP},
Dielectric Constant of Si = ϵ_s = 11.8
thickness of depletion width (W_{dmax}) = $\sqrt{\frac{2\epsilon_s\epsilon_o 2\phi_f}{qN_A}}$ = 0.1425μm
ϵ_o=8.85×10^{-12} $\frac{F}{m}$
Depletion Capacitance C_{DEP} = $\frac{\epsilon_{OX}\times\epsilon_o}{t_{OX}}$ = 0.732 $\frac{nF}{cm^2}$

So we have set the value of metal work function in parameter file and plots the Energy band diagrams in various regions

Energy Band Diagram in Equilibrium or Flat Band Condition

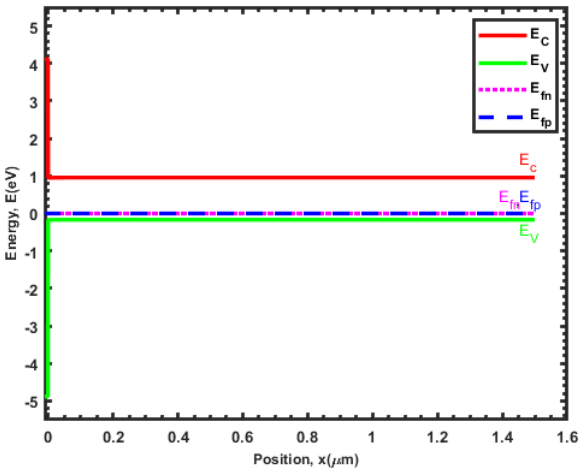

Figure 13: Energy Band Diagram at V_g = 0 V

Flat Band occurs when V_g = 0 V. The flat band voltage is the voltage where no band bending occurs. At the flat-band voltage, electric field is zero everywhere.

Energy Band Diagram in Accumulation Region

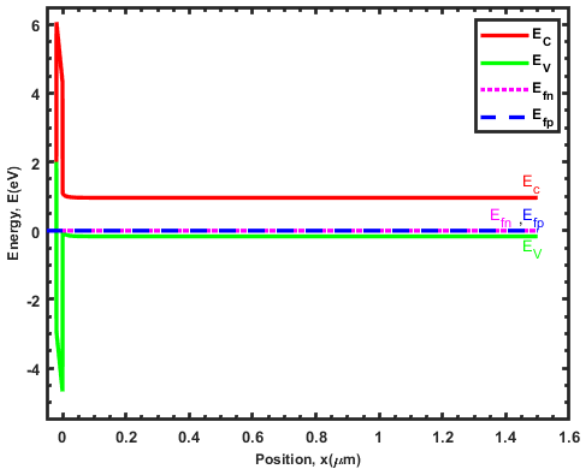

Figure 14: Energy Band Diagram at V_g = -2 V

Accumulation occurs at voltage V_g less than flat band condition. For p-type substrate when we applied negative voltage, the negative charge on the gate attracts the hole from the substrate. So band bending occurs as shown in above figure.

Energy Band Diagram in Depletion Region

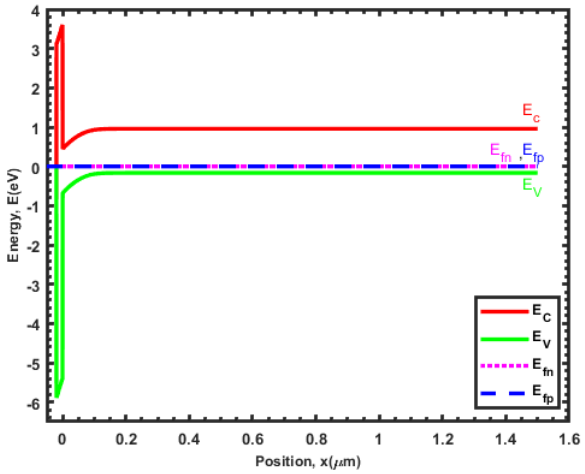

Figure 15: Energy Band Diagram at V_g = 1 V

As we increase the value of applied voltage from negative to positive, the holes will repelled back to the bulk and depletion charges accumulated near the Si-SiO_2 interface. A depletion region is formed and $\phi_s < 2\phi_f$. So band bending occurs in other direction as shown in above figure.

Energy Band Diagram in Inversion Region

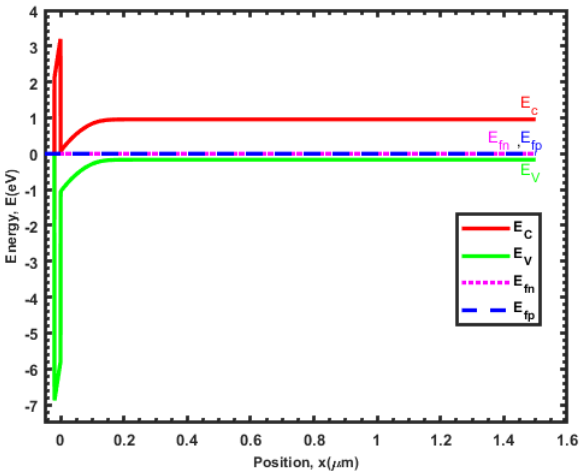

Figure 16: Energy Band Diagram at $V_g = 2$ V

$$\mathrm{V}_{th} = 2\phi_F + \frac{K_s}{K_O} x_o \sqrt{\frac{4qN_A}{K_s \epsilon_O} \phi_F}$$

$\phi_S = 2\phi_F = 2 \times 0.389 = 0.778$ V
Dielectric Constant of Silicon ,$K_S = 11.8$
Dielectric Constant of SiO_2 ,$K_O = 3.9$
Thickness of oxide ,$x_O = 20$ nm
Substrate Doping, $N_A = 5 \times 10^{16} cm^{-3}$
So the Calculated Value of V_{th} is,

$$\mathrm{V}_{th} = 1.47 \text{ V}$$

As we further increase the applied voltage value than the electrons accumulate near the Si-SiO_2 interface and a condition will come When $\phi_s = 2\phi_f$ this is onset of inversion and the applied voltage at this condition is threshold voltage. Now, for $\phi_s > 2\phi_f$ strong inversion. So band bending increases as shown in above figure.

Now we are doing the x cut analysis of the MOSFET . so we are plotting the Energy bands for cutt off , linear and saturation region of operation.

Energy Band Diagram For Channel length 1.5 μm in Cutt off Region

$$V_{GS} = 0 \text{ V}$$

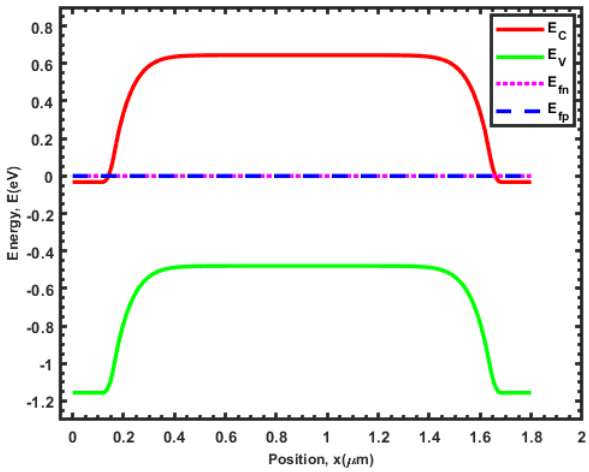

Figure 17: Energy Band Diagram in Cutt off region at $V_{GS} = 0$ V

Above Plot is for the MOSFET having channel length (1.5 μm) is in cuttoff region .

Energy Band Diagram For Channel length 1.5 μm in Linear Region

$$V_{GS} = 1.8 \text{ V}$$
$$V_{DS} = 0.3 \text{ V}$$

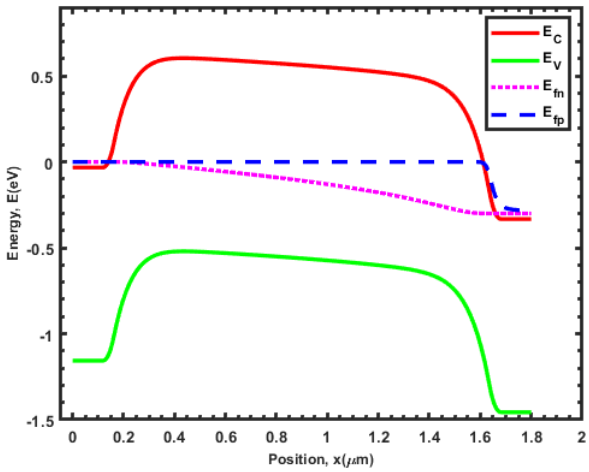

Figure 18: Energy Band Diagram in Linear region at $V_{GS} = 1.8$ V ,$V_{DS} = 0.3$ V

Above Plot is for the MOSFET having channel length (1.5 μm) is in Linear region and we observe that on drain side barrier height increases and the shift is -qV_{DS} = -0.3 ev and on gate side the energy level shifted by -q(V_{GS} - V_{TH} = -0.34 eV

Energy Band Diagram For Channel length 1.5 μm in Saturation Region

$V_{GS} = 1.8$ V
$V_{DS} = 0.9$ V

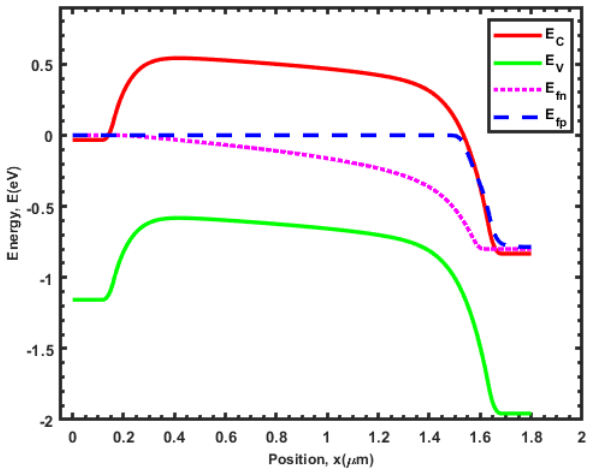

Figure 19: Energy Band Diagram in saturation region at $V_{GS} = 1.8$ V ,$V_{DS} = 0.9$ V

Above Plot is for the MOSFET having channel length (1.5 μm) is in Saturation region and we observe that on drain side barrier height increases and the shift is -qV_{DS} = -0.9 ev and on gate side the energy level shifted by -q(V_{GS} - V_{TH} = -0.34 eV

Energy Band Diagram For Channel length 500 nm in Cutt off Region

$V_{GS} = 0$ V

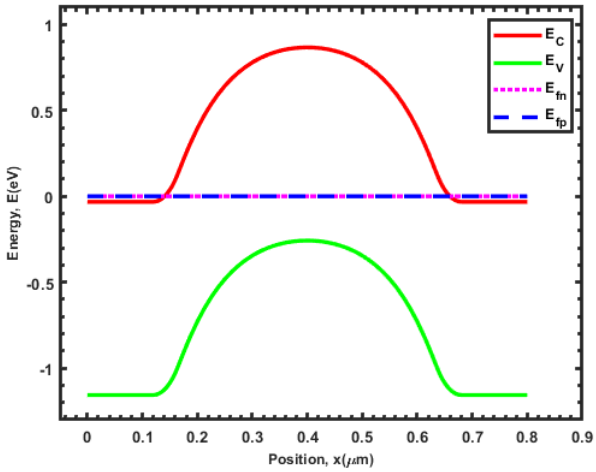

Figure 20: Energy Band Diagram in Cutt off region at $V_{GS} = 0$ V

Above Plot is for the MOSFET having channel length (500 nm) is in cuttoff region .

Energy Band Diagram For Channel length 500 nm in Linear Region

V_{GS} = 1.8 V
V_{DS} = 0.3 V

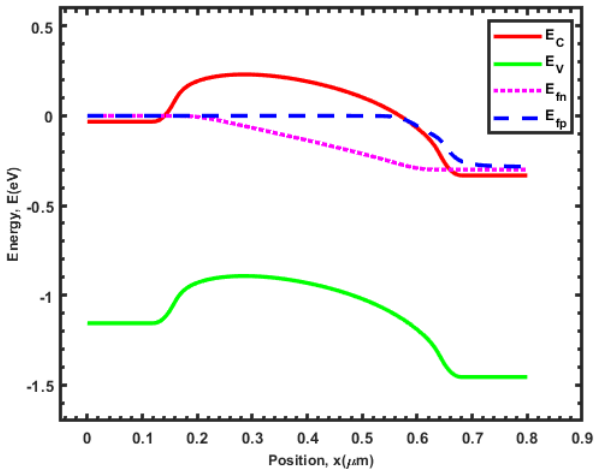

Figure 21: Energy Band Diagram in Linear region at V_{GS} = 1.8 V ,V_{DS} = 0.3 V

Above Plot is for the MOSFET having channel length (500 nm) is in Linear region and we observe that on drain side barrier height increases and the shift is -qV_{DS} = -0.3 ev and on gate side the energy level shifted by -q(V_{GS} - V_{TH} = -0.34 eV

Energy Band Diagram For Channel length 500 nm in Saturation Region

V_{GS} = 1.8 V
V_{DS} = 0.9 V

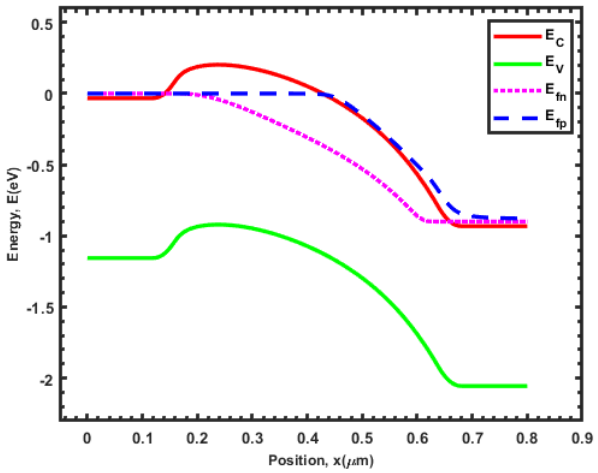

Figure 22: Energy Band Diagram in saturation region at V_{GS} = 1.8 V ,V_{DS} = 0.9 V

Above Plot is for the MOSFET having channel length (1.5 μm) is in Saturation region and we observe that on drain side barrier height increases and the shift is -qV_{DS} = -0.9 ev and on gate side the energy level shifted by -q(V_{GS} - V_{TH} = -0.34 eV .

Energy Band Diagram For Channel length 180 nm in Cutt off Region

$V_{GS} = 0$ V

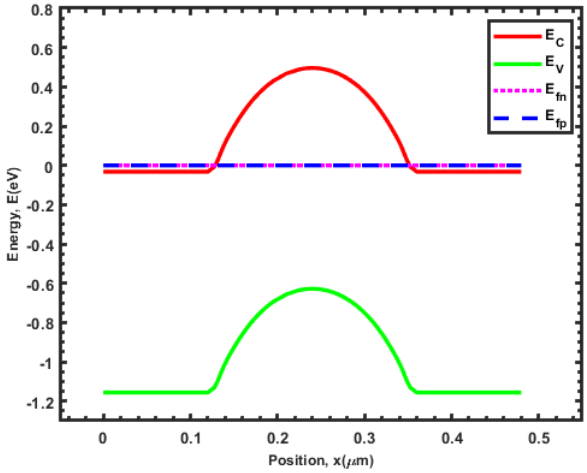

Figure 23: Energy Band Diagram in Cutt off region at $V_{GS} = 0$ V

Above Plot is for the MOSFET having channel length (180 nm) is in cuttoff region .

Energy Band Diagram For Channel length 180 nm in Linear Region

$V_{GS} = 1.8$ V
$V_{DS} = 0.3$ V

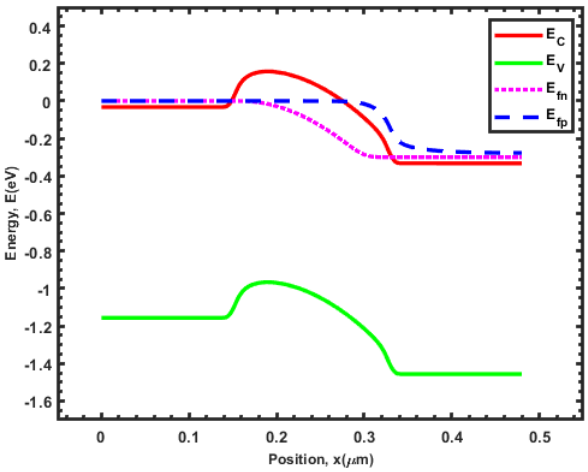

Figure 24: Energy Band Diagram in Linear region at $V_{GS} = 1.8$ V ,$V_{DS} = 0.3$ V

Above Plot is for the MOSFET having channel length (180 nm) is in Linear region and we observe that on drain side barrier height increases and the shift is -qV_{DS} = -0.3 ev and on gate side the energy level shifted by -q(V_{GS} - V_{TH} = -0.34 eV

Energy Band Diagram For Channel length 180 nm in Saturation Region

V_{GS} = 1.8 V
V_{DS} = 0.9 V

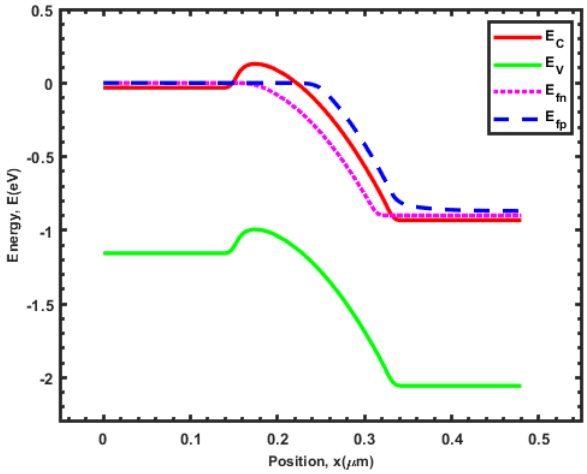

Figure 25: Energy Band Diagram in saturation region at V_{GS} = 1.8 V ,V_{DS} = 0.9 V

Above Plot is for the MOSFET having channel length (180 nm) is in Saturation region and we observe that on drain side barrier height increases and the shift is -qV_{DS} = -0.9 ev and on gate side the energy level shifted by -q(V_{GS} - V_{TH} = -0.34 eV .

3.4 Find out the various performance parameters only for 500 nm devices, along with theoretical calculations for Vt(lin), Vt(sat), gm, gds, Subthreshold slope, DIBL, Ion/Ioff, Av and ft

3.4.1 $V_{T,Lin}$ and $V_{T,Sat}$

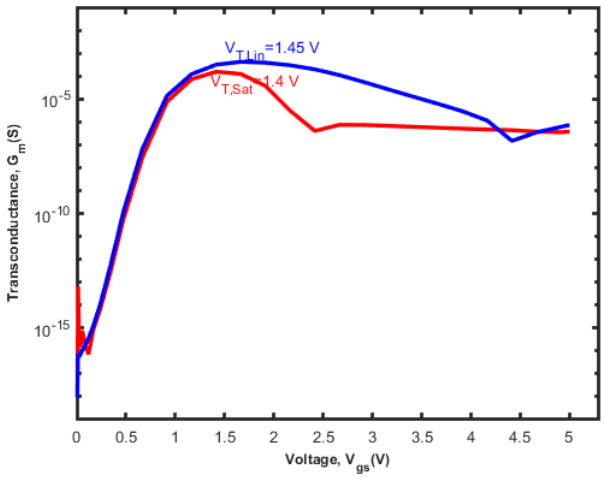

Figure 26: $V_{T,Lin}$ and $V_{T,Sat}$ for 500 nm device

$V_{T,Lin}$ is calculated from the g_m vs V_{gs} for low $V_{ds} = 0.2V$
$V_{T,Sat}$ is calculated from the g_m vs V_{gs} for High $V_{ds} = 1$ V

$$V_{T,Lin} = 1.45 \text{ V}$$
$$V_{T,Sat} = 1.4 \text{ V}$$

3.4.2 Transconductance g_m

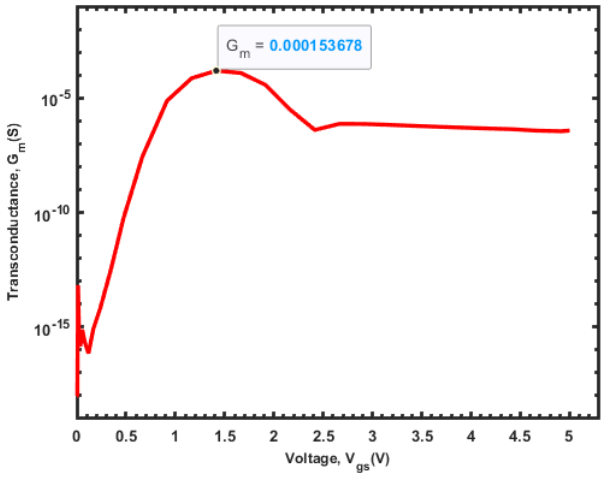

Figure 27: g_m vs V_{gs} for 500 nm device

$$g_{m,max} = \frac{dI_{ds}}{dV_{GS}}$$
$$g_{m,max} = 0.15 \text{ mS}$$

3.4.3 Transconductance g_{ds}

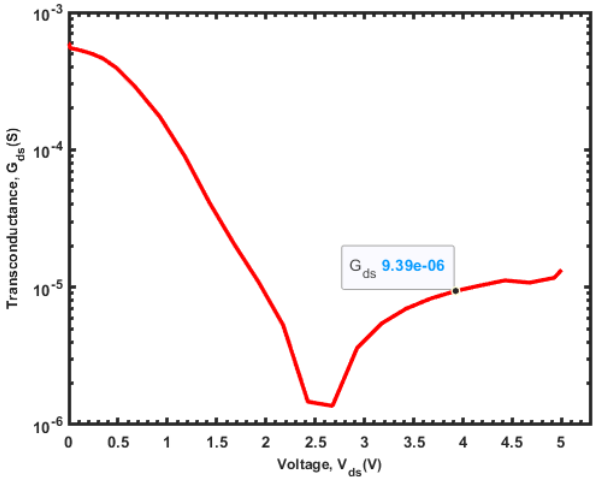

Figure 28: g_{ds} vs V_{gs} for 500 nm device

$$g_{ds} = 9.39 \ \mu\text{S}$$
$$R_o = \frac{1}{g_{ds}} = 105Kohm$$

3.4.4 Subthreshold Slope:

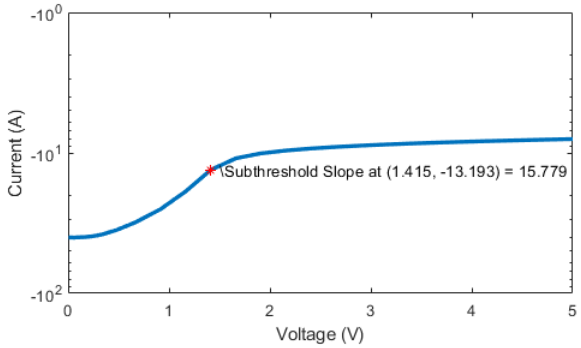

Figure 29: Subthreshold Slope for 500 nm device

$$\text{Subthreshold Slope} = \frac{dLogI_{DS}}{dV_{GS}}$$
$$\text{Subthreshold Swing} = \frac{1}{SubthresholdSlope} = 63 \text{ mV/decade}$$

3.4.5 DIBL:

$$V_{DS,Low} = 0.2 \text{ V}$$
$$V_{DS,High} = 1 \text{ V}$$
$$V_{T,Lin} = 1.45 \text{ V}$$
$$V_{T,Sat} = 1.4 \text{ V}$$

$$DIBL = \frac{V_{T,Lin} - V_{T,Sat}}{V_{DS,High} - V_{DS,Low}} = \frac{1.45 - 1.4}{1 - 0.2} = 0.0625 \tag{1}$$

3.4.6 Ion/Ioff

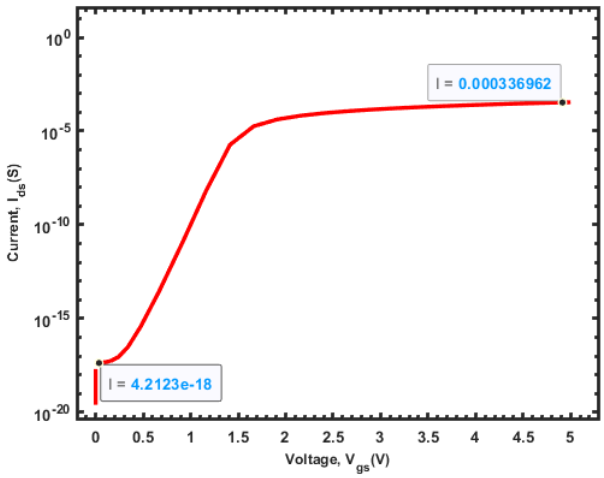

Figure 30: Ion/Ioff for 500 nm device

$$\text{Ion} = 0.3 \text{ mA}$$
$$\text{Ioff} = 4.2 \times 10^{-18}$$

$$\frac{Ion}{Ioff} = 7.14 \times 10^{16} \tag{2}$$

3.4.7 Gain, A_V

$$\text{Gain, } A_V = g_m \times R_o$$
$$g_m = 0.15 \text{ mA/V}$$
$$R_o = 105 \text{ Kohm}$$
$$\text{Gain, } A_V = 15.75 \text{ V/V}$$
$$\text{Gain, } A_V \text{ (in DB)} = 20 \text{ Log(Gain, } A_V \text{)} = 23.94 \text{ DB}$$

3.4.8 Transit Frequency F_T

$$F_T = \frac{g_m}{2\times\pi\times(C_{gs}+C_{gd})}$$

3.5 Effect of body bias voltage on energy band(at least three biases) for channel length 500 nm

Now we are apply a voltage V_{BS} and we will observe the changes in Band Diagram

Energy Band Diagram For Body bias voltage V_{BS}=0 V

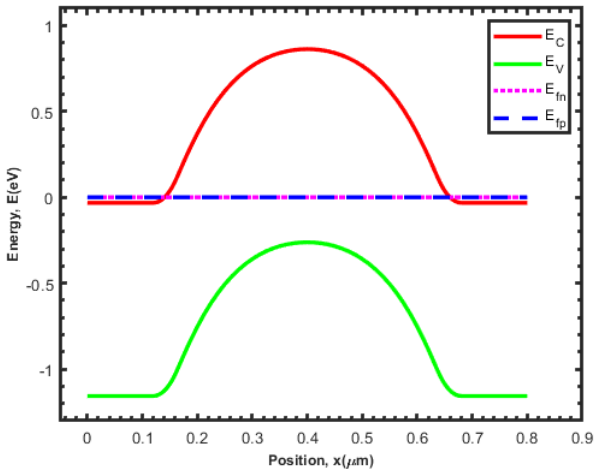

Figure 31: Energy Band Diagram For Body bias voltage V_{BS}=0 in 500 nm Device

For V_{BS}=0 V , there is no change in the Barrier

Energy Band Diagram For Body bias voltage V_{BS}=0.2 V

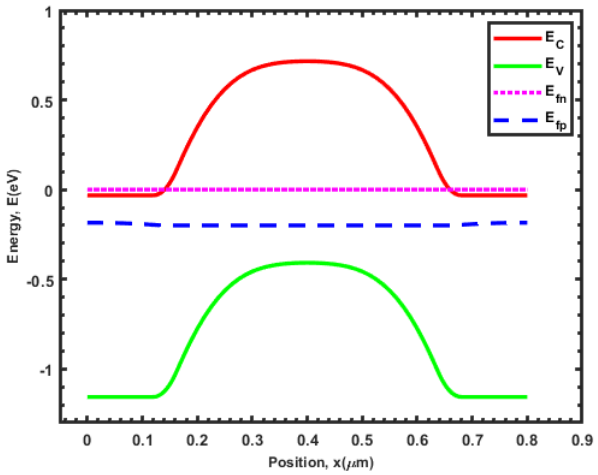

Figure 32: Energy Band Diagram For Body bias voltage V_{BS}=0.2 V in 500 nm Device

For V_{BS}=0.2 V , there is a slight change in Band bending , Barrier height is reduced by -qV_{BS} times means it get reduced by 0.2 eV

Energy Band Diagram For Body bias voltage V_{BS}=0.5 V

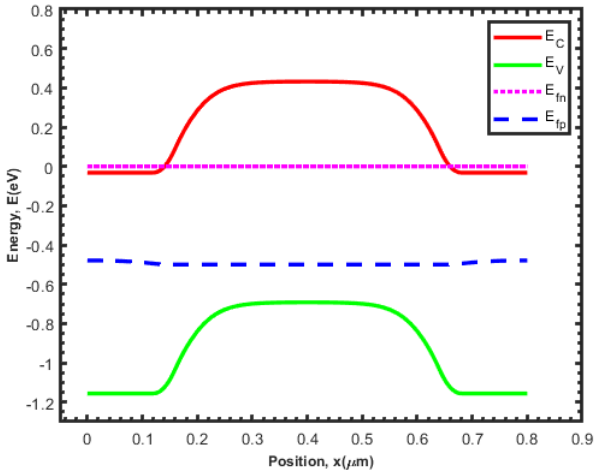

Figure 33: Energy Band Diagram For Body bias voltage V_{BS}=0.5 V in 500 nm Device

For V_{BS}=0.5 V , there is a change in Band bending , Barrier height is reduced by -qV_{BS} times means it get reduced by 0.5 eV

Energy Band Diagram For Body bias voltage V_{BS}=0.8 V

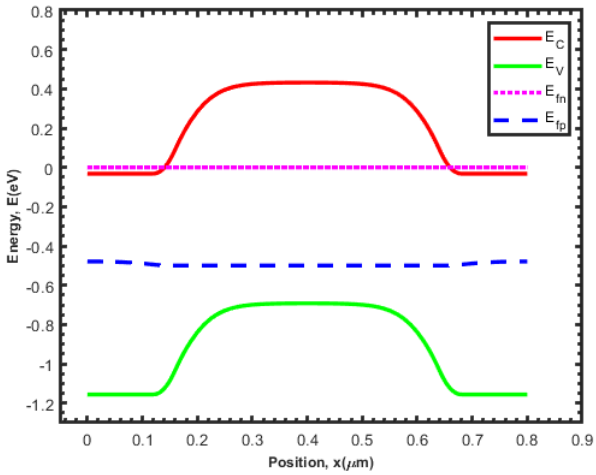

Figure 34: Energy Band Diagram For Body bias voltage V_{BS}=0.8 V in 500 nm Device

For V_{BS}=0.8 V , there is a change in Band bending , Barrier height is reduced by -qV_{BS} times means it get reduced by 0.8 eV

3.6 Vt roll-off for each device (plot Vt vs Lg)

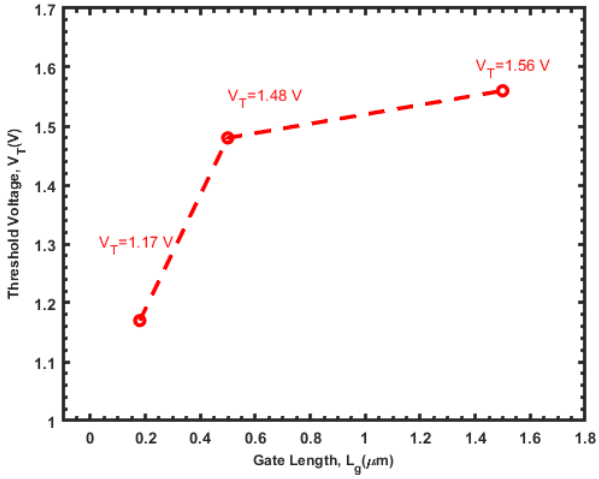

Figure 35: Threshold(V_{th}) Vs Gate Length(L_g)

$W_T = 0.1425\mu$m
$N_A = 5 \times 10^{16}$
$C_{ox} = 0.172 \ \frac{\mu F}{cm^2}$
$r_J = 0.15\mu$m

$$\Delta V_{TH} = -\frac{qN_A W_T r_j}{C_{ox} L_g}\left[\sqrt{1 + \frac{2W_T}{r_j}} - 1\right] \tag{3}$$

For Lg = 1.5 μ m :

$$\Delta V_{TH} = -0.006V \tag{4}$$

For Lg = 0.5μ m :

$$\Delta V_{TH} = -0.05V \tag{5}$$

For Lg = 0.18 μ m :

$$\Delta V_{TH} = -0.334V \tag{6}$$

4 Conclusion

This experiment involved designing of MOSFET using SWB (Sentauraus WorkBench) and used SDE (Command Line mode). During this experiment we analysis the MOSFET by observing the Energy Band Diagrams in different regions for P-type substrate, transfer and output characterstics of MOSFET , Effect of Body bias and $V_{rolloff}$.
This study also provides the good learning of the TCAD tool and learn to design the device using SDE (Command Line mode) and also get experiential learning of SWB (Sentauraus WorkBench), SDevice , SVisual.