EE537 Circuit Simulation Lab
Experiment 8

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AIM: Design of an inverting amplifier using a two stage OTA.

1 Design of an inverting amplifier using a two stage OTA

Design an inverting amplifier using a 2 stage miller compensated OTA. Fig. 1 shows the schematic of the inverting amplifier to be designed.

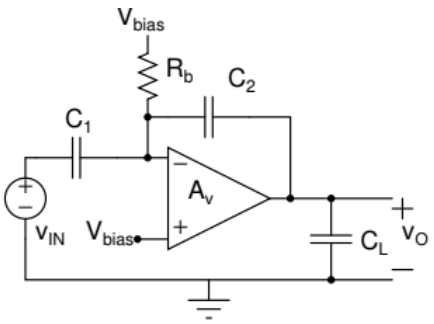

Figure 1: Inverting amplifier with capacitive voltage feedback

Target Specification	
Specification	**Value**
Midband gain	20 dB
Bandwidth	$> 1MHz$
Input capacitance	1 pF
Load capacitance	10 pF
Slew rate	$>= 10V/\mu s$
Gain error	0.1%
Phase margin	=> 65°
Operating temperature range	0°C to 70°C

Table 1 - Target Specifications for inverting amplifier using a 2 stage miller compensated OTA

1.1 Implement the 2 stage using a miller compensated 2 stage OTA. Show the calculations used for all the specifications and detailed design procedure.

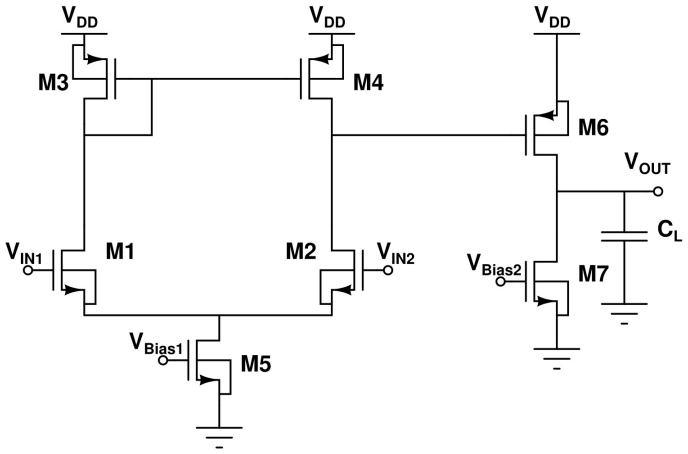

Figure 2: 2 stage OTA Without Miller compensation technique

We have to see effect of miller compensation capacitor on the performance of 2 Stage OTA. we will see the detailed technique and need of pole splitting. So, before going to analyse 2 stage OTA with Miller compensation capacitor we will analyse first analyse without miller compensation capacitor. On Observing the Above Circuit we have 2 Poles at the output of each stage and 1 zero at the gate of M3 because of parasitic capacitance at that node,

Pole 1:
So for Pole 1 at the output of first stage of 2 stage OTA is calculated in form of $\frac{1}{r_{req}C_{eq}}$ where r_{eq} and c_{eq} are the equivalent resistance and capacitance at that node .

$$P1 = \frac{1}{(r_{o2}||r_{o4})C_o} \tag{1}$$

where r_{o2} and r_{o4} are the output resitance of M2 and M4 , c_o is the parasitic capacitance at that node .
Pole 2:
So for Pole 2 at the output of second stage of 2 stage OTA is calculated in form of $\frac{1}{r_{req1}C_{eq1}}$ where r_{eq1} and c_{eq1} are the equivalent resistance and capacitance at that node .

$$P1 = \frac{1}{(r_{o6}||r_{o7})C_L} \tag{2}$$

where r_{o6} and r_{o7} are the output resitance of M6 and M7 , c_L is the Load capacitance at that node .
Zero:

$$Z1 = \frac{g_{m3}}{C_P} \tag{3}$$

where $\frac{1}{g_{m3}}$ are the output resitance of M3 and M4 , c_P is the parasitic capacitance at that node .

On observing the above two poles we can claim that these poles are very close to each other due to which we cant reach to our target specification. Because we get phase margin approximately 0° So here comes the concept of Pole splitting. In pole splitting we want that one pole moves towards origin and other pole moves away from the origin. for doing this we have to use miller compensation capacitor beetween the two stages. The circuit follows as:

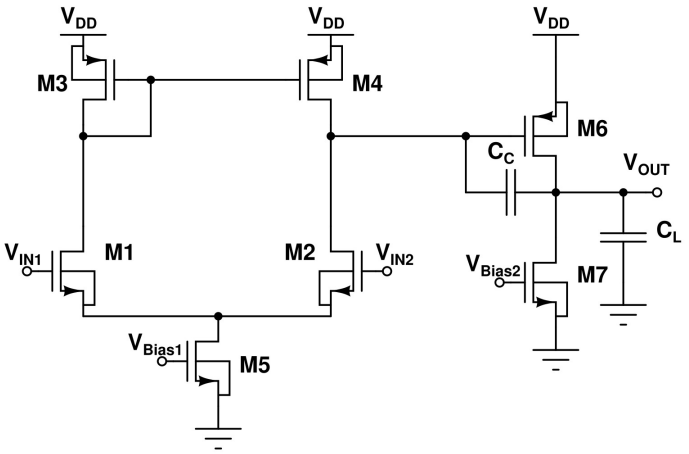

Figure 3: 2 stage OTA With Miller compensation technique

Now we have to find the pole and zero for above circuit,

Pole 1:

$$P1 = \frac{1}{(r_{o2}||r_{o4})(C_c g_{m7}(r_{o6}||r_{o7}))} \tag{4}$$

Due to Miller capacitor, we find that pole at the output of the first stage of 2 stage OTA is move closer to origin and becomes dominant pole.

Pole 2:

$$P2 = \frac{1}{\frac{1}{g_{m7}}C_L} = \frac{g_{m7}}{C_L} \tag{5}$$

Due to miller capacitor, We find that pole at output of second stage of 2 stage OTA is moved away from the origin.

Zero: Now because of miller capacitor that created a zero at output of second stage. because there is current flowing path from the output of first stage to the output of second stage.so, the from M6 and current from the miller capacitor cancel out each other.

By Applying KCL at output node,

$$g_{m7}V_1 = (V_1 - V_{OUT})sC_C$$

Where V_1 is the output Voltage of first stage.

$$Z1 = \frac{g_{m7}}{C_C} \tag{6}$$

Now Transfer function A(s) is,

$$A(s) = \frac{A_o(1 - \frac{s}{Z1})}{(1 + \frac{s}{P1})(1 + \frac{s}{P2})} \tag{7}$$

for ω_{GBW} ,

$$|\frac{A_o}{(1 + \frac{s}{P1})}| = 1 \tag{8}$$

by solving this we get the relation,

$$\omega_{GBW} = A_o P_1 \tag{9}$$

where Ao = $g_{m1}(r_{o2}||r_{o4})g_{m7}(r_{o6}||r_{o7})$
P1 = $\frac{1}{(r_{o2}||r_{o4})(C_c g_{m7}(r_{o6}||r_{o7}))}$

$$\omega_{GBW} = \frac{g_{m1}}{C_c} \tag{10}$$

Now For the Phase margin ,

$$PM = 180° - tan^{-1}(\frac{\omega_{GBW}}{\omega_{P1}}) - tan^{-1}(\frac{\omega_{GBW}}{\omega_{P2}}) - tan^{-1}(\frac{\omega_{GBW}}{\omega_{Z1}}) \tag{11}$$

As we know P1 is dominant pole and $(\frac{\omega_{GBW}}{\omega_{P1}})$ is a very large no.. So, $tan^{-1}(\frac{\omega_{GBW}}{\omega_{P1}})$ is equal to 90° And for Z1 is very far from ω_{GBW} and we have a relation $\omega_{Z1} = 10 * \omega_{GBW}$. so we assume that $\frac{\omega_{GBW}}{\omega_{Z1}}$ is very less no. almost equal to zero. so $tan^{-1}(\frac{\omega_{GBW}}{\omega_{Z1}})$ is almost equal to zero.
we want to achieve 65° Phase Margin. for this,

$$65° = 180° - 90° - tan^{-1}(\frac{\omega_{GBW}}{\omega_{P2}}) \tag{12}$$

After solving this we get a relation ,

$$\omega_{P2}=4^*\omega_{GBW}$$

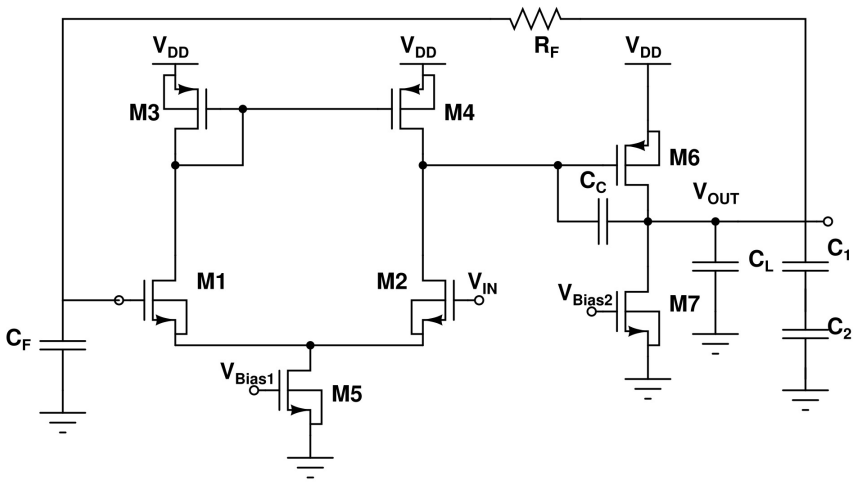

Figure 4: 2 stage OTA with miller compensation capacitor with feedback

For this Circuit Transfer function is,

$$A(s) = \frac{A_o(1 - \frac{s}{Z1})}{(1 + \frac{s}{P1})(1 + \frac{s}{P2})} * \frac{C_2}{C_1 + C_2} \tag{13}$$

And ω_{GBW} is,

$$\omega_{GBW} = \frac{g_{m1}}{C_c} * \frac{C_2}{C_1 + C_2} \tag{14}$$

We have given midband gain = 20dB so, $given C_1 = 100fF$ and $C_L = 10pF$. so from midband gain we can calculate the value of $C_2 = 1pF$.
we have 2 equations;

$$\omega_{P2}=4^*\omega_{GBW}$$
$$\omega_{Z1} = 10 * \omega_{GBW}$$
Using above two equations we get,
$$\omega_{Z1} = 2.5 * \omega_{P2}$$
$$\frac{g_{m7}}{C_C} = 2.5 * \frac{g_{m7}}{C_L}$$
$$C_C = 4pF$$

Now we have given Slew Rate given that it should be $>= 10V/\mu s$
Slew rate is given by = Min$(\frac{I_5}{C_C}, \frac{I_6}{C_C + C_L + \frac{C_1 C_2}{C_1 + C_2}})$

$$\frac{I_5}{C_C} >= 10V/\mu s \tag{15}$$

$$I_5 >= 10 * 4pFV/\mu s >= 40\mu A \tag{16}$$

$$\frac{I_6}{C_C + C_L + \frac{C_1 C_2}{C_1 + C_2}} >= 10V/\mu s \tag{17}$$

$$C_C + C_L + \frac{C_1 C_2}{C_1 + C_2} = 14.09pF$$

$$I_6 >= 10V/\mu s * 14.09pF >= 140.09\mu A \tag{18}$$

Transistor Sizing

For M1 and M2 are matched differential input pair and it will have same current of $I_5/2$.

$$I_1 \text{ and } I_2 = 20\mu A$$
$$V_{gs1} = 600\ mV$$
$$V_{th,n} = 500\ mV$$
$$\mu_n * C_{ox} = 300\ \mu S \text{ So, } (\frac{W}{L})_1 = (\frac{W}{L})_2$$

So for W/L we will find with NMOS Current equation in saturation mode:

$$I_{1,2} = 1/2 * \mu_n * C_{ox} * (W/L)_{1,2} * (V_{gs1,2} - V_{th,n})^2 \tag{19}$$

$$20\mu A = 1/2 * 300\mu S * (W/L)_{1,2} * (600mV - 500mV)^2 \tag{20}$$

By Solving this,

$$\boxed{(\frac{W}{L})_1 = (\frac{W}{L})_2 = 13.33}$$

Now for Transistor M3 and M4 are forming a Pmos current mirror load so $(\frac{W}{L})_3 = (\frac{W}{L})_4$. And same current flow $I_5/2 = 20\ \mu A$.

$$|V_{gs3,4}| = 600\ mV$$
$$|V_{th,p}| = 500\ mV$$
$$\mu_p * C_{ox} = 150\ \mu S$$

$$I_{3,4} = 1/2 * \mu_p * C_{ox} * (W/L)_{3,4} * (|V_{gs3,4}| - |V_{th,p}|)^2 \tag{21}$$

$$20\mu A = 1/2 * 150\mu S * (W/L)_{3,4} * (600mV - 500mV)^2 \tag{22}$$

By Solving this,

$$\boxed{(\frac{W}{L})_3 = (\frac{W}{L})_4 = 26.67}$$

Now for M5 which is Nmos as a current source where $I_5 = 40\mu A$

$$V_{gs5} = 600\ mV$$
$$V_{th,n} = 500\ mV$$
$$\mu_n * C_{ox} = 300\ \mu S$$

$$I_5 = 1/2 * \mu_n * C_{ox} * (W/L)_5 * (V_{gs5} - V_{th,n})^2 \tag{23}$$

$$40\mu A = 1/2 * 300\mu S * (W/L)_5 * (600mV - 500mV)^2 \tag{24}$$

By Solving this,

$$\boxed{(\frac{W}{L})_5 = 26.67}$$

Now for second stage transistors M6 and M7,
For Nmos M6 , $I_6 = 140.09\ \mu A$

$$V_{gs6} = 600\ mV$$
$$V_{th,n} = 500\ mV$$
$$\mu_n * C_{ox} = 300\ \mu S$$

$$I_6 = 1/2 * \mu_n * C_{ox} * (W/L)_6 * (V_{gs6} - V_{th,n})^2 \tag{25}$$

$$140.09\mu A = 1/2 * 300\mu S * (W/L)_6 * (600mV - 500mV)^2 \tag{26}$$

By Solving this,

$$\boxed{(\frac{W}{L})_6 = 93.4}$$

Now M7, $I_7 = 140.09\ \mu A$

$$|V_{gs7}| = 600\ mV$$
$$|V_{th,p}| = 500\ mV$$
$$\mu_p * C_{ox} = 150\ \mu S$$

$$I_7 = 1/2 * \mu_p * C_{ox} * (W/L)_7 * (|V_{gs6}| - |V_{th,n}|)^2 \tag{27}$$

$$140.09\mu A = 1/2 * 150\mu S * (W/L)_7 * (600mV - 500mV)^2 \tag{28}$$

By Solving this,

$$\boxed{(\frac{W}{L})_7 = 186.8}$$

Gain Error

Closed loop gain:

$$A_{CL} = \frac{A}{1 + \beta A} \tag{29}$$

$$\Delta A_{CL} = \frac{-1}{\beta(1 + \beta A)} \tag{30}$$

$$A\beta = 10^4$$

$$\frac{\Delta A_{CL}}{A_{CL}} = \frac{1}{A\beta} * 100 = 0.01 \tag{31}$$

1.2 Show all the plots required to verify the achieved specifications.

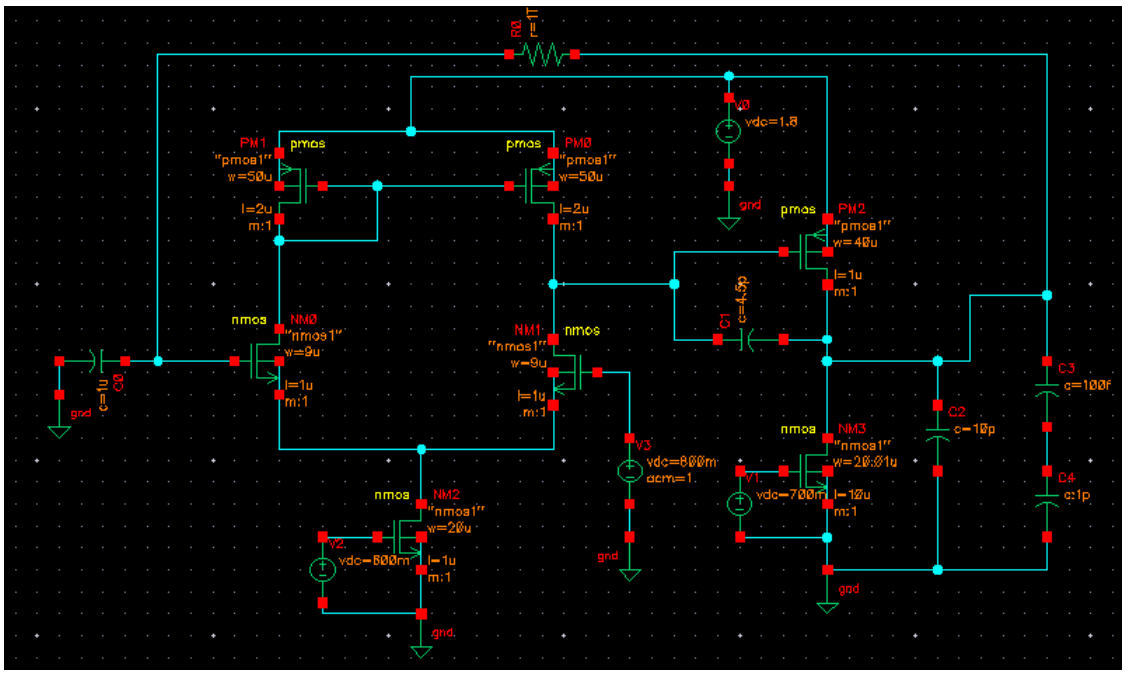

Figure 5: Schematic for 2 stage OTA

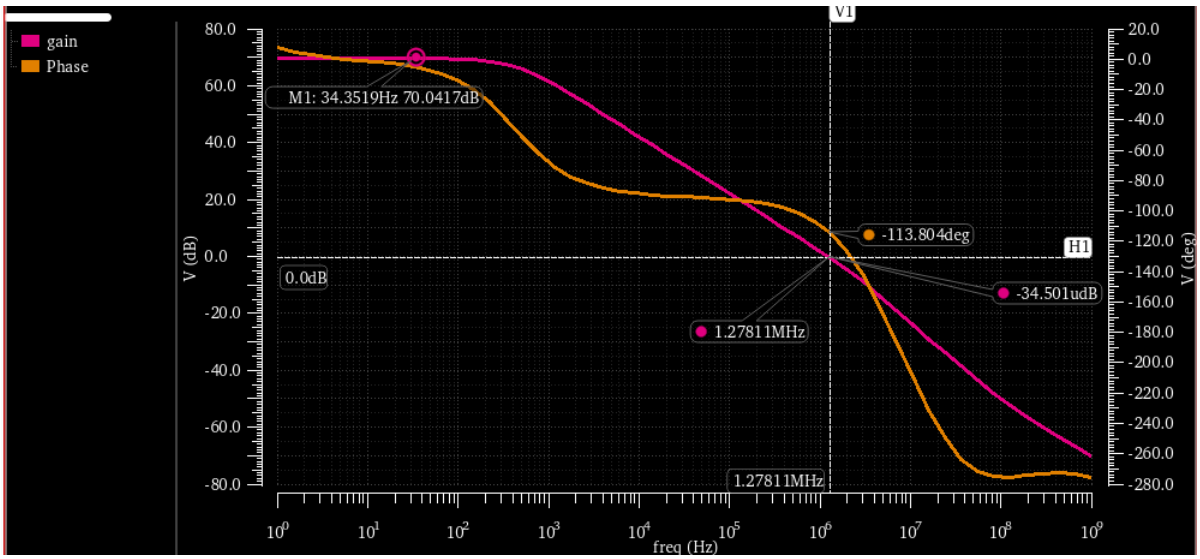

Figure 6: Gain and Phase Plot

Got a Gain of 71 dB and Phase Margin = 67°

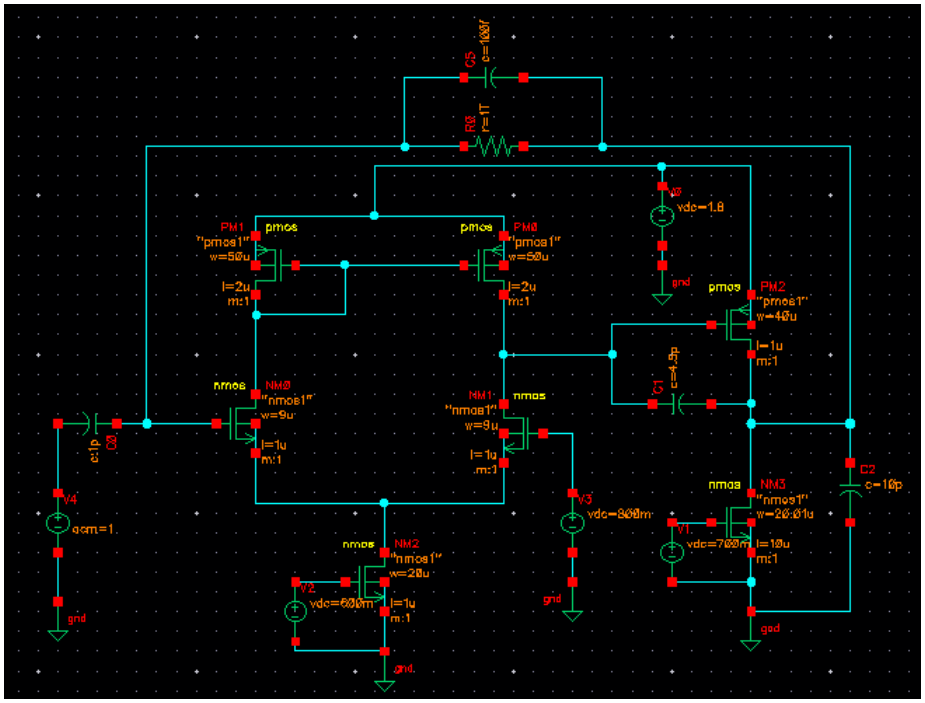

Figure 7: Schematic for Midband gain of 2 stage OTA

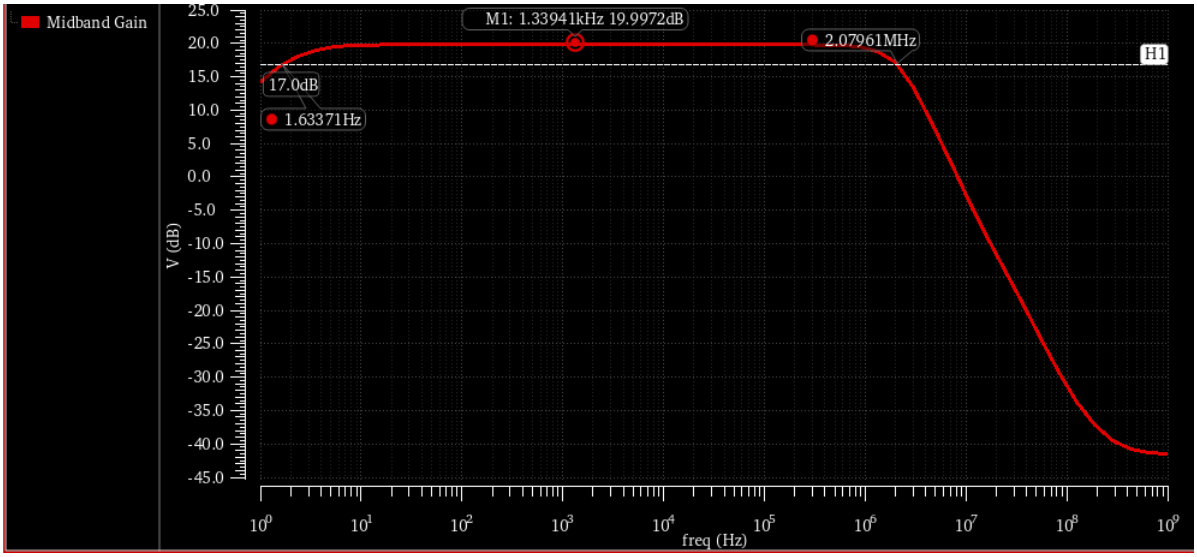

Figure 8: Midband Gain

MidBand Gain = 20 dB