EE663: Frequency Synthesizers, Clock and Data Recovery Circuits

Course Project

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Project Aim: Design a phase-locked loop (PLL) that meets the given criteria, including all sub-blocks (phase frequency detector, voltage-controlled oscillator,loop filters, and divider) using Verilog models and transistor level in Cadence design suit. .

1 Introduction

A phase-locked loop (PLL) is a circuit designed to align the output signal of an oscillator with a reference or input signal, ensuring synchronization in both frequency and phase within a given system. In the synchronized or locked state, the phase error between the output signal of the oscillator and the reference signal is either zero or remains constant. If a phase error accumulates, a control mechanism intervenes to minimize the phase error by acting on the oscillator. In this control system, the phase of the output signal becomes locked to the phase of the reference signal, hence the term "phase-locked loop." The project aims to develop a square-wave output frequency generator, primarily utilizing the PLL as a frequency multiplier, achieved by multiplying the frequency of the reference oscillator.

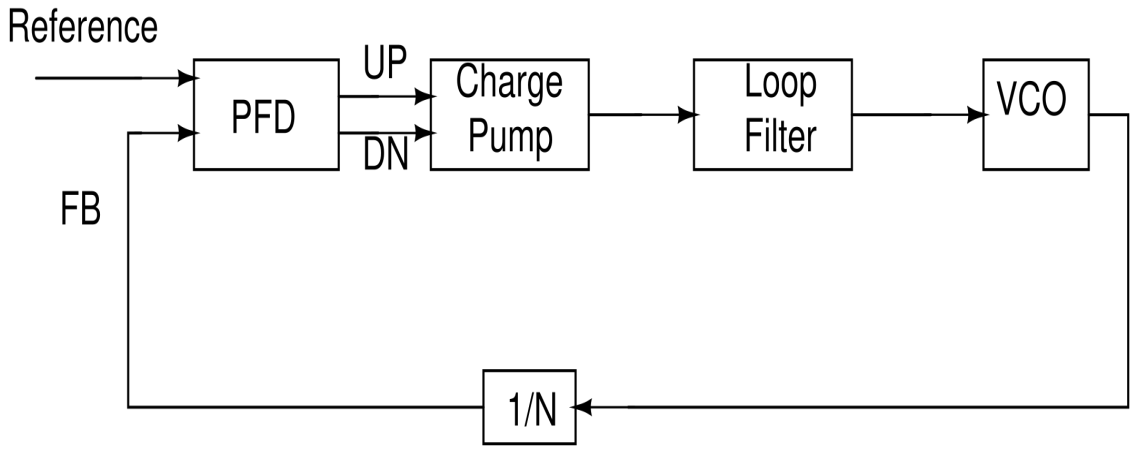

Figure 1: Basic block diagram of phase-locked loop

Target specifications

Reference Frequency	Output Frequency	Divider
2.50e+8	2.00e+9	8.00

2 Design of Phase Frequency Detector (PFD)

In PLL, the Phase frequency divider compares the phases of reference signal and feedback signal.This detector transforms the phase difference into a voltage (or current), which is subsequently processed through a Low-Pass Filter (LPF) before being converted into the phase for the Voltage Controlled Oscillator (VCO). The fundamental architecture for the phase-frequency detector is outlined below:

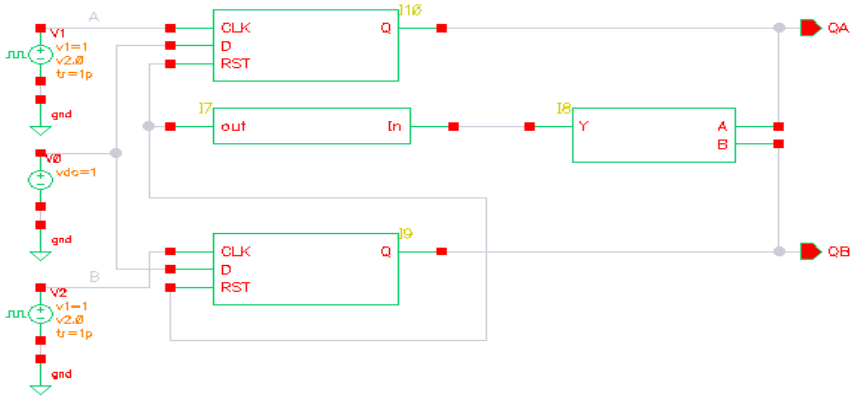

Figure 2: Circuit for phase frequency detector

For implementing PFD, We need D filp flops and And gates. so the circuit of D flip flop is consist of 2 and 3 input NAND gates and invertor. for implementing NAND and Invertor we use CMOS technology and the circuit shown in below figure:

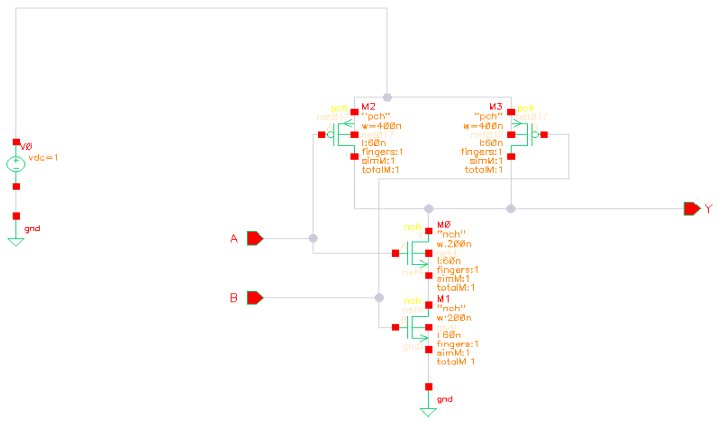

Figure 3: 2-input NAND Circuit

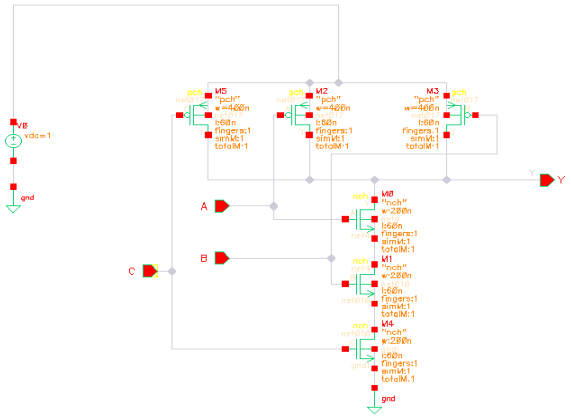

Figure 4: 3-input NAND Circuit

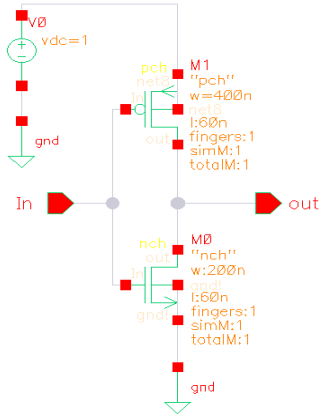

Figure 5: Invertor Circuit

Now we make the testbenches of these circuit and use it to implement D- Flip Flop.

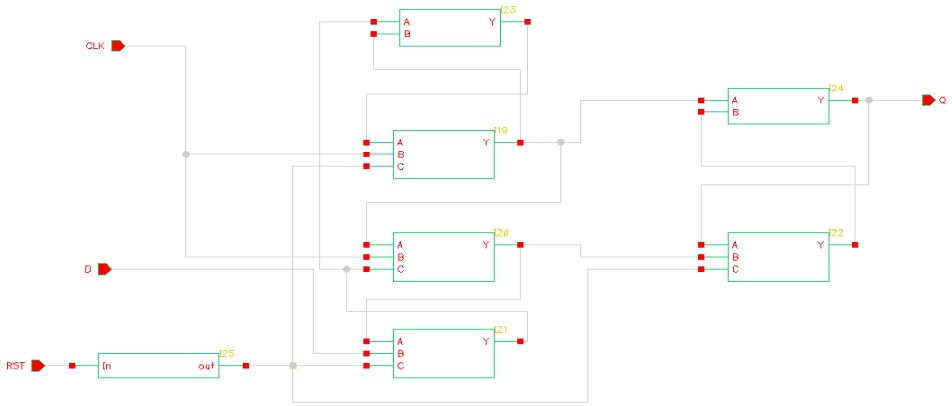

Figure 6: D flip flop circuit

Output of PFD:

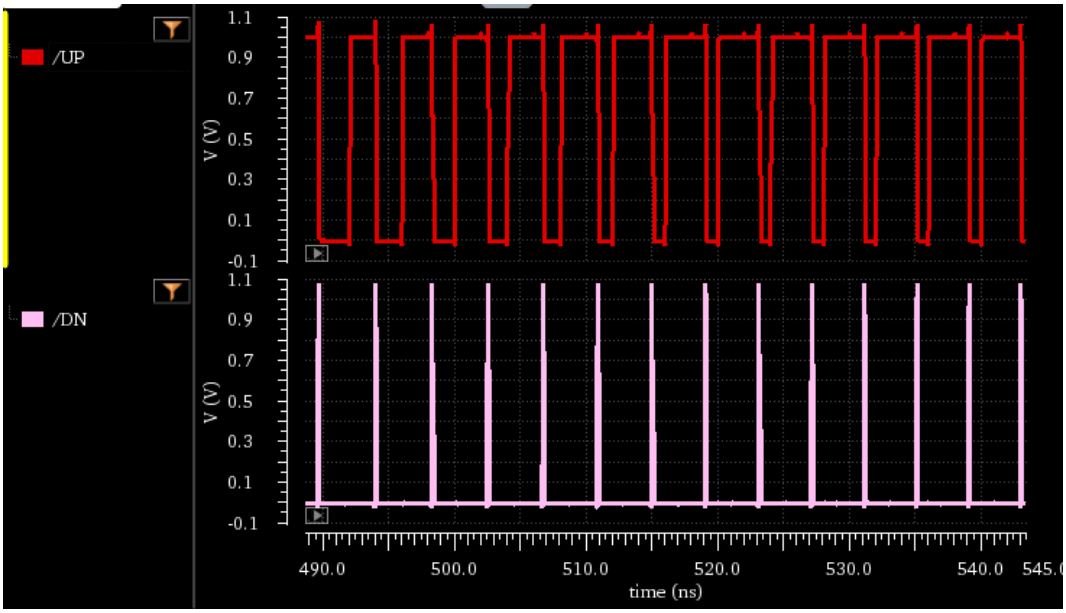

Figure 7: Output plot of PFD

In the above output plot we can conclude that phase of reference signal is ahead of feedback signal. so we can see the difference of phase and as we can also see that there is some reset delay is added.

3 Design of the Charge Pump and Loop Filter

The charge pump consists of two switches equipped with two symmetrical current sources. One current source is linked to a positive power supply, while the other is connected to a negative one. The switches alter their states based on the UP and DN signals. The output of the low-pass filter (LPF), determined by the UP and DN signals, is the Voltage-Controlled Oscillator (VCO) control signal.

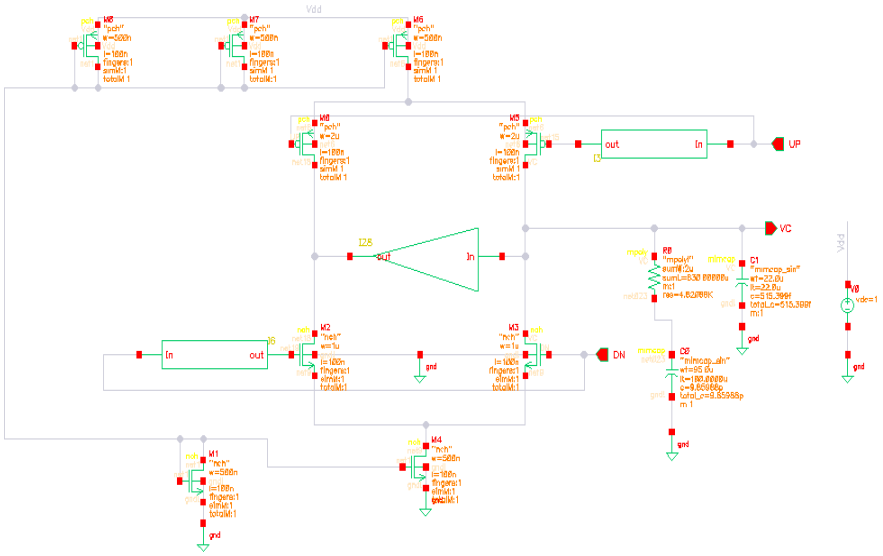

Figure 8: Charge pump and loop filter circuit

We use voltage buffer for making the voltage equal at the two nodes. so the votage buffer circuit

used in this charge pump is shown below:

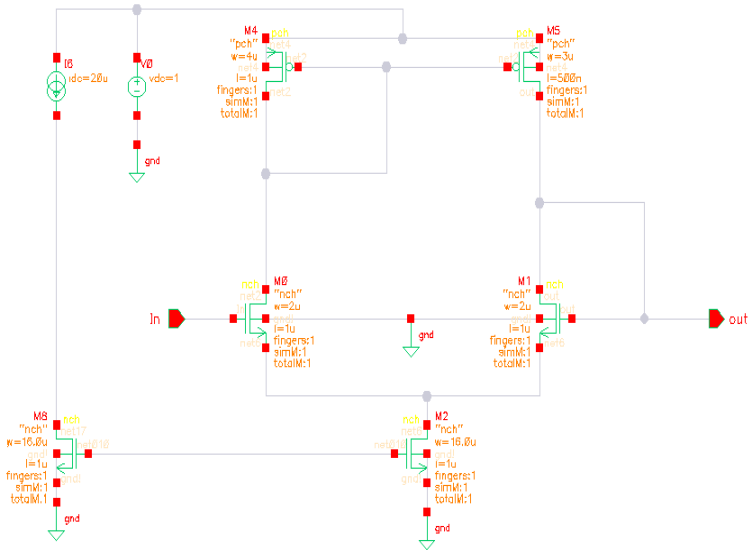

Figure 9: Voltage buffer circuit

Output of Charge Pump:

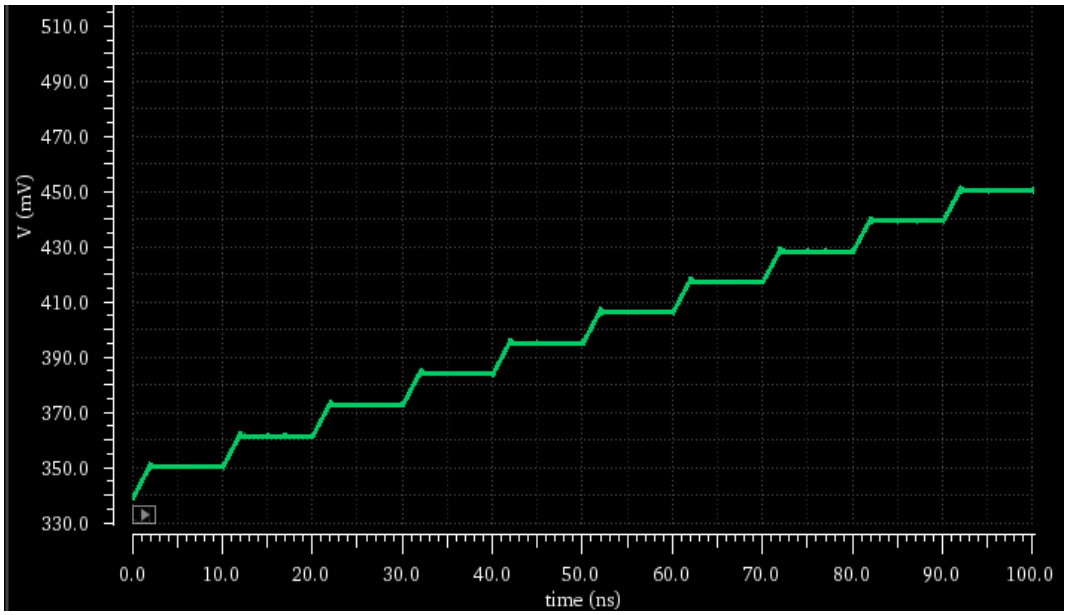

Figure 10: output of charge pump

As we can conclude it that capacitor is charging for UP signal high. for that we use voltage buffer to equate the voltage and remove the current fluctuations.

4 Design of Voltage Controlled Oscillator (VCO)

VCOs play a pivotal role in the architecture of a PLL. The fundamental concept behind a VCO is to generate a clock signal while adhering to the Barkhausen criteria for oscillation. According to the Barkhausen criteria, the magnitude of the VCO's transfer function at the oscillation frequency is unity, and the phase is at -180 degrees. The architecture for a ring VCO is outlined below:

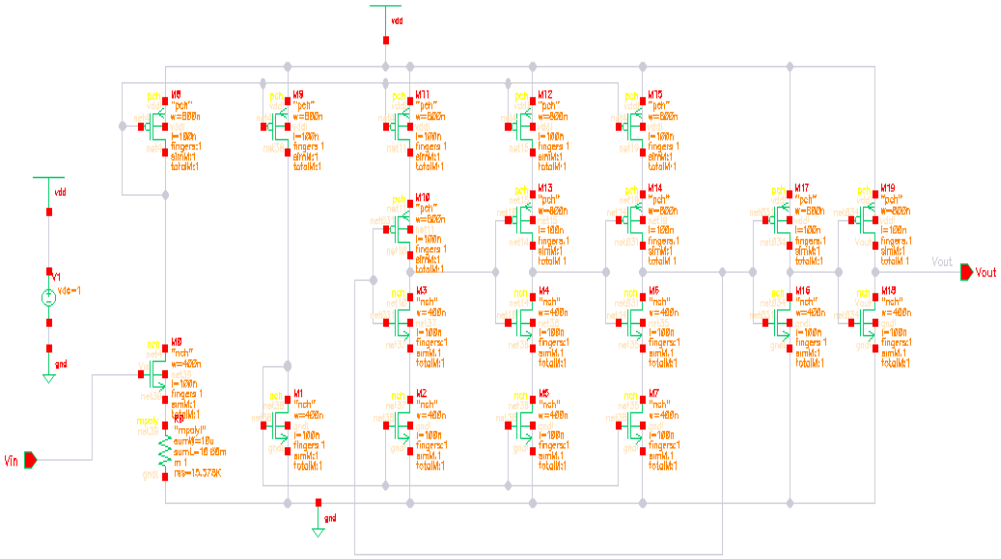

Figure 11: VCO circuit

While using VCO we need to assure to given the trigger using initial conditions in the ADEL. And, we have done the parametric analysis while sweeping input voltage V_C from 0 to 1 V and we check the output frequency while sweeping control voltage and we noted the value of V_C at that point we get the required output frequency of 2 GHz. And than we find the derivative of output frequency plot to get the K_{VCO} so we note the value of K_{VCO} from the Control voltage value at our required frequency. **Output of VCO:**

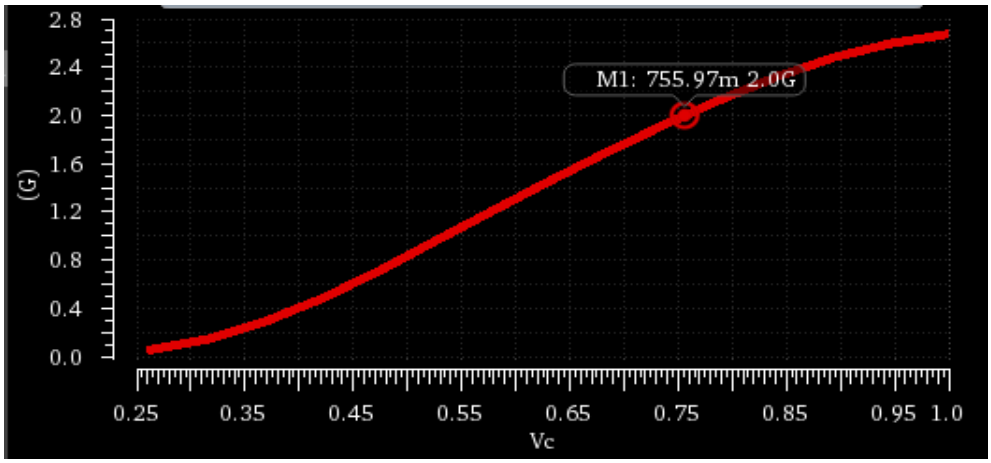

Figure 12: VCO Frequency plot

As we can see from the above plot that for 2 GHz output frequency we need V_c should be around 755.97 mV. Now for the same V_c we find the K_{VCO} from the below result.

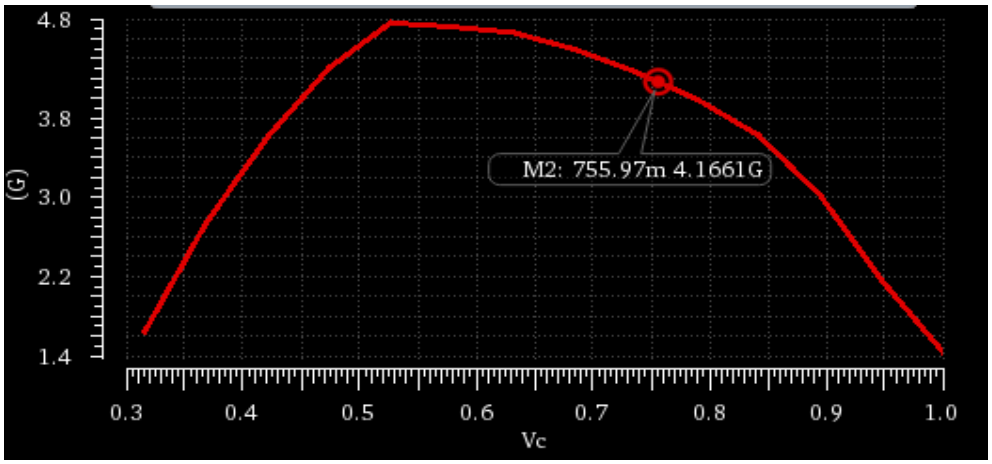

Figure 13: K_{VCO} plot

From the above plot, We get

$$\boxed{K_{VCO} = 4.16 \text{ GHz}}$$

5 Design of Frequency Divider

We use frequency divider in PLL to make tha output frequency in order of the frequency of reference frequency. Actually, we need to design the frequency divider by 8 , for that we are using 3 D flip flops in which output Q of the first D flip Flop goes in the input of other and $\bar{Q}$ is connected to the clock. schematic for Frequency divider is shown below.

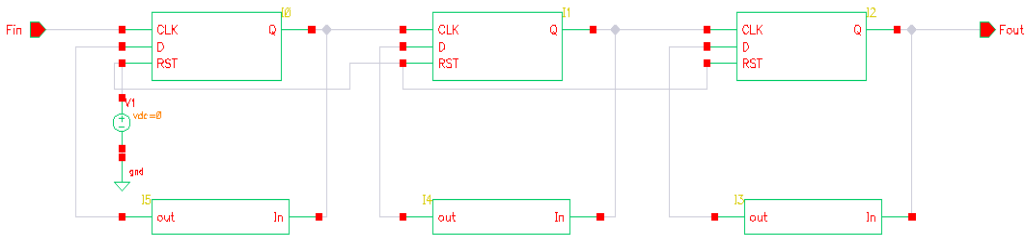

Figure 14: Schematic of frequency divider

Output plots of frequency divider by 8:

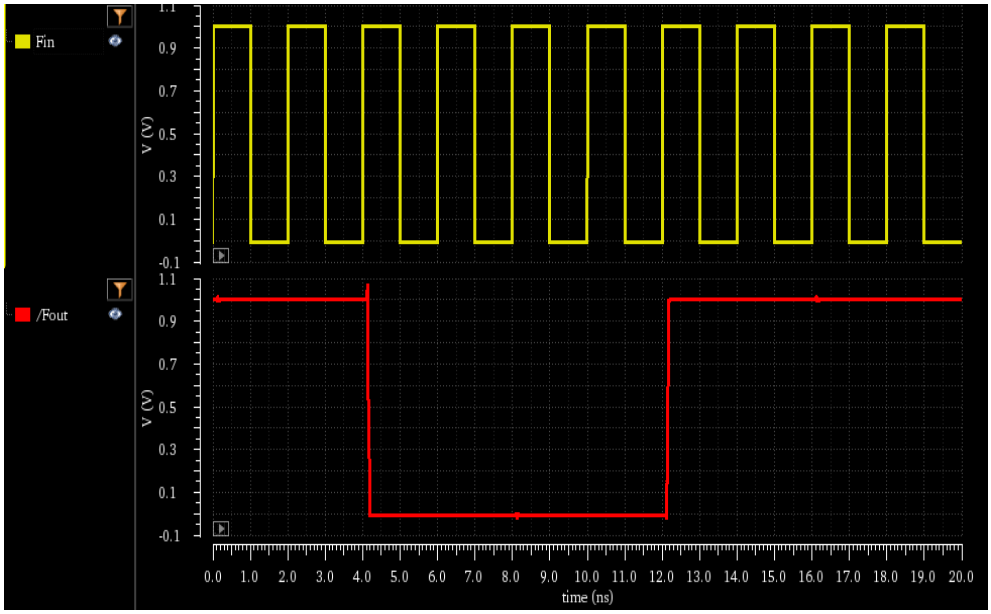

Figure 15: Frequency divider plot

From the Above result we can see that frequency divider by 8 is working fine and its divides the input frequency by 8 times.

6 Design procedure for the PLL

1. Find K_{VCO} from the simulation.

   From simulation we get

   $$\boxed{K_{VCO} = 4.16 \text{ GHz}}$$

2. Choose the desired phase margin ϕ_m and find the value of b

   We choose desired phase margin $\phi_m = 65°$

   Now from the equation ,

   $$b = 2(tan^2\phi_m + tan\phi_m\sqrt{1 + tan^2\phi_m}) \tag{1}$$

   $$\boxed{\text{b} = 19.35}$$

3. Find the $\omega_{u,Loop}$ and ω_Z

$$\omega_{u,Loop} = \frac{2\pi F_{ref}}{20} = \frac{2\pi \times 2.5 \times 10^8}{20} = 2\pi[12.5 \times 10^6] \text{ rad}$$

$$\omega_Z = \frac{\omega_{u,Loop}}{\sqrt{b+1}} = 2\pi[3.35 \times 10^6] \text{ rad}$$

4. Select I_o and C_1 such that below equation is satisfied

$$\frac{K_{VCO}}{N} I_o = \frac{(b+1)^{\frac{3}{2}}}{b} C_1 \omega_Z^2 \tag{2}$$

By solving the above equation we get,

$$\frac{I_O}{C_1} = 4.062 \times 10^6$$

$$\text{if, } I_O = 40\ \mu A$$

$$\text{Than , } \boxed{C_1 = 9.85pF}$$

5. Find the value of C_2 and R

$$\text{b} = \frac{C_1}{C_2} = 19.35$$

$$C_2 = \frac{C_1}{b} = 0.508 \text{ pF}$$

$$\boxed{C_2 = 0.508 \text{ pF}}$$

Now for R,

$$\omega_Z = \frac{1}{RC_1}$$

$$\text{R} = \frac{1}{2\pi \times 3.35 \times 10^6 \times 9.85 \times 10^{-12}}$$

$$\boxed{\text{R} = 4.823 \text{ K}\Omega}$$

Now we will design the Loop filter by using the above values of R , C_1 and C_2 .

7 Results

The PLL Block we design is shown below

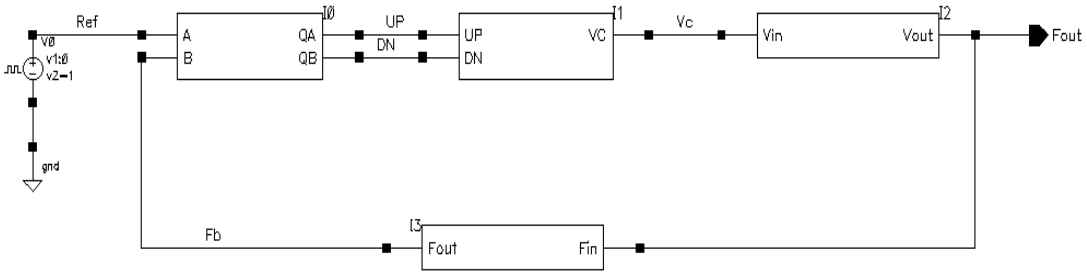

Figure 16: PLL Block Representation

Reference signal plot

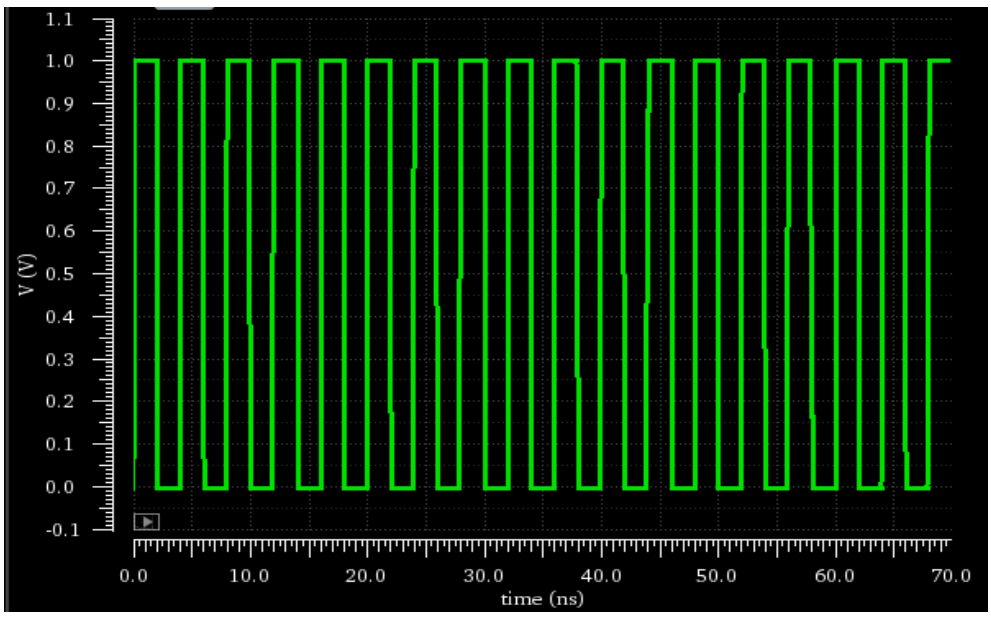

Figure 17: Reference input signal

Above plot is reference signal plot, our input frequency is 2.5×10^8. So the time period of the signal is 4 ns.

Feedback signal plot

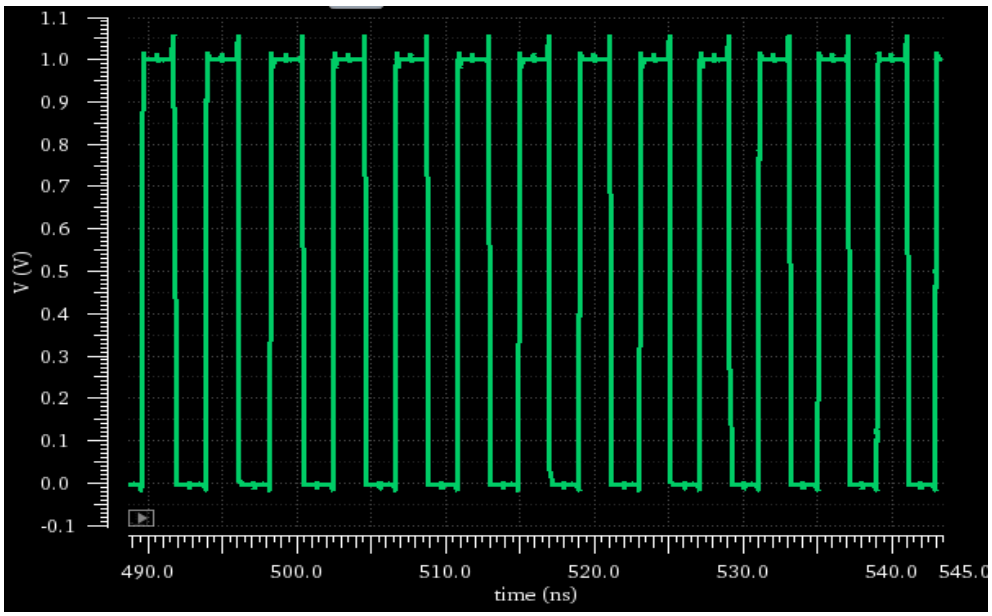

Figure 18: Feedback signal plot

Above plot is the feedback signal plot and it is output of frequency divider and it goes into the input terminal of PFD , which measures the difference between the input and feedback phase and frequency.

Output signal plot

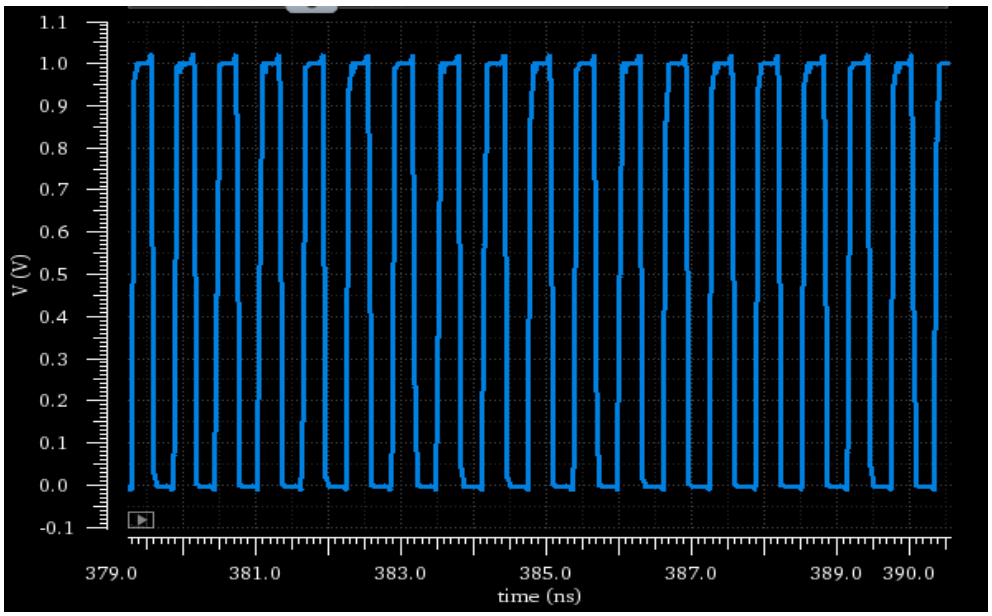

Figure 19: output signal plot

Above plot is the output signal plot, it is the output of VCO.

Control voltage V_C plot

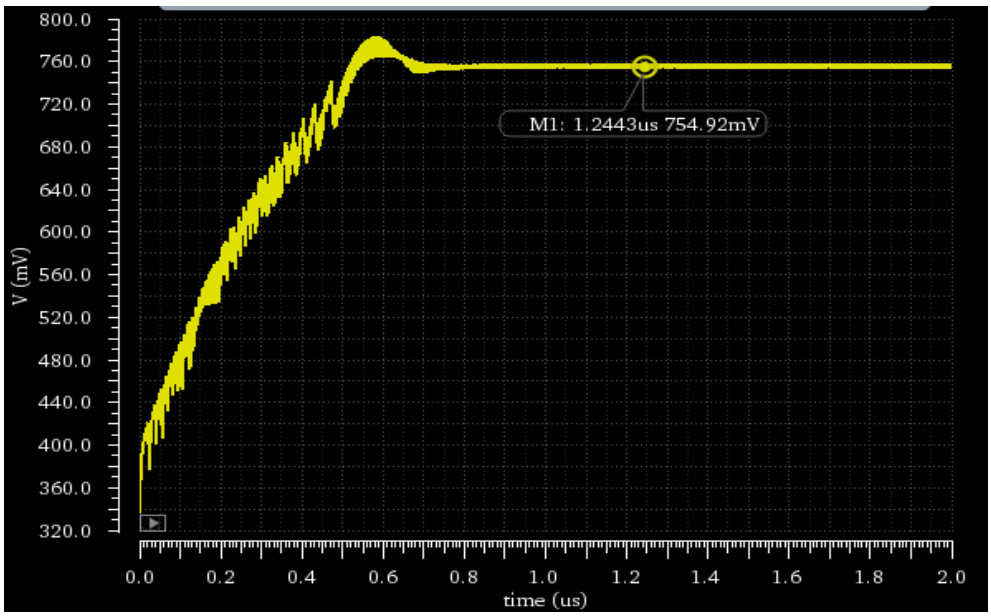

Figure 20: Control voltage V_C plot

It is the plot of control voltage V_C , Initially we seen that it is charging and at some point of time it will constant. For PLL the control voltage need to lock the PLL is 755.97 mV as we have seen above and from the plot we get the V_C is 754.92 mV .

Output frequency lock plot

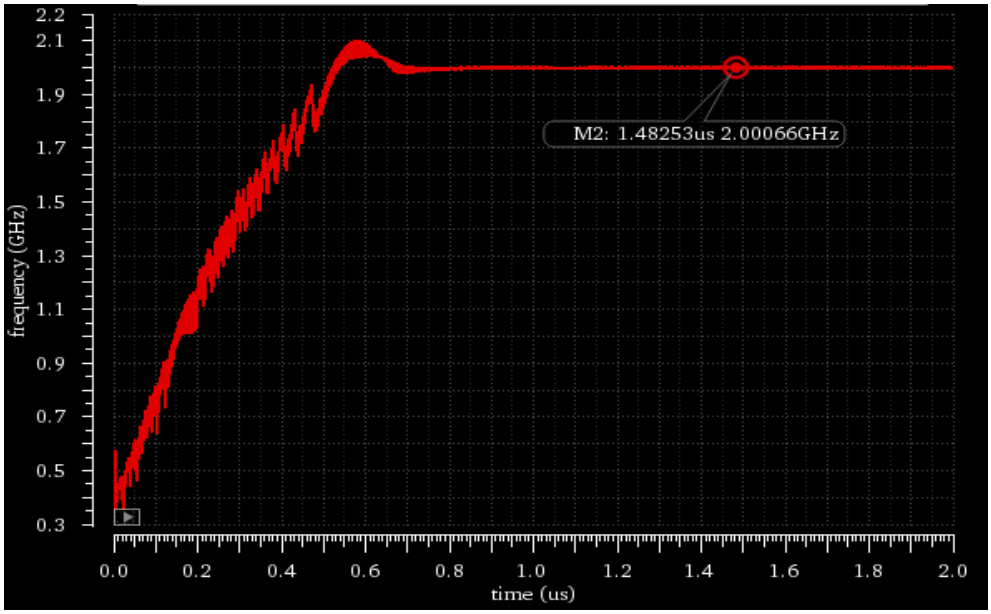

Figure 21: Output Frequency Lock at 2 GHz

Above plot shows that our PLL is working fine it will lock at our output frequency of 2 GHz.

8 Conclusion

In this course project we gain the hands-on experience on PLL design . For designing PLL we use TSMC 65nm technology for implementing the circuits. we learned to design various blocks of PLL , First we work on phase frequency detector, charge pump , loop filter , VCO and frequency divider.

And we also implement D-flip flop , NAND gate , Invertor for implementation of PFD and frequency divider. And also implement voltage buffer circuit used in charge pump.

9 Acknowledgement

I would like to thanks Dr. Mahendra Sakare sir for giving this course project and guidance during this project and also thanks to Mayank kumar singh for their guidance. I would also like to thanks IIT Ropar for providing the cadence virtuoso TSMC 65 nm License.

10 References

[1] P. K. Hanumolu, M. Brownlee, K. Mayaram and Un-Ku Moon, "Analysis of charge-pump phase-locked loops," in IEEE Trans. on Circuits and Syst. I: Regular Papers, vol. 51, no. 9, pp. 1665-1674, Sept. 2004.

[2] H. R. Rategh, H. Samavati and T. H. Lee, "A CMOS frequency synthesizer with an injection-locked frequency divider for a 5-GHz wireless LAN receiver," in IEEE J. of Solid-State Circuits,vol. 35, no. 5, pp. 780-787, May 2000.

[3] Behzad Razavi, "Design of CMOS Phase-Locked Loops: From Circuit Level to Architecture Level" , Cambridge University Press, 2020.

[4] H. M. S. Fazeel, L. Raghavan, C. Srinivasaraman and M. Jain, "Reduction of Current Mismatch in PLL Charge Pump," 2009 IEEE Computer Society Annual Symposium on VLSI, Tampa, FL, USA, 2009, pp. 7-12, doi: 10.1109/ISVLSI.2009.45.