Indian Institute of Technology Kharagpur

AUTUMN Semester, 2019
COMPUTER SCIENCE AND ENGINEERING

Computer Organization Laboratory

Assignment-9: Verilog Design of Floating Point Adder

Full Marks: 20

Time allowed: 6 hours

INSTRUCTIONS: Make one submission per group in the form of a single zipped folder containing your Verilog source code files(s) and Verilog testbench(es). Name your submitted zipped folder as `Assgn_9_Grp_<Group_no>.zip` and (e.g. `Assgn_9__Grp_25.zip`). Inside each submitted source and testbench files, there should be a clear header describing the assignment no., problem no., semester, group no., and names of group members. Liberally comment your code to improve its comprehensibility.

1. [**IEEE-754 Single-precision Floating Point Adder Circuit**] Design (using Verilog), simulate (using a proper Verilog testbench), and synthesize an **IEEE-754 single-precision floating point adder circuit**. Pipeline the circuit by inserting pipeline registers at appropriate places (i.e., an addition will now take multiple clock cycles to complete). You can consider having an input control signal termed `start` to indicate the start of the addition operations. A suggested interface of your design is:
`module FP_adder_32 (input clk, input rst, input start, input [31:0] a, input [31:0] b, output reg [31:0] sum);`, where the signal names suggest their functionality. You are free to modify the interface as you feel appropriate. **No need to implement the design on a FPGA for demonstration.** (20 marks)