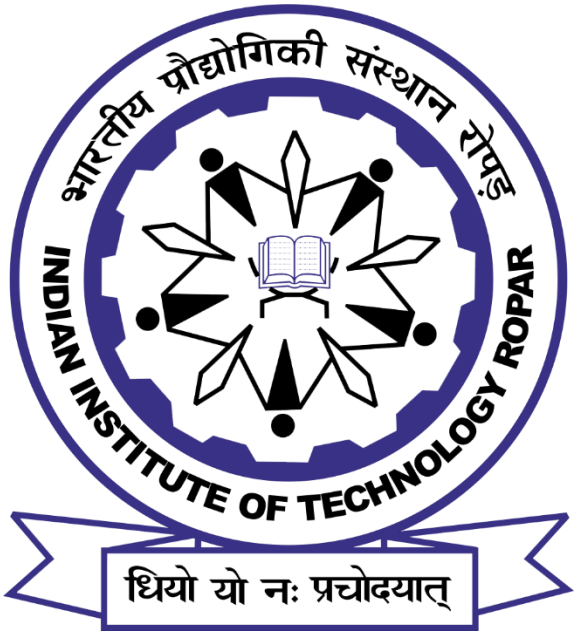
Analog Circuits EE301



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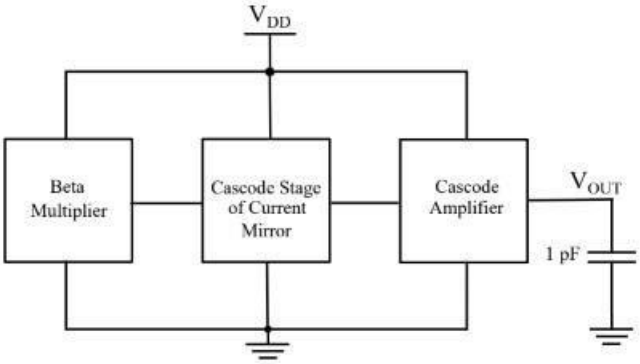
Entry Number: 2022EEB1201
Submission Date: 9th Nov 2024
Course Instructor: Dr. Mahendra Sakare

Aim:

To design Beta Multiplier, Cascode Current Mirror and Cascode Amplifier (in 180nm and 22 nm technology) in LtSpice and Magic.

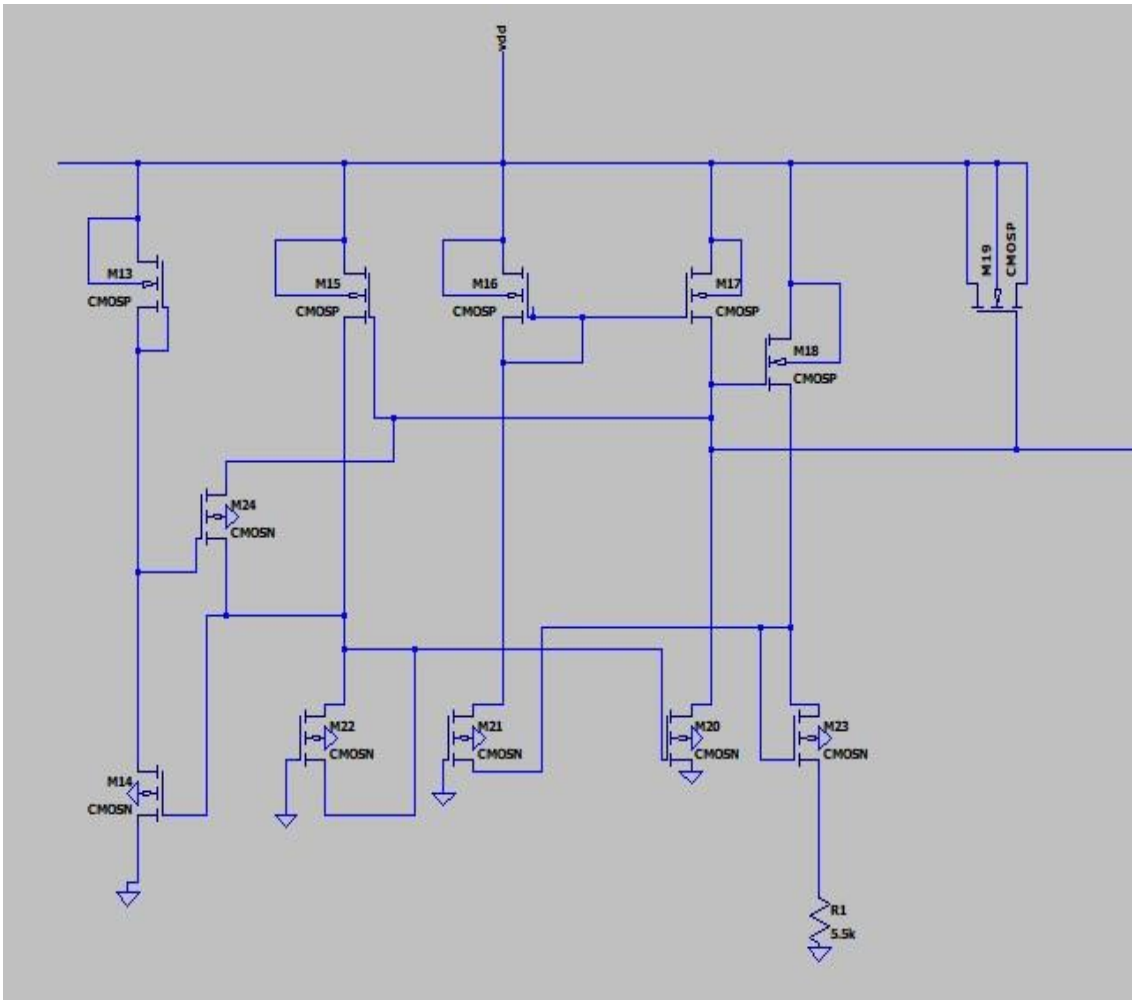
LtSpice Simulation:

The overall block diagram of cascode amplifier with other blocks:

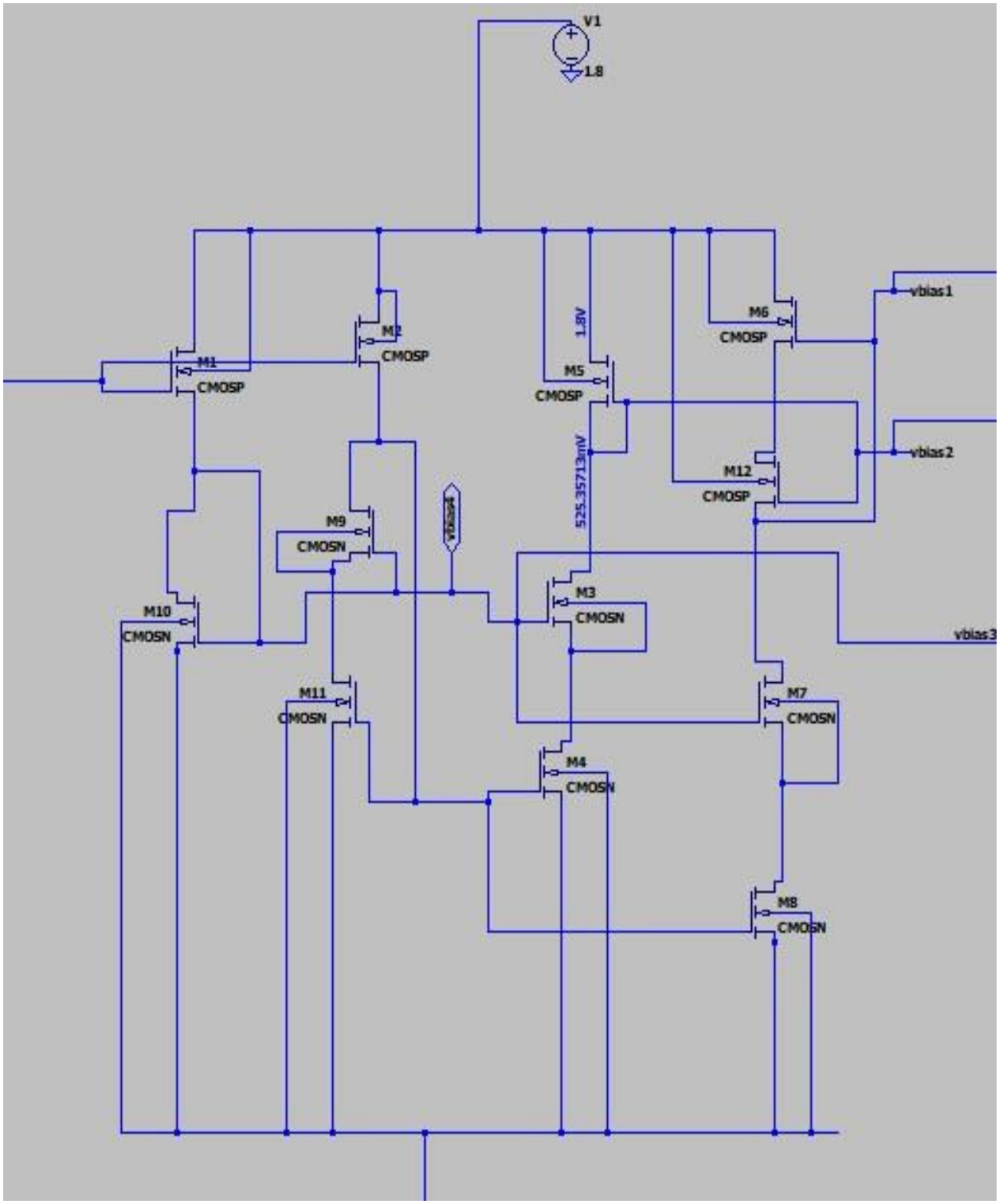


A) 180 nm Technology: Simulation

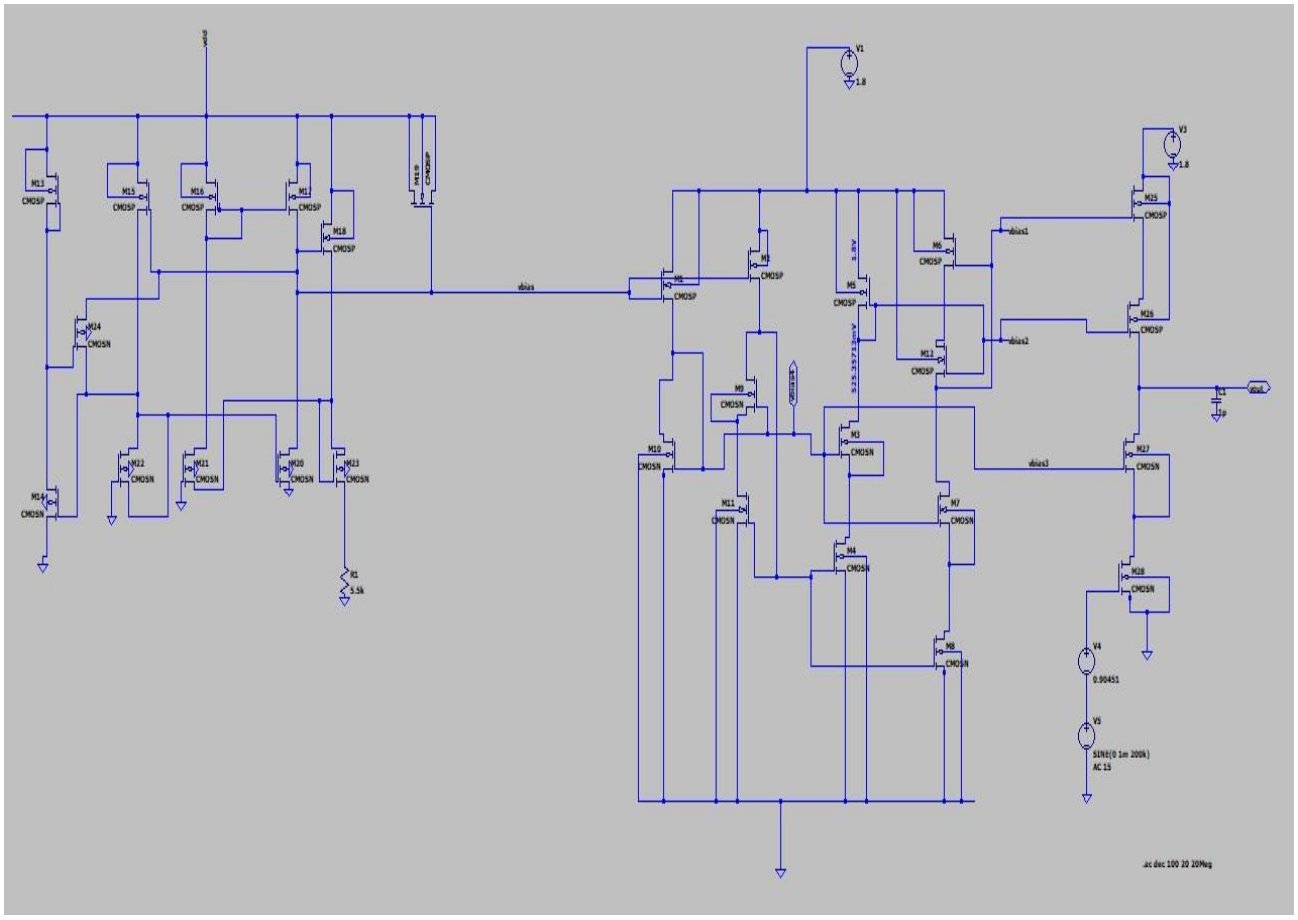
The following images show circuits made in LtSpice for Beta Multiplier, Cascode Current Mirror and Cascode Amplifier (180nm). W/L were set according to the given values in Beta Multipier and Cascode Current Mirror. For Cascode Amplifier, this ratio was found by calculations shown in next section.



Beta Multiplier



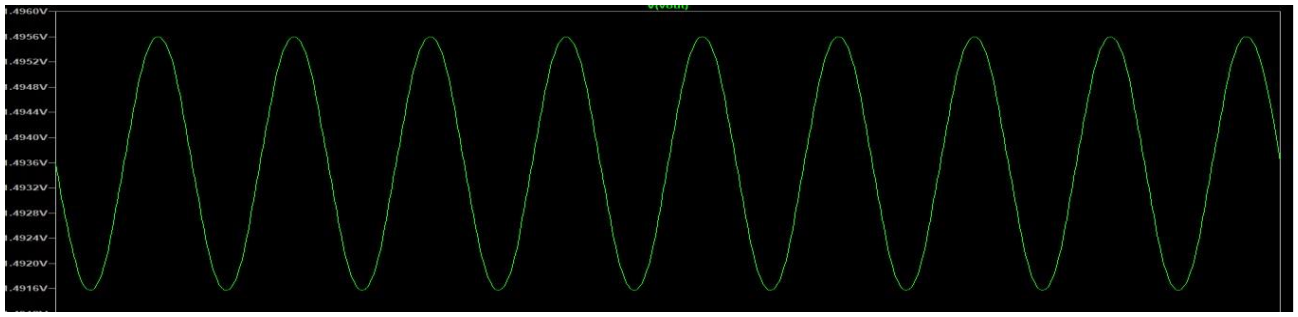
Cascode Current Mirror



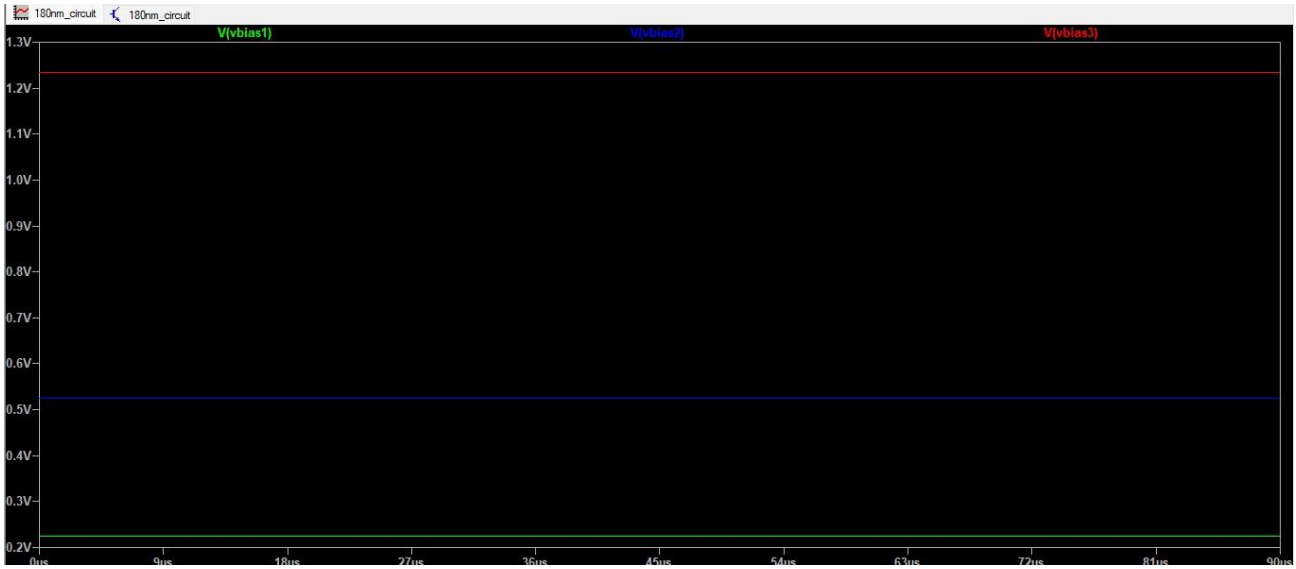
Cascode Amplifier

Output

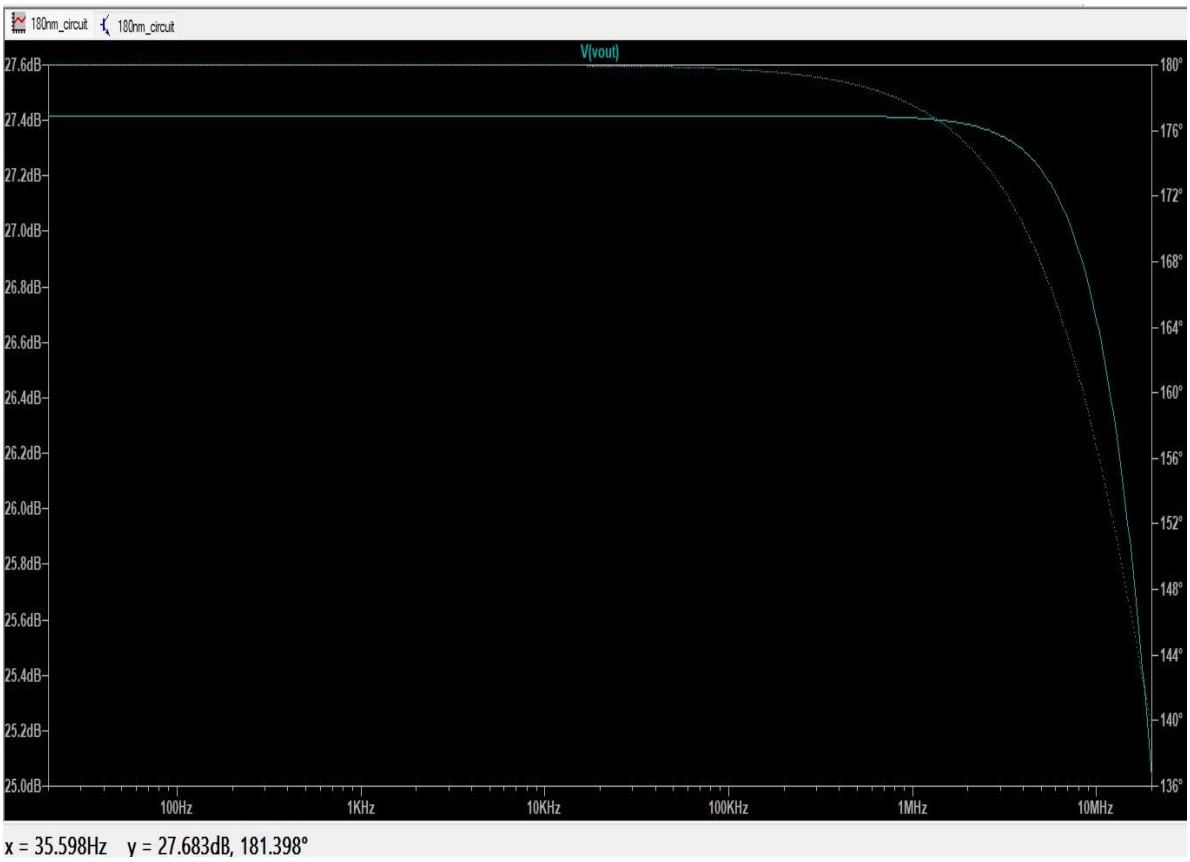
The Simulation outputs obtained were:



Output Waveform



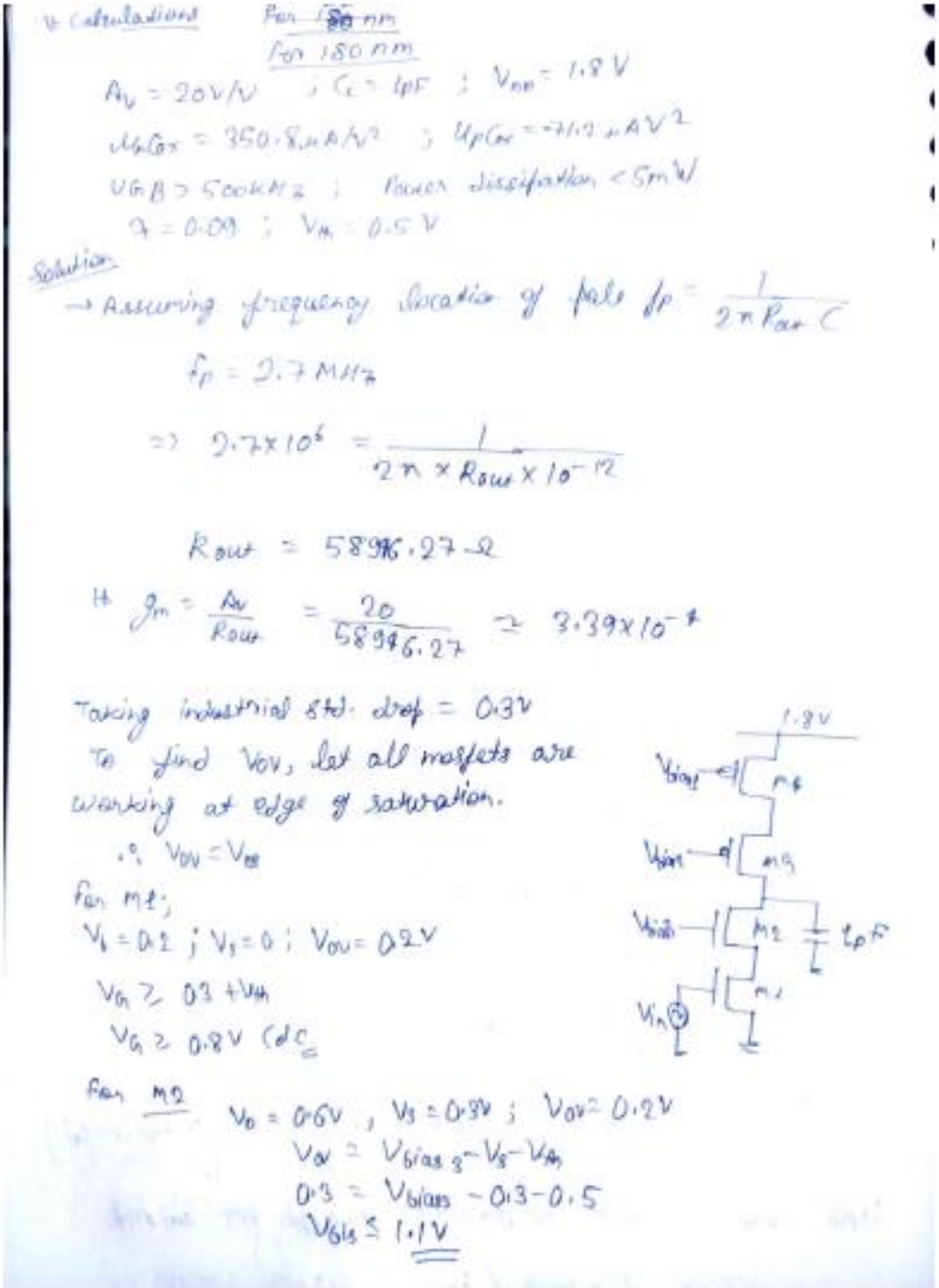
Vbias Values



Frequency Response

Calculations

The following calculations were done to find W/L ratio for Cascode Amplifier.



Calculations For 180 nm

$A_v = 20 V/V$; $C_L = 1pF$; $V_{DD} = 1.8V$

$\mu_n C_{ox} = 350.8 \mu A/V^2$; $\mu_p C_{ox} = 71.9 \mu AV^2$

$V_{GB} > 500mV$; Power dissipation $< 5mW$

$\gamma = 0.09$; $V_{th} = 0.5V$

Solution

→ Assuming frequency location of pole $f_p = \frac{1}{2\pi R_{out} C}$

$f_p = 2.7 MHz$

$\Rightarrow 2.7 \times 10^6 = \frac{1}{2\pi \times R_{out} \times 10^{-12}}$

$R_{out} = 58996.27 \Omega$

$g_m = \frac{A_v}{R_{out}} = \frac{20}{58996.27} \simeq 3.39 \times 10^{-4}$

Taking industrial std. drop = 0.3V

To find V_{OV}, let all mosfets are working at edge of saturation.

$\therefore V_{OV} = V_{DS}$

For M1;

$V_t = 0.2$; $V_s = 0$; $V_{OV} = 0.2V$

$V_G \geq 0.3 + V_{th}$

$V_G \geq 0.8V$ (dc)

For M2 $V_D = 0.6V$, $V_S = 0.3V$; $V_{OV} = 0.2V$

$V_{OV} = V_{bias\,3} - V_S - V_{th}$

$0.3 = V_{bias} - 0.3 - 0.5$

$V_{bias} \leq 1.1V$

Now $g_m = \mu_n C_{ox} \frac{W}{L} \times V_{ov}$

$3.39 \times 10^{-4} = 350.8 \times 10^{-6} \times \left(\frac{W}{L}\right) \times (0.3)$

$\left(\frac{W}{L}\right)_{nmos} = 3.22$

Now same I_D flows through all mosfets:

$I_D = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_p \times V_{ov}^2 (1 + \lambda V_{ds})$ — ① $V_{ov} = V_{eff}$

$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) \times V_{ov}^2 (1 + \lambda V_{DS})$ — ②

equating ① and ②

$\left(\frac{W}{L}\right)_{pmos} = \frac{3.39 \times 10^{-4}}{-35.6 \times 10^{-6}} \simeq 9.522$

→ Power dissipation $= V_{DD} \times I_D$

$= 1.8 \times [5.2 \times 10^{-5}] = 9.4 \times 10^{-5} < 5mW$

If for V_{Gias2}, V_{Gias1}; $V_{ov} = 0.3V$

for m3; $V_D = 1.2V$; $V_S = 1.5V$

$|V_{GS}| - |V_{th}| \leq V_{DS}$

$|V_{Gias2} - V_S| - |-0.5| \leq |0.3|$

$|V_{Gias2} \geq 1.7V$

If for m4; $V_D = 1.5V$; $V_S = 1.8V$

$V_{Gias} \geq 1.4V$

for NMOS; $L = 180nm$; $W = 180 \times 3.22 nm$

$W = 579.6 nm$

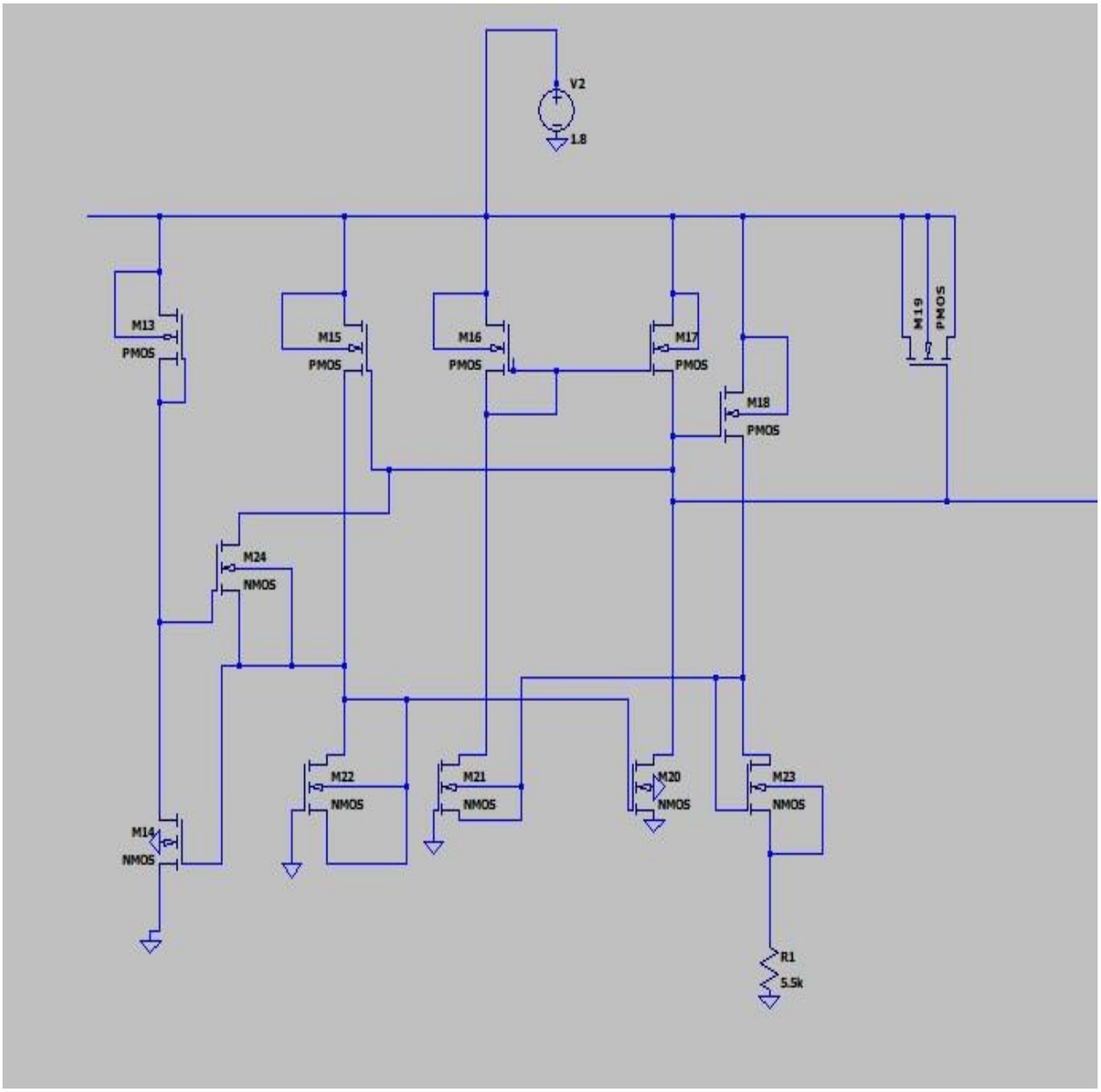
$\frac{W}{L} = 3.22$

for PMOS; $L = 180nm$; $W = 180 \times 9.522$

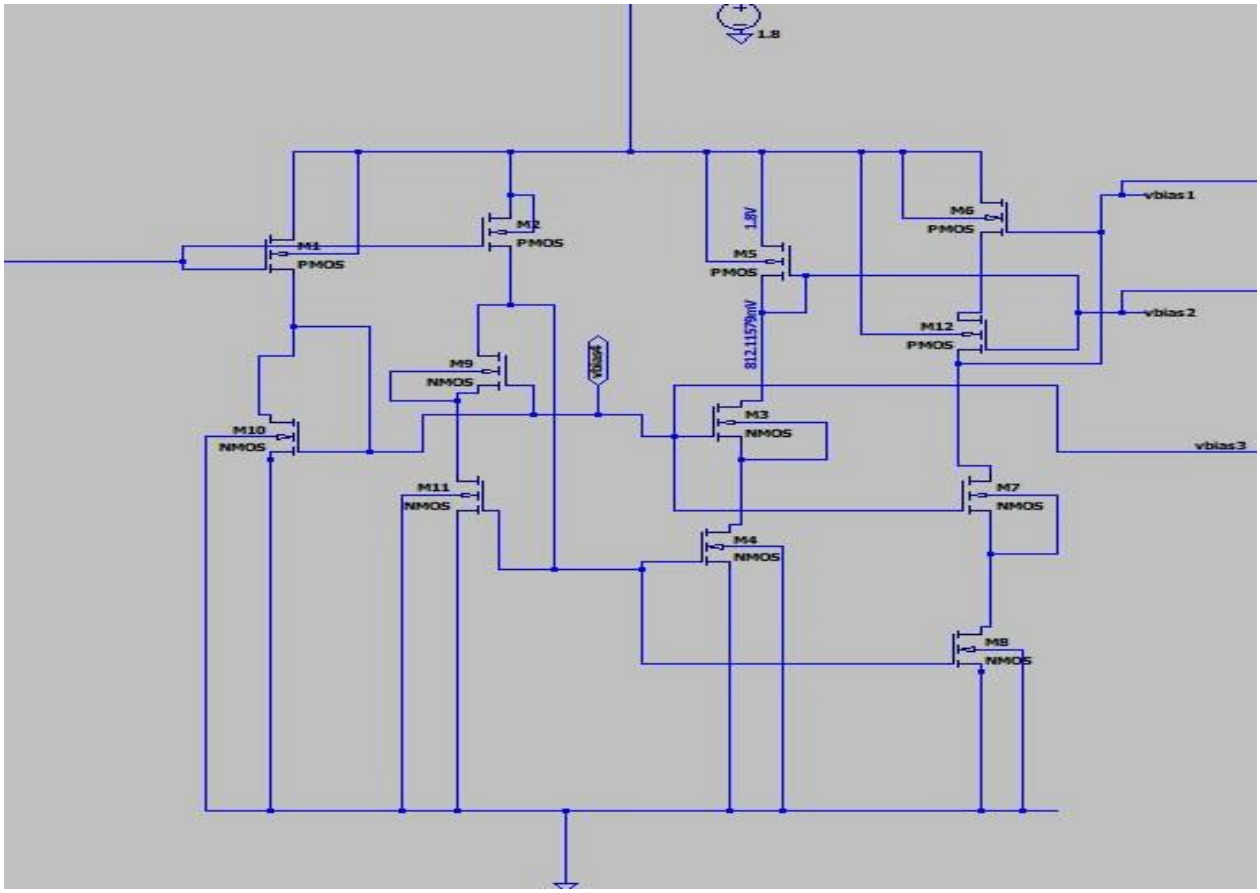
$W = 1713.6 nm$

B) 22 nm Technology: Simulation

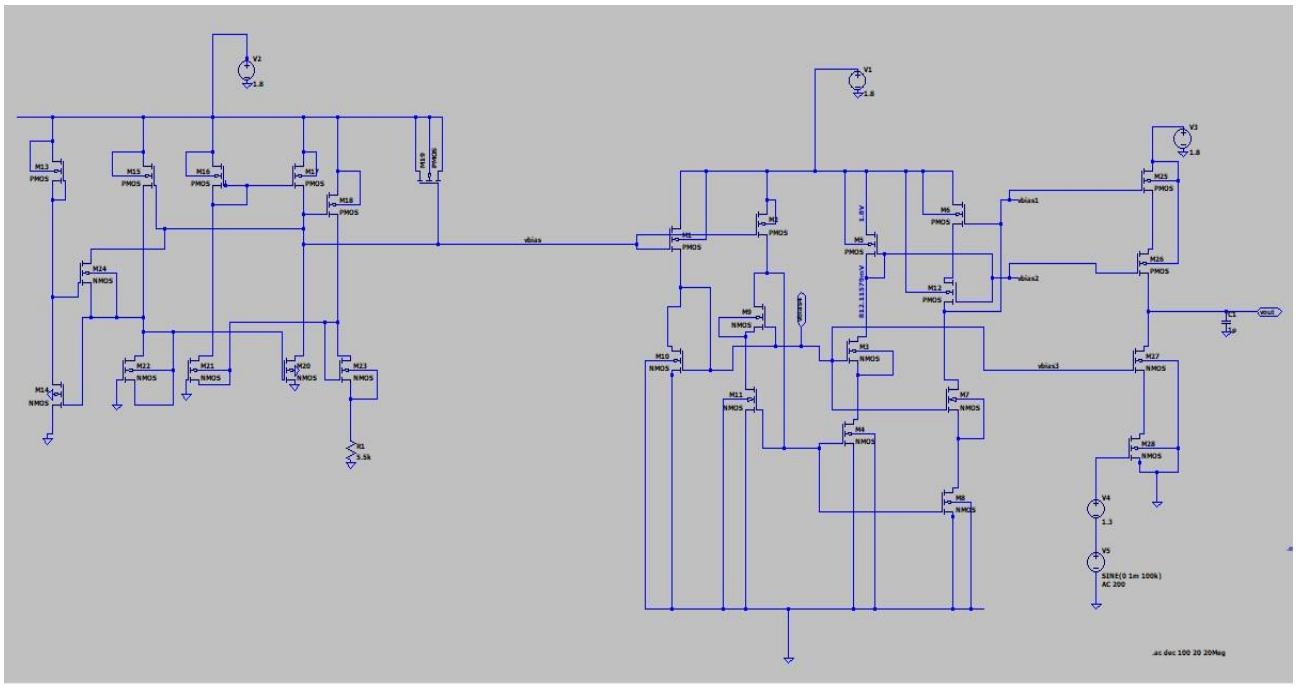
The following images show circuits made in LtSpice for Beta Multiplier, Cascode Current Mirror and Cascode Amplifier (22nm). W/L were set according to the given values in Beta Multipier and Cascode Current Mirror. For Cascode Amplifier, this ratio was found by calculations shown in next section.



Beta Multiplier



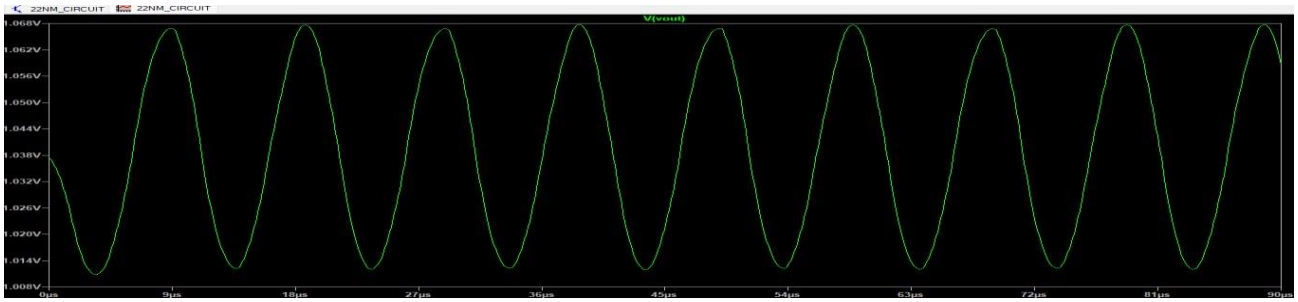
Cascode Current Mirror



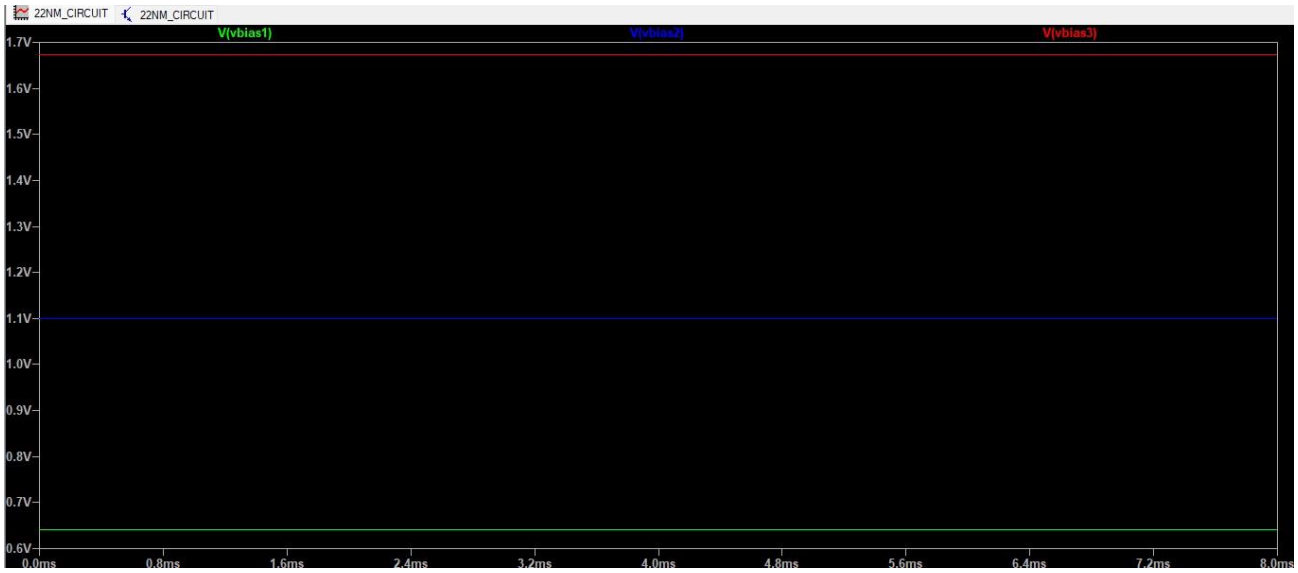
Cascode Amplifier

Output

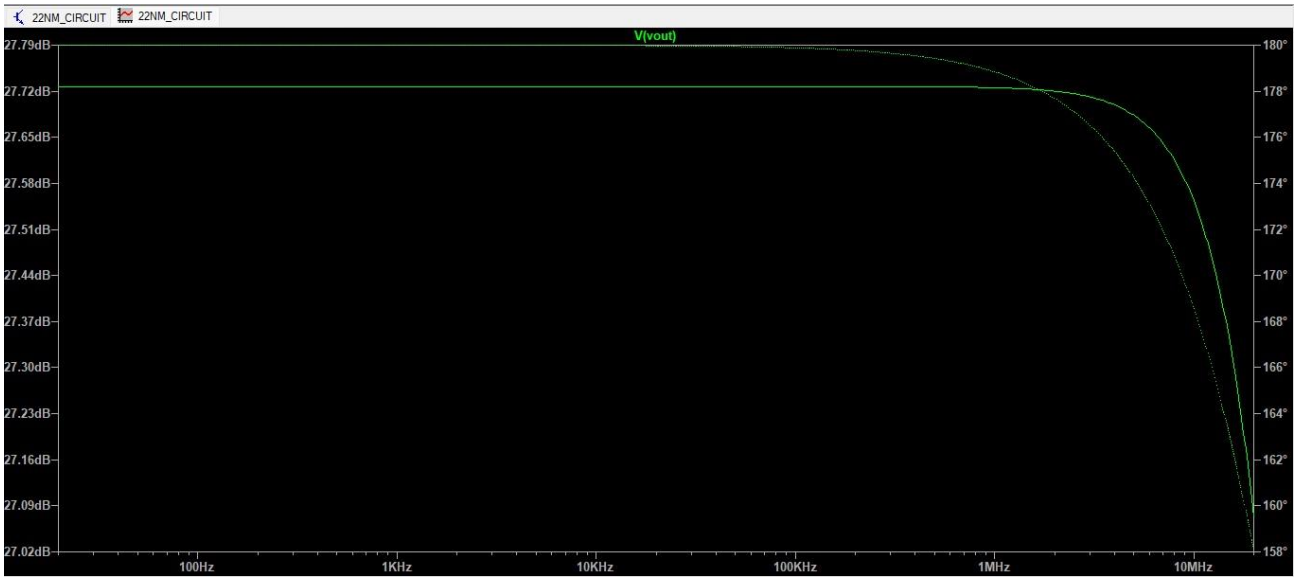
The Simulation outputs obtained were:



Output Waveform



Vbias Values



Frequency Response

Calculations

The following calculations were done to find W/L ratio for Cascode Amplifier.

For 22nm : Similar calculations.

Given $A_v = 20 V/V$; $V_{DD} = 1.8V$; $C_L = 1pF$

Assumed $|V_{TH}| = 0.4V$; $\mu_n C_{ox} = 100 \mu A/V^2$

$\mu_p C_{ox} = 50 \mu A/V^2$

And frequency location of pole $f_p = 2.7 MHz$

$$\rightarrow R_{out} = \frac{1}{2\pi f_p C_L} = 58946.27\ \Omega$$

$$\rightarrow g_m = \frac{A_v}{R_{out}} = \frac{20}{58946.27} = 3.39 \times 10^{-7}$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{ov})^2$$

using $g_m = \mu_n C_{ox} \frac{W}{L} \times V_{ov}$

$$0.000399 = 100 \times 10^{-6} \times \left(\frac{W}{L}\right) \times (0.3V)$$

$$\left(\frac{W}{L}\right)_{nmos} = 11.309$$

$$I_D = \frac{g_m \times V_{ov}}{2} = 5.085 \times 10^{-5} A$$ (2 neglected)

↳ As same current is flowing through M3 and M4

$$I_D = \frac{1}{2} \times \mu_p C_{ox} \left(\frac{W}{L}\right)_{PMOS} \times V_{ov}^2$$

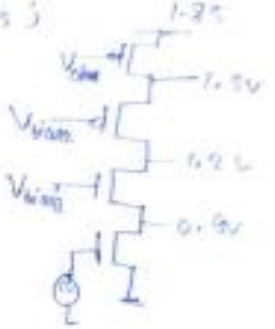
$5.085 \times 10^{-5} = \frac{1}{2} \times 50 \times 10^{-6} \times \left(\frac{W}{L}\right)_{PMOS} \times (0.3)^2$

$\left(\frac{W}{L}\right)_{PMOS} = 22.6$

Power dissipated $= V_{DD} \times I_D = 1.8 \times 5.085 \times 10^{-5}$

$= 9.153 \times 10^{-5} W \ (< 5nW)$

Finding ranges of V_{bias1}, V_{bias2}, V_{bias3} & V_S;



Assuming all at a saturation.

① M1: $V_D = 0.9V$; $V_S = 0V$; $V_{TH} = 0.4V$

$V_G - V_S - V_{TH} = V_D - V_S$

$V_G - 0 - 0.4 = 0.9 - 0$

$V_G = 0.9 + 0.4 = 1.3V$

② M2: $V_D = 1.2V$; $V_S = 0.9V$

$V_{bias} - 0.9 - 0.4 = 1.2 - 0.9$

$V_{bias3} = 0.9 + 0.4 + 0.3$

$= 1.7V$

③ M3: $V_{GS} - V_{TH} \geq -0.3$

$V_{bias} - 1.2 - 0.4 \geq -0.3$

$V_{bias} \geq -0.3 + 0.8$

$V_{bias2} \geq 0.5V$

④ M4: $V_{GS} - V_{TH} \geq -0.3$

$V_{bias} - 1.8 + 0.4 \geq -0.3$

$V_{bias} \geq -0.3 + 1.4 \geq 1.1V$

W and $L = 22nm$

for NMOL; $L = 22nm$; $W = 22 \times 11.309 \simeq 248.8$

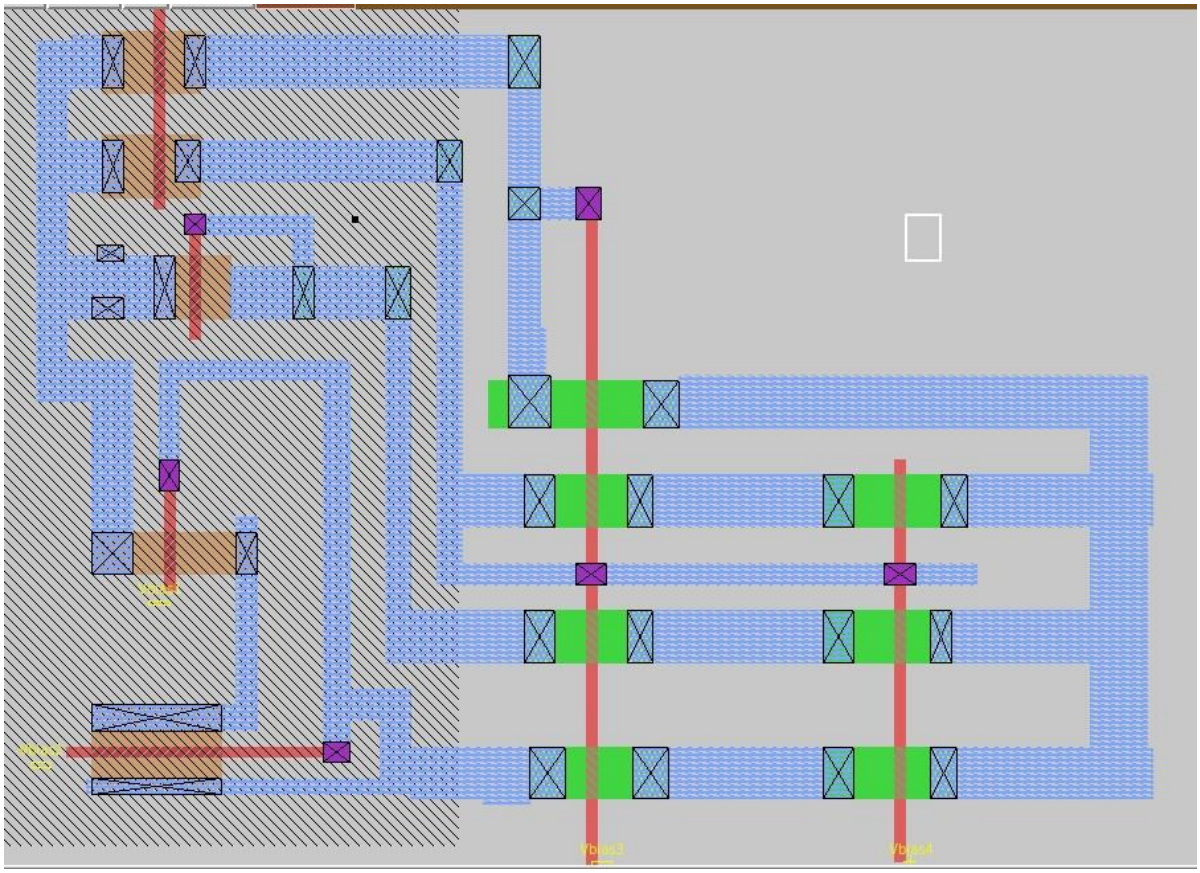
$\left(\frac{W}{L}\right) = 11.30$

for PMOS; $L = 22nm$; $W = 22 \times 22.6 = 497.2nm$

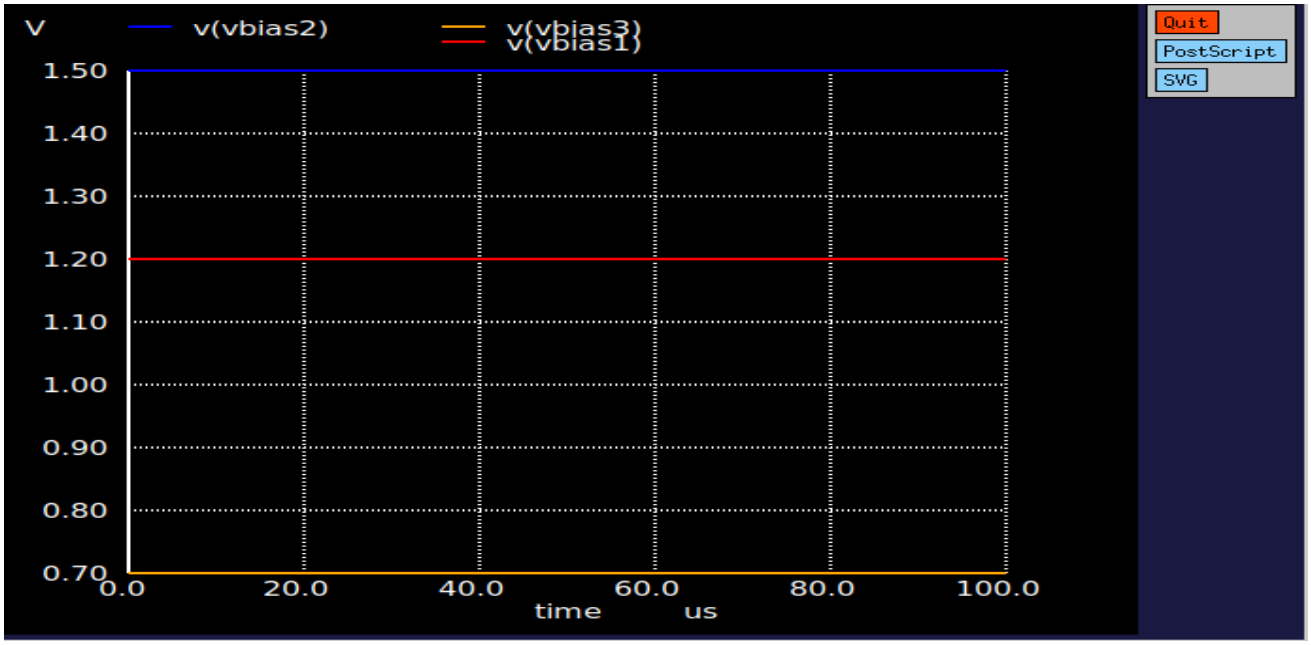
Thus the given simulation satisfies all the requirements.

Magic Layout (for 180nm Technology):

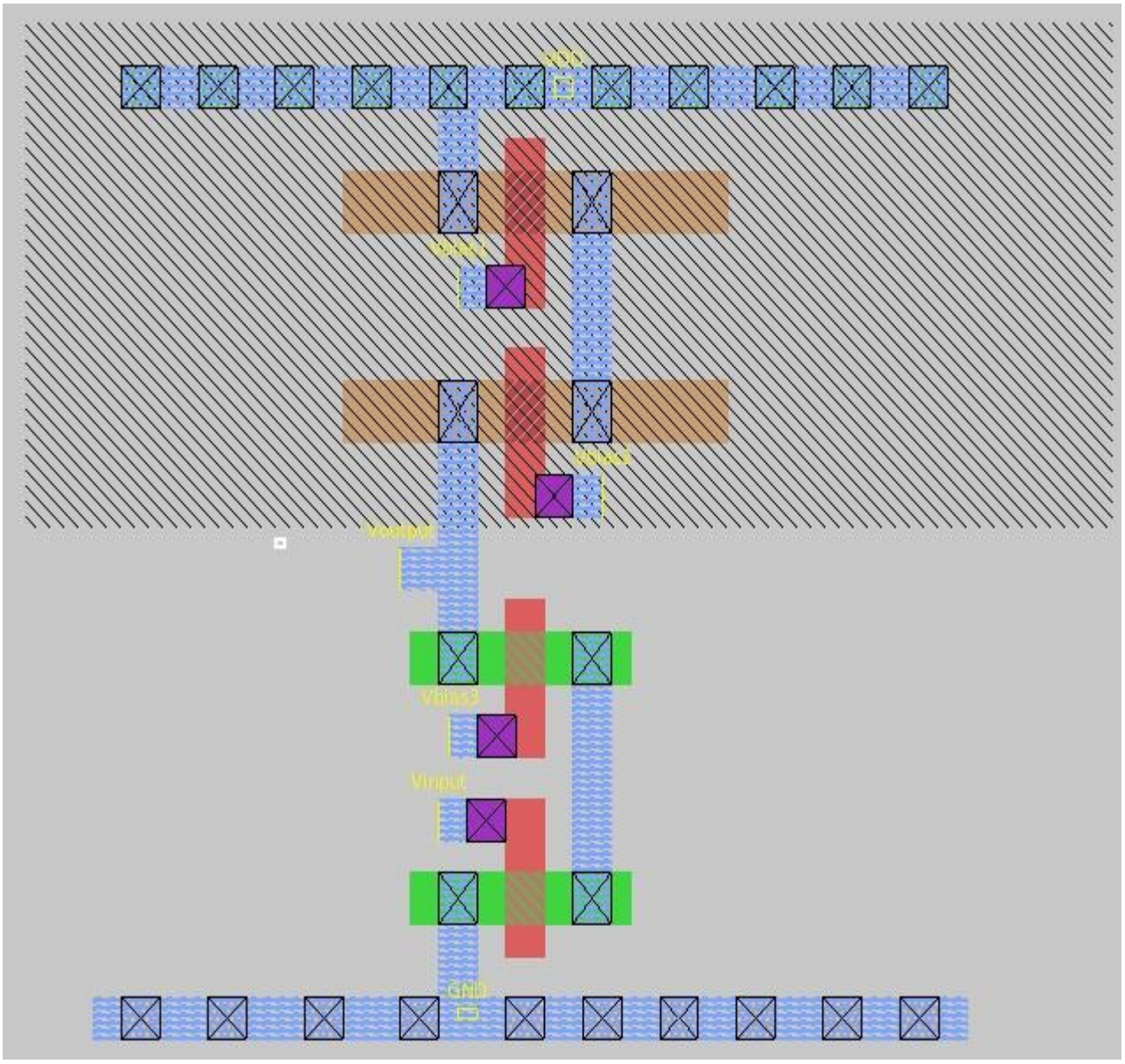
The Layout is made using the W/L values calculated earlier.



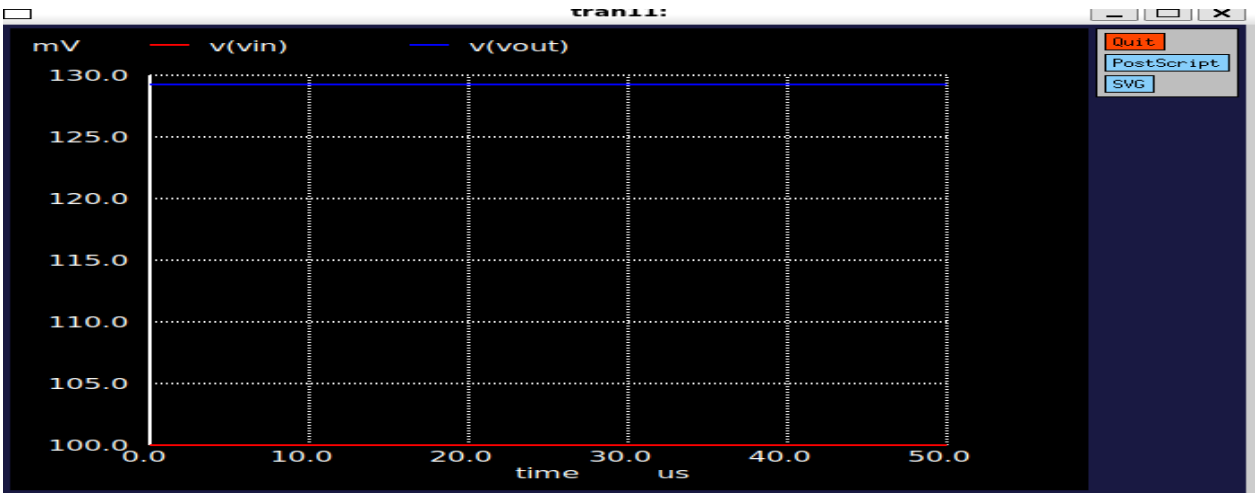
Cascode Current Mirror



OUTPUT OF CURRENT MIRROR



Cascode Amplifier



Specifications:

- Required gain = 20log(20) dB = 26.02dB. The Simulation gave a gain of 27.4 dB and 27.2 dB gain for 180nm and 22nm technology respectively.
- Power Dissipation should be less than 5mW. We obtain it as 0.094mW and 0.091mW for 180nm and 22nm technology for same Vdd applied respectively.
- Unity Gain Bandwidth (UGB) must be greater than 500KHz. We got UGB as 30.22 MHz and 210 MHz for 180nm and 22nm technology respectively.
- The frequency response of both simulations is of low pass filter. Thus all the required specifications are satisfied.

Detailed comparison of 180nm and 22nm technology nodes:

- **Power Consumption**: In 22nm technology, both the biasing voltages (Vbias) and the currents required for operation are generally lower than those in 180nm technology. This reduced power requirement results in significantly lower power consumption for 22nm devices compared to those fabricated at 180nm. Lower power consumption is a major advantage, especially for applications where energy efficiency is a priority, such as in portable devices and large-scale data centers.
- **Unity Gain Bandwidth and Cut-Off Frequency**: The unity gain bandwidth, which is an indicator of how fast a transistor can operate, is notably higher in 22nm technology. This translates to a higher cut-off frequency in circuits designed with 22nm transistors, allowing them to switch at faster rates than those made with 180nm technology. This makes 22nm technology preferable for high-speed applications and circuits that require fast response times, such as in RF and high-frequency digital circuits.
- **Device Density and Performance**: 22nm MOSFETs are approximately eight times smaller than 180nm MOSFETs, enabling significantly higher transistor density on a single chip. This increased packing density allows for more complex and capable circuits within the same chip area, leading to improved performance in terms of processing power and functionality. For example, a processor with more cores or larger cache can be implemented within the same area, enhancing performance in applications ranging from mobile devices to servers.
- **Challenges in Design and Cost Implications**: Despite the performance benefits, 22nm technology presents increased challenges in layout design due to the smaller MOSFET sizes. Designing these layouts requires greater precision and often necessitates more advanced fabrication techniques, such as double-patterning lithography. These complexities can drive up the design and manufacturing costs, as well as require specialized design expertise. Additionally, small feature sizes can make devices more susceptible to variability, impacting yield and requiring additional process controls.

Analysis and Inferences

1. **Gain**: Both technologies met the required gain value (26.02 dB), achieving practical values of 27.4 dB and 27.2 dB for 180nm and 22nm, respectively. This close alignment confirms the accuracy of the amplifier design.
2. **Power Dissipation**: Although the theoretical requirement was to stay below 5mW, the simulated values for power dissipation were much lower, with 0.098mW for 180nm and an even lower 0.091mW for 22nm technology. This indicates a strong efficiency for both designs, with the 22nm design being particularly power-efficient due to its smaller scale.

3. **Unity Gain Bandwidth (UGB)**: The theoretical UGB requirement (>500kHz) was easily surpassed in both designs, achieving practical values of 30.22 MHz for 180nm and 210 MHz for 22nm technology. This suggests superior high-frequency performance, particularly for the 22nm technology, which may be advantageous in high-speed applications.

Conclusion:

Thus we simulated Beta Multiplier, Cascode Current Mirror and Cascode Amplifier (for both 180nm and 22nm Technology) on LtSpice. The simulation results obtained were close to the theoretical ones and satisfied all the required performance specifications. We also designed the layout for Cascode Current Mirror and Cascode Amplifier on Magic (only for 180nm Technology).

Finally, we compared both 180nm and 22nm Technology based on LtSpice Simulation and Magic Layout.