Low-Power Bootstrapped Sample and Hold Circuit for Analog-to-Digital Converters

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Abstract*—In this paper, a modified low-power bootstrapped sample and hold (S/H) circuit is proposed. The effect of the proposed modified low-power bootstrapped sample and hold (S/H) circuit appears in the medium and high-frequency applications in which it reduces the power consumption without affecting the signal-to-noise and distortion ratio (SNDR). The proposed modified low-power bootstrapped sample and hold (S/H) circuit is based on eliminating the multiplier circuit which is responsible for keeping the gate-source voltage of the sampling transistor constant and replaced it with a PMOS transistor which performed the same job. In addition to that, it is based on using the transmission gate as the sampling transistors which avoid the degradation of the signal-to-noise and distortion ratio (SNDR). All the introduced bootstrapped sample and hold (S/H) circuits were simulated using 90nm CMOS technology on LT Spice IV. As a result, the proposed modified low-power bootstrapped sample and hold (S/H) circuit saves 70% to 92% of the power consumption compared with previous work reported in the literature with signal-to-noise and distortion ratio (SNDR) of 57 dB for 7 MHz input frequency signal.

Keywords—ADC; S/H; Transmission gate; Bootstrapped; Bluetooth.

I. INTRODUCTION

Analog-to-digital converter (ADC) is considered as one of the main electronic block in mixed signal applications. It is used in low-frequency applications such as biomedical applications [1][2]. Furthermore, ADC becomes a bottleneck in digital signal processing applications which is medium-frequency applications. Furthermore, it is used in high-frequency applications such as wireless communication [3].

Sample and hold (S/H) circuit is one of the main significant analog building blocks, especially in ADCs. It is the first block of the ADC components in which the input signal seen by the input of the S/H circuit. Therefore, it has a significant effect on the whole ADC performance which in turns will affect the overall system [4].

At the circuit level and in the low voltage operation. If the sum of the absolute value of the PMOS threshold voltage and that of the NMOS is greater than the supply voltage. The conventional analog switches consist of transmission gates may not be fully turned on as they are under a higher voltage operation. The MOSFETs expected to be turned on may have extremely poor conductance and would limit the bandwidth of the circuits. Therefore, a bootstrapped technique is required which has been proved in [5].

The accuracy of the S/H circuit depends mainly on the on-resistance of the sampling switch which will affect the switch linearity. The bootstrapped S/H circuit keeps the gate-source voltage of the sampling transistor fixed at the supply voltage. This approach keeps the on-resistance small and constant and thus improves the switch linearity and reliability.

The objective of this paper is to propose a modified low-power bootstrapped S/H circuit for medium and high frequency applications. The transmission gate has been used as a switching element. The voltage operation will be low in order to guarantees the device reliability. It's worth noting that different sampling rates affect the signal to noise and distortion ratio (SNDR), speed and power consumption of the S/H circuit and the overall ADC. Section II illustrates the design of bootstrapped sampling MOS switch. Simulation results are presented in section III. Section IV concludes the paper.

II. DESIGN OF BOOTSTRAPPED SAMPLING MOS SWITCH

Bootstrapped circuit is considered the suitable circuit in low voltage operation. It is connected to the sampling transistor in S/H circuits. The aim of the bootstrapped circuit is to make the on-resistance of the sampling transistor small in order to improve the on-conductance between the input and output of the sampling switch. This section will present the proposed modified low-power bootstrapped S/H circuit for medium and high frequency applications. In addition to that, different bootstrapped circuits which are connected to the S/H circuit using transmission gate will be discussed and compared with the proposed circuit. The principle of the first bootstrapped technique is shown in Fig. 1. The single NMOS transistor is represents the sampling transistor switch. In the off-state, the gate is grounded, so the device is in cutoff mode. In the on-state, a constant voltage of (V_{DD}) is applied across the gate-source terminals, and a low on-resistance is formed from drain to source independent of the input signal. If the gate voltage exceeds (V_{DD}) for a positive input signal, none of the terminal-to-terminal device voltages exceeds (V_{DD}) [6].

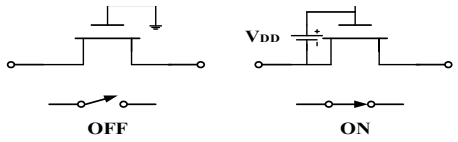

Fig. 1. Bootstrapped MOS switch [6]

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Fig. 2, shows the actual bootstrapped circuit. It operates on a single phase clock Ø that turns the bootstrapped switch M_{11} on and off. When Ø is low, transistors M_7 and M_{10} discharge the gate of M_{11} to ground and thus the bootstrapped circuit in the off phase. In this phase, (V_{DD}) is applied across capacitor C_3 by M_3 and M_{12}. This capacitor will act as the battery across the gate and source during the on phase. The job of M_8 and M_9 is to isolate the switch from C_3 while it is charging. When Ø is high, the gate of M_8 will be pulled down by M_5, allowing charge from the battery capacitor C_3 to flow onto gate G. This turns on both M_9 and M_{11}. M_9 enables gate G to track the input voltage S shifted by (V_{DD}), keeping the gate-source voltage constant regardless of the input signal. For example, if the source S is at (V_{DD}), then gate G is at ($2V_{DD}$); however, ($V_{GS} = V_{DD}$). The body (n-well) of M_8 is connected to its source in order to repress latch up. M_7 and M_{13} are not functionally necessary but to improve the circuit reliability. Device M_7 reduces the (V_{DS}) and (V_{GD}) experienced by device M_{10} when Ø is low. The channel length of M_7 can be increased to further improve its punch through voltage. M_{13} ensures that (V_{GS8}) does not exceed (V_{DD}). M_1, M_2, C_1 and C_2 form a clock multiplier that enables M_3 to charge C_3 during the off phase [6].

The capacitor C_3 must be sufficiently large to supply charge to the gate of the switching device in addition to all parasitic capacitances in the charging path. Otherwise, charge sharing will significantly reduce the boosted voltage according to (2), where C_p is the total parasitic capacitance connected to the top plate of C_3 while it is across the main switching device M_{11} [6].

$$V_G = V_S + (C_3 / (C_3 + C_p))\, V_{DD} \qquad (2)$$

When the bootstrapped switch is off, a C_{ds} capacitor is formed between the drain and the source of the sampling transistor. It couples the input signal to the sampling capacitors which is composed by the drain-source capacitor of the sampling transistor and the routing parasitic capacitance. The coupling effect degrades the high frequency performance because C_{ds} induces unequal charges in the comparison cycles, which results in a dynamic offset. Therefore, two cross coupled metal oxide metal (MOM) capacitors can be used to neutralize the effect. A dummy switch is alternative solution to reduce the coupling effect [4].

The proposed modified low-power bootstrapped S/H circuit is illustrated in Fig. 3. Simply, it is the same as the S/H circuit with bootstrapped circuit shown in Fig. 2 but without the multiplier circuit. The multiplier circuit consists of M_1, M_2, C_1 and C_2. In Fig. 2, the gate of the NMOS transistor M_3 which is responsible for charging the capacitor C_3 is biased by the multiplier circuit. On the other hand, in Fig. 3, the NMOS transistor M_3 is replaced by a PMOS transistor M_3 and its gate is biased by the gate of the bootstrapped switch. M_3 will charge C_3 to (V_{DD}) in the off-sate of the bootstrapped switch, while in the on-state, the stored charge in C_3 will be applied to the gate-source of the bootstrapped switch. Both circuits are make the gate-source voltage of the bootstrapped switch constant and equal to the supply voltage independent of the input signal. This result in small and constant on-resistance of the sampling switch. The main important feature of the proposed modified low-power bootstrapped circuit is the power consumption. It consumes less amount of power compared to the other presented bootstrapped S/H circuit in medium and high frequency applications. In addition to that, the SNDR will not have a degradation even in high frequency application when the input signal is 7 MHz.

A simulation result shows the clock pulses formed on the gate of the sampling transistor M_{11} and the input signal in Fig. 4. Furthermore, it shows a constant gate-source voltage of the sampling switch which independent of the input signal.

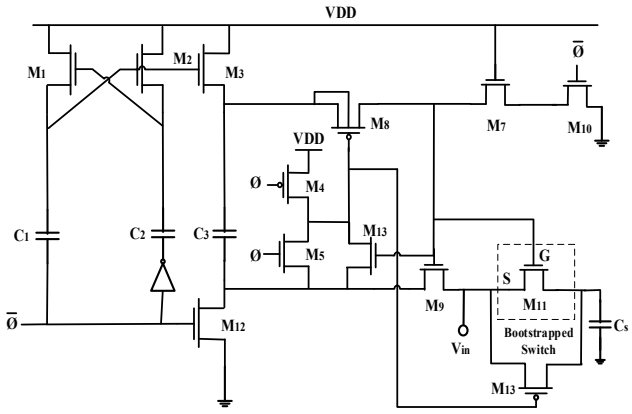

Fig. 2. S/H with bootstrapped circuit [6]

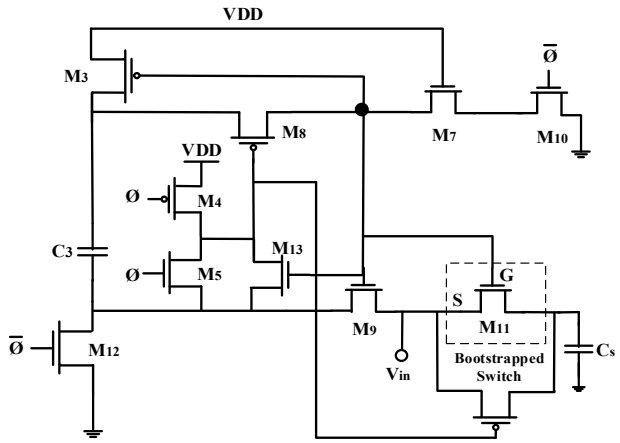

Fig. 3. Proposed modified low-power bootstrapped S/H circuit

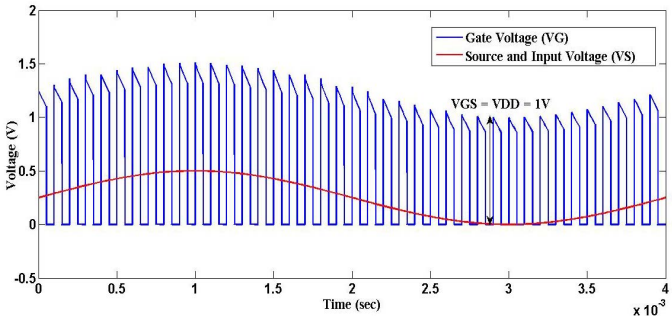

Fig. 4. M_{11} Input signal with the clock pulses formed on G for the proposed modified low-power bootstrapped S/H circuit

Fig. 5, shows the second type of bootstrapped technique which is S/H circuit with boosted driver. The principle of this circuit is to drive a boosted driver to the S/H circuit made of transmission gate. It operates by applying a square wave input signal of (V_{DD}). When Ø is high "off-state of the transmission gate S/H circuit", the bottom plate of C_2 and the top plate of C_1 are charged to (V_{DD}). On the other hand, (V_{DD}) will be applied to each second capacitor plates when Ø goes low "on-state of the transmission gate S/H circuit". Then, M_3 will transfer the charges stored in C_2 to the gate of M_N with an inverted square wave output which is generated according to [7][8]:

$$V_{gateMN} = 2V_{DD} \cdot (C_2/(C_2+C_{gateMN}+C_{parasitic})) \quad (1)$$

In other words, the boosted driver output is connected to the gate of the sampling transistor M_N. It has an inverted periodical signal switching between ($2V_{DD}$ - ΔV) and the ground. (ΔV) result from the charge sharing between the capacitor C_2 and the parasitic capacitance at the gate of M_N [3]. A simulation result shows the input clock pulses, the boosted driver output which is inverted boosted clock of 2V and the input voltage in Fig. 6.

The bandwidth of this circuit is ($1/2 \prod R_{on} C_S$), where R_{on} is the on-resistance of the sampling transistor M_N. This technique has the advantages in keeping the on-resistance of the sampling switch small which will result in both low power and wide bandwidth [3]. On the other hand, the gate-source voltage of the sampling transistor M_N is varying as shown in Fig. 6. This will make the on-resistance of the sampling transistor M_N varies. The effect of this problem will appear in the high-frequency applications where the sampling rate is high which will lead to high power consumption.

As a result, using bootstrapped circuit shown in Fig. 2 and Fig. 3 ensures that the switch is operating in a manner consistent with the reliability constraints. Because of this switch, (V_{GS11}) is relatively independent of the input signal. The importance of this circuit appears in minimizing the power consumption especially in the high-frequency applications compared to the S/H circuit with boosted driver as will be shown in the simulation results section. In addition to that, it keeps the on-resistance small constant value. The switch linearity is also improved and signal dependent charge injection is reduced using the transmission S/H circuit. Thus, bootstrapped circuit increase the settling speed and input bandwidth [6].

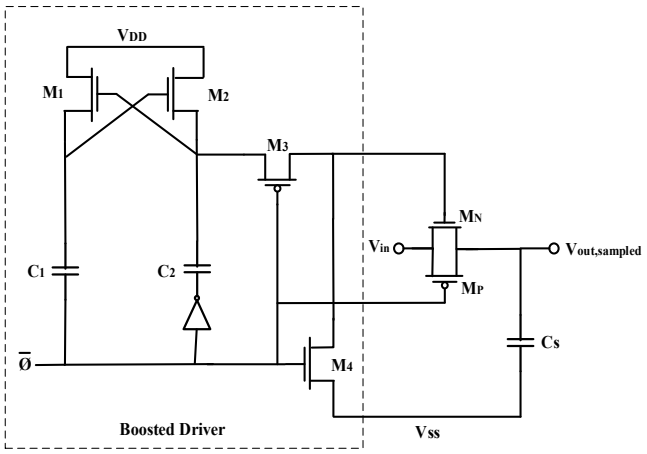

Fig. 5. S/H circuit with boosted driver [3]

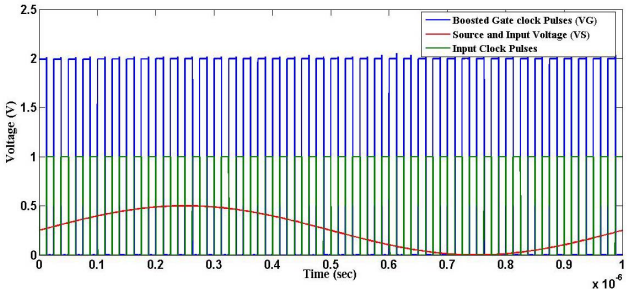

Fig. 6. Input clock pulses, boosted driver output and the input voltage

III. SIMULATION RESULTS

The three presented bootstrapped S/H circuit was simulated using 90nm CMOS technology on LT Spice IV. The input signal is a sine wave with 500 mV_{p-p} amplitude for a 1V supply voltage. They were tested under 20 kHz, 1 MHz and 7 MHz input signal frequencies. SNDR and the power consumption were measured for the presented bootstrapped S/H circuits. Fig. 7 shows the sampled output voltage for the proposed modified low-power bootstrapped S/H circuit. Fig. 8 illustrates the fast Fourier transform (FFT) of the sampled output voltage for the proposed modified low-power bootstrapped S/H circuit. The remaining presented bootstrapped S/H circuits have the same shape of the sampled output voltage and the FFT spectrum. The difference between them is shown in Table 1. Table. 1, illustrates the simulation results of the different bootstrapped S/H circuits with transmission gate as a switching element. As a result, the proposed modified low-power bootstrapped S/H circuit achieve the minimum power consumption among the others without notable SNDR degradation for medium and high frequency applications. Therefore, it is the best candidate in term of lower power consumption and high SNDR.

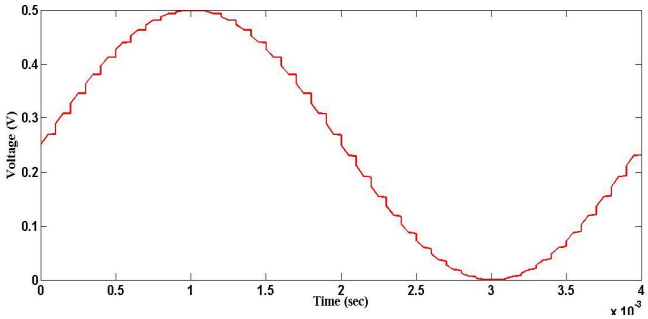

Fig. 7. Sampled output voltage for the proposed modified low-power bootstrapped S/H circuit

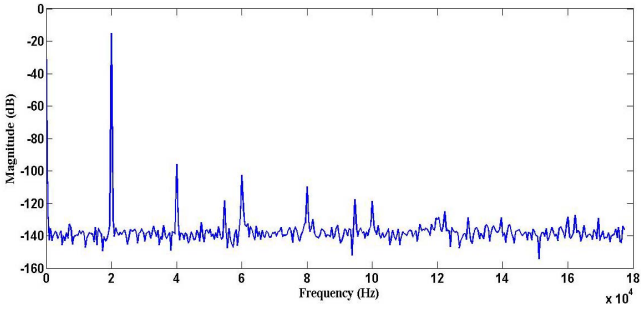

Fig. 8. FFT spectrum of sampled output voltage for the proposed modified low-power bootstrapped S/H circuit

IV. Conclusion

A proposed modified low-power bootstrapped S/H circuit is presented. The main theme of the proposed modified low-power bootstrapped circuit is to minimize the power consumption for S/H circuit without affecting the SNDR performance. This achieved by eliminating the multiplier circuit in [6] and replaced it with a PMOS transistor. As a result, the proposed low-power S/H with modified bootstrapped circuit consumes less power compared to other bootstrapped circuits which reported in [3] and [6] for medium and high frequency applications.

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TABLE. 1. SIMULATION RESULTS

S/H Circuits Types		**S/H with Boosted Driver [3]**	**S/H with Bootstrapped Circuit [6]**	**Proposed Modified Low-Power Bootstrapped S/H Circuit**
Applications	***Parameters***			
Audio (20 kHz)	SNDR (dB)	65.27	65.07	65.14
	Average Power Consumption	44.28 nW	54.03 nW	35.76 nW
	Power Saving (%)	-	-	20% - 35%
	Sampling Rate	800 KS/s with sampling capacitor of 1pf		
Bluetooth (1 MHz)	SNDR (dB)	56.56	56.76	56.69
	Average Power Consumption	2.06 µW	747.49 nW	201.09 nW
	Power Saving (%)	-	-	89% - 73%
	Sampling Rate	40 MS/s with sampling capacitor of 0.1pf		
DVB-H (7 MHz)	SNDR (dB)	57.06	57	57.01
	Average Power Consumption	12.68 µW	3.42 µW	883.57 nW
	Power Saving (%)	-	-	92% - 70%
	Sampling Rate	280 MS/s with sampling capacitor of 0.1pf		