

Article

# 10-Bit 5 MS/s Successive Approximation Register Analog-to-Digital Converter with a Phase-Locked Loop and Modified Bootstrapped Switch for a BLDC Motor Drive

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**Abstract:** In this paper, we present a successive approximation register (SAR) analog-to-digital converter (ADC) with a charge-pump (CP) phase-locked loop (PLL) and a bootstrapped switch, also called PLL-SAR ADC. To meet system-on-chip (SOC) and industrial requirements, the proposed SAR ADC and the control circuits of electric vehicles must be integrated into a single chip and be fabricated using the TSMC 0.25- $\mu$ m 1P3M complementary metal oxide semiconductor (CMOS) high-voltage process. It is difficult to implement a high-speed SAR ADC with the TSMC 0.25- $\mu$ m CMOS high-voltage process because it includes an N-type buried layer, which shorts all p-type metal oxide semiconductor field-effect transistor (PMOSFET) bodies together to withstand high voltages. In the proposed PLL-SAR ADC, two clock signals, an external clock signal and an internal clock signal from the CP-PLL, are provided to guarantee that a correct clock signal is fed. This design improves the robustness of the designed system. A monotonic capacitor-switching procedure is considered to reduce power consumption. Furthermore, a bootstrapped switch was added along with a dummy switch and a dummy transistor to eliminate disturbances in the input voltages and to improve the device's anti-noise capability. Moreover, a two-stage dynamic comparator was used to prevent kickback noise induced by the parasitic capacitors. The measurements indicate that the signal-to-noise-and-distortion ratio, effective number of bits, power consumption, and chip area are 53.82 dB, 8.65 bits, 1.256 mW, and  $1.261 \times 0.975 \text{ mm}^2$ , respectively. The FoM is approximately 0.625 pJ/conv-step at 1.256 mW, 8.65 bits, and 5 MS/s. The high sampling rate of 5 MS/s and high accuracy of 8.65 bits are the main advantages of the proposed PLL-SAR ADC.



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## 1. Introduction

This paper presents a 10-bit 5-MS/s successive approximation register (SAR) analog-to-digital converter (ADC) with a charge pump (CP) phase-locked loop (PLL) and a bootstrapped switch (referred to as PLL-SAR ADC) for a brushless direct current (BLDC) motor drive system. To meet system-on-chip and industrial requirements, we integrated the proposed SAR ADC and the control circuit of electric vehicles and implemented them by using the TSMC 0.25- $\mu$ m high-voltage complementary metal oxide semiconductor (CMOS). There is a demand for reducing the power consumption and cost of electric vehicles through the use of a CP-PLL [1], comparator, two bootstrapped switches, two monotonic capacitor arrays, SAR control logic, and digital error correction logic [2]. Moreover, because the

SAR ADC does not require a high-performance operational amplifier (OP Amp), its power consumption is remarkably low.

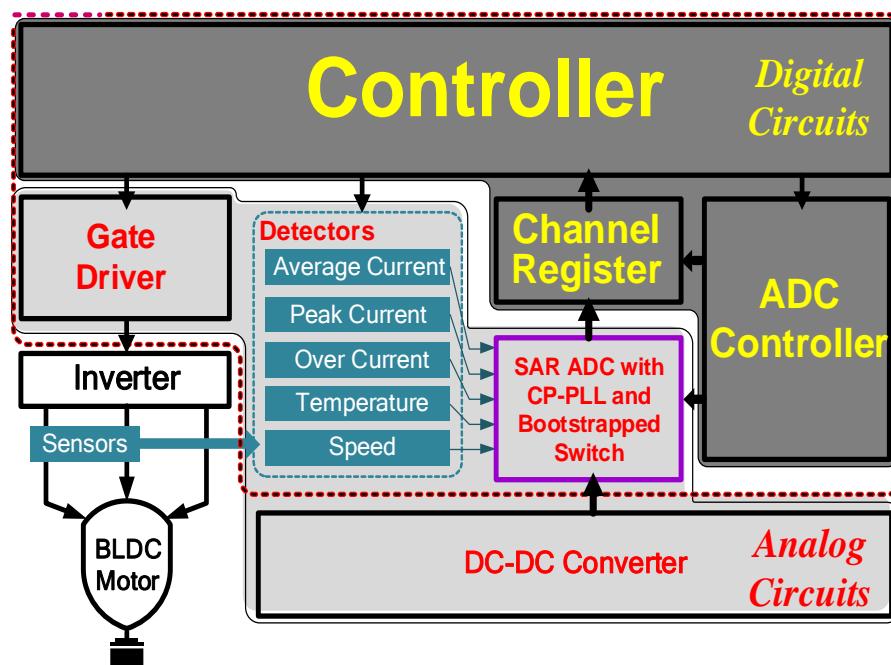
A BLDC motor drive is characterized by higher efficiency, lower maintenance, and higher cost. A new digital control concept for BLDC machines was introduced and experimentally verified. Because of the simplistic nature of this control concept, it can potentially be implemented in a low-cost, application-specific integrated circuit. Furthermore, this simplified control strategy does not require a state observer to regulate speed. A field programmable gain amplifier (PGA)-based novel digital pulse-width modulator (PWM) control scheme was developed to considerably reduce the system size and cost [3]. A high-performance permanent-magnet synchronous motor driver IC featuring a scheme without position sensors and with current-sensing circuits was proposed. To produce current-sensing circuits, a 10-bit SAR ADC and various gain amplifiers were implemented in the fabricated IC [4]. Sensing circuits and PGAs differ considerably in terms of the resolution of the SAR ADC. PGAs are used to amplify small voltages ( $\sim 20$  mV) that must be digitalized using 12-bit ADCs with up to 12.5 MS/s in motor control applications [5]. A high-performance MCU-integrated PGA with a complete on-chip motor control solution was fabricated with a 65-nm CMOS. The switching noise was mitigated through the provision of an on-chip programmable R-bank, which can achieve the necessary noise filtering, along with on-board capacitors [6]. That is, a completed on-chip motor control system can be implemented in the CMOS process.

The low-power low-noise integer-N divider-less technique can be employed to produce a digital PLL with high resolutions. A CP and a pulse-generation circuit are introduced to form the time-domain integral variable-gain amplifier to increase the resolution. A small-area SAR ADC is used to transform voltage signals into digital signals, thus avoiding the need for an analog filter, which occupies a large area. Compared with the conventional analog phase detector, the SAR ADC phase detector is compact and consumes less power [1]. In general, the resolution of a SAR ADC with a PLL is restricted to 8 or 10 bits. An 8-bit SAR ADC was designed for transceivers for use in space communication. A CP-PLL was used to generate the reference clock signal of this SAR ADC, and its effective number of bits (ENOB) and signal-to-noise-and-distortion ratio (SNDR) were 7.7 bits and 48.15 dB, respectively. The main advantages of the SAR ADC are low power consumption, high speed, and high linearity because of its integer-based digital-to-analog converter (DAC) architecture [7]. Furthermore, a 10-bit SAR ADC and PLL were employed with the TSMC 0.18- $\mu$ m CMOS process for the optical sensors used in the depth cameras embedded in virtual reality and augmented reality applications. Using the Vcm-based switching method significantly reduced the switching power of the DAC, and the resulting SAR ADC with the PLL design used fewer capacitors in the DAC array [8]. Moreover, a low-power reference-sampling digital PLL (RS-DPLL) equipped with a reference-sampling phase detector that used the bottom-plate sampling technique was proposed. The sampled voltage error was digitized using a gated amplifier incorporated with a compact 8-bit SAR ADC, resulting in a high resolution. The RS-DPLL, which was implemented using 28-nm CMOS technology, achieved a jitter of 355-fs rms and power consumption of only 1.1 mW [9]. Combining SAR ADC with PLL is a popular solution in many industrial applications. Moreover, this design is suitable for the BLDC motor drive.

An efficient capacitor-switching procedure was presented for a 10-bit 50-MS/s SAR ADC [10]. This switching procedure reduced both switching energy and total capacitance. Compared with the conventional switching procedure, this procedure had approximately 81% and 50% lower average switching energy and total capacitance, respectively. Moreover, the biased comparator reduced the dynamic offset induced by input common-mode voltage variation. However, this implementation was affected by process variations, and the coupling effect was not completely eliminated. To overcome this limitation, a dummy switch was used to improve the sample-and-hold accuracy. The dummy compensation mechanism removed the effect of clock feedthrough contributed by the observed voltage error to extremely low levels. The CMOS analog bootstrapped switch was found to be

suitable for use in a high-precision sample-and-hold circuit [11]. Subsequently, an SAR ADC equipped with a DAC consisting of grouped capacitors was implemented to reduce the bottom-plate parasitic capacitance threshold for the achievement of high speed and high power efficiency. The dual-path bootstrapped switch improved the sampling spurious-free dynamic range (SFDR) by more than 5 dB by isolating the critical signal from the N-well capacitance [12].

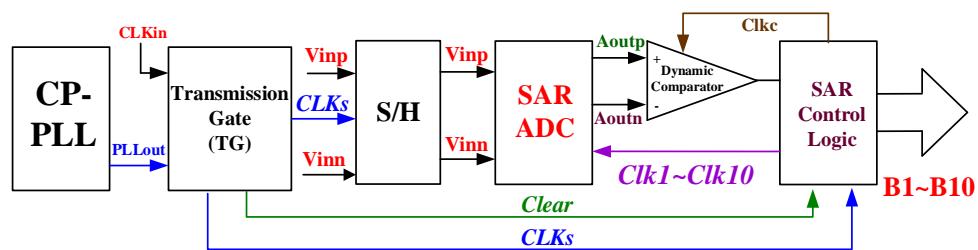
Figure 1 presents a system block diagram of an electric vehicle with a BLDC motor drive, which is composed of a digital controller, a channel register, an ADC controller, a gate driver, various detectors, a SAR ADC with a CP-PLL and bootstrapped switch, a direct current–direct current (DC–DC) buck converter, an inverter, and a BLDC motor [13]. The digital circuits include the digital controller, channel register, and ADC controller, and the analog circuits include the gate driver, detectors, SAR ADC with a CP-PLL and bootstrapped switch, and DC–DC buck converter. Notably, multichannel detectors were used to detect and monitor useful parameters, including average current, peak current, overcurrent, temperature, and speed. After the sensing data are digitalized using the proposed SAR ADC, a digital control code is fed into the ADC controller to generate an appropriate PWM signal for controlling the gate driver and smoothly driving the BLDC motor. In brief, the designed SAR ADC is a key component in BLDC motor drive. The proposed PLL-SAR ADC performs with low power consumption, high sampling rate, and high linearity. It meets the requirements of SAR ADC in BLDC motor drive because the PWM register contains an 8-bit channel with clock frequencies of 0.25–8.0 MHz. An N-type buried layer is used to withstand high voltages through sharing of the bodies of all p-type metal oxide semiconductor field-effect transistors (PMOSFETs or PMOSs) in the TSMC 0.25- $\mu\text{m}$  CMOS high-voltage process. We attempted to avoid shorting the source and body in the PMOSFETs. Furthermore, a dummy switch and a dummy transistor are added to improve the performance of the sample-and-hold circuit. The proposed SAR ADC provides a correct clock signal without an external signal generator. The remainder of this paper is organized as follows. Section 2 elucidates the circuit design of the proposed SAR ADC with a CP-PLL and modified bootstrapped switch. Section 3 presents the simulated and measured results. Section 4 presents our concluding remarks.



**Figure 1.** Proposed system block diagram of an electric vehicle for the BLDC motor drive.

## 2. Circuit Design of the Proposed PLL-SAR ADC

Figure 2 presents the system block diagram of the proposed PLL-SAR ADC with the modified bootstrapped switch. It was implemented with a monotonic capacitor-switching procedure to save power, CP-PLL to control the clock signal (CLks), clear signal to reset the digital codes of the SAR control logic (Clear), and transmission gate (TG) to select the appropriate clock signal. Two clock signals, an external clock signal (CLKin) and an internal clock signal from the CP-PLL (*PLLout*), are provided to guarantee that a correct CLks is obtained. After the design and verification of the proposed blocks, the PLL-SAR ADC system was fabricated with the TSMC 0.25- $\mu$ m 1P3M CMOS high-voltage process for industrial applications through integration of the control circuits into a single chip.

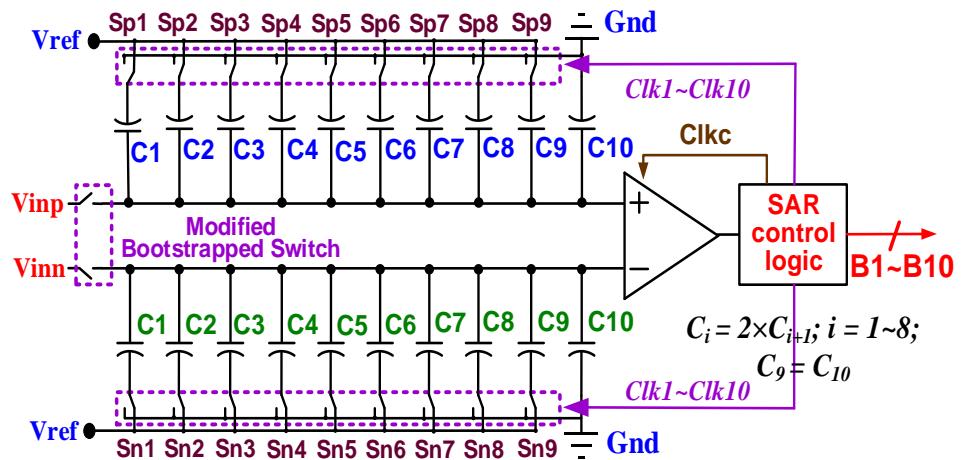


**Figure 2.** System block diagram of the proposed PLL-SAR ADC with a bootstrapped switch.

### 2.1. System Design of the SAR ADC

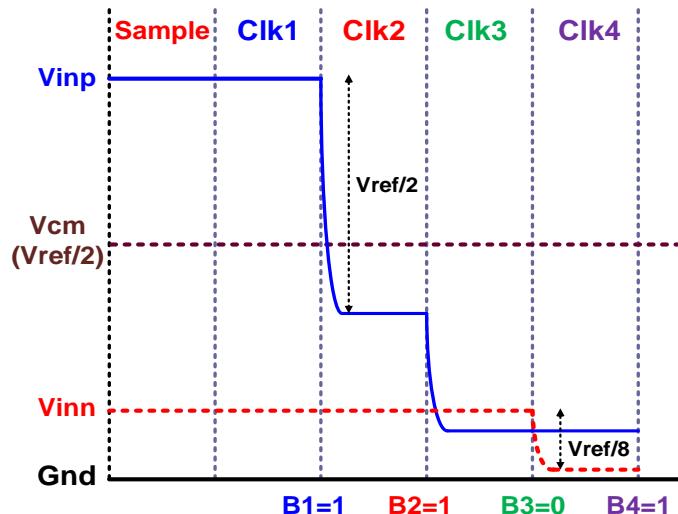
In the single-ended architecture, only one end of the capacitor is switched. Consequently, the power consumption and the chip area are smaller than those of the dual-ended architecture. The advantage of the dual-ended architecture is that it can suppress any interference noise. Thus, combining the single capacitor-switching procedure with the dual-ended architecture yields a continuous progressive ADC with low power dissipation and the suppression of switching noise.

Figure 3 illustrates the dual-ended SAR ADC with the monotonic switching topology used herein. In the sample mode, the differential input signal passes through the sample-and-hold circuit (S/H) and samples the input signal against the upper plate of the capacitor array. The switches Sp1–Sp9 and Sn1–Sn9 are switched to the reference voltage  $V_{ref}$ , which is connected to the power supply  $V_{DD}$ . In the first cycle ( $Clk1$ ), the comparison begins with the use of the differential input voltages  $V_{inp}$  and  $V_{inn}$ , and all of the switches remain unchanged. If the positive input voltage  $V_{inp}$  is higher than the negative input voltage  $V_{inn}$ , then the first output bit B1 is set to 1. In the second cycle ( $Clk2$ ), the first weighted capacitor C1 on the positive side is switched to the ground voltage ( $Gnd = 0$  V) through switching of the first positive switch Sp1. The other positive switches Sp2–Sp9 and negative switches Sn1–Sn9 remain unchanged. If  $V_{inp}$  is higher than  $V_{inn}$ , then the second output bit B2 is set to a high voltage ( $V_{ref}$ ) and the second weighted capacitor C2 on the positive side is connected to  $Gnd$ . If not, the second output bit B2 is set to a low voltage ( $Gnd$ ), the second capacitor C2 on the negative side is switched to  $Gnd$ , and the remaining capacitors remain connected to  $V_{ref}$ . This switching procedure continues until the minimum output bit (B10) is obtained. The power consumption of this capacitance switching is effectively reduced because switching is only performed with one side of the capacitor. Two basic capacitors ( $C_{11}$ ) at upside and downside and four switches (Sp10–Sp11 and Sn10–Sn11) are eliminated, leading to a significantly smaller chip area and significantly less switching noise compared with those of the conventional 10-bit SAR ADC [10].



**Figure 3.** Adopted dual-ended SAR ADC with monotonic switching topology.

Figure 4 shows the adopted monotonic switching procedure, which does not require upward transition and performs sampling on the top plate. These features accelerate DAC settling. In addition, the first comparison can be performed without any capacitor switching in the first clock ( $Clk1$ ), as illustrated in Figure 4. In  $Clk2$ , the adopted switching sequence reduces  $Vinp$  to  $(Vinp - Vref/2)$  and maintains the negative input voltage  $Vinn$ . In  $Clk3$ , the positive input voltage  $Vinp$  is reduced to  $(Vinp - Vref/2 - Vref/4)$ , and the negative input voltage  $Vinn$  is unchanged. In  $Clk4$ , the negative input voltage is reduced to  $(Vinn - Vref/8)$ , and the positive input voltage  $Vinp$  remains unchanged. The switching procedure continues until the ground voltage is reached. In contrast to the conventional switching procedure [10], the proposed procedure only requires the downward transition to be switched in each comparison. The monotonic capacitor-switching procedure thus reduces power consumption and switching noise.

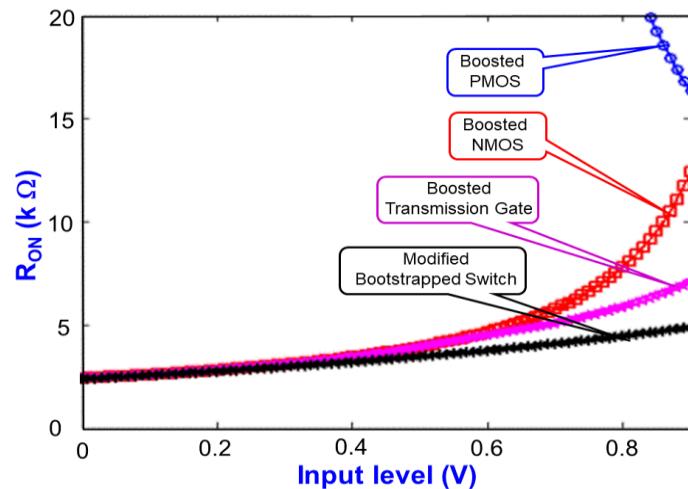


**Figure 4.** Waveform of the adopted monotonic switching procedure.

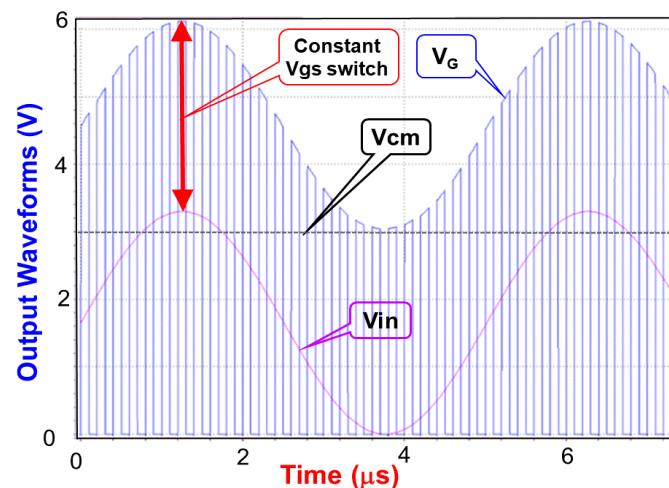
## 2.2. Modified Bootstrapped Switch with a Dummy Switch and Dummy Transistor

In the sample mode, a modified S/H is used to sample the differential input voltage, which is affected by the changing switch impedance. As the control signal ( $PLLout$ ) is fed into the switch from the CP-PLL, distortion occurs as a result of the changing switch impedance, which increases the signal noise and distortion and reduces the signal-to-noise ratio (SNR) and SNDR. To overcome this problem, a good switch with a small on-resistance must be identified. Figure 5 depicts the simulated on-resistance  $R_{on}$  with respect to the input levels of various switches, including the boosted PMOS, boosted NMOS, boosted

TG, and modified bootstrapped switch with a constant gate-to-source voltage ( $V_{gs}$ ). The modified bootstrapped switch operates with a small and linear conducting impedance. Figure 6 illustrates the simulated output waveforms of the modified bootstrapped switch. Notably, the  $V_{gs}$  remains constant between the gate voltage  $V_G$  and the input signal  $V_{in}$ .



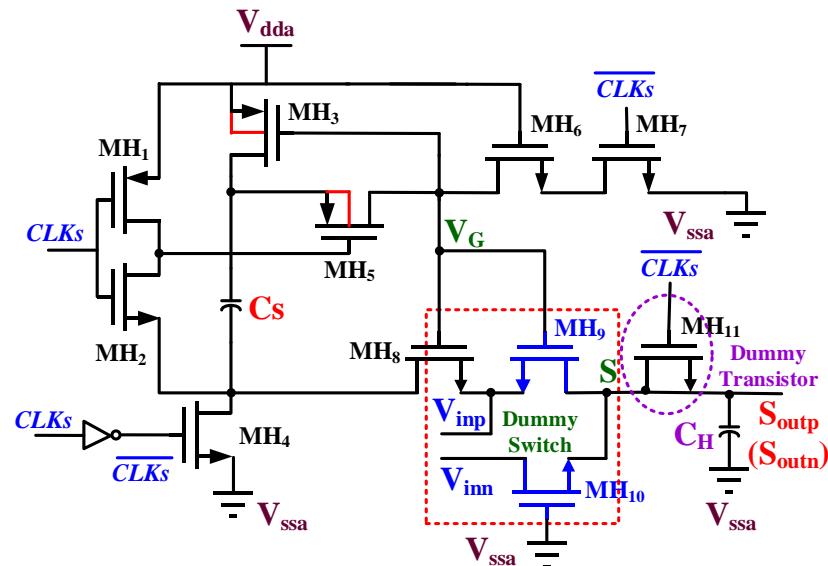
**Figure 5.** Simulated on-resistance with respect to the input levels of various switches.



**Figure 6.** Simulated output waveforms of the modified bootstrapped switch with a constant  $V_{gs}$ .

Figure 7 depicts the modified sample-and-hold circuit with a constant  $V_{gs}$  switch and a dummy switch. It is composed of a sampling capacitor  $C_S$  and a bootstrapped switch  $MH_9$  to facilitate operation with low power dissipation and a wide bandwidth. The boosted driver causes periodic output switching between  $(V_{dda} + V_{inp})$  and  $V_{inp}$  by using the analog positive power supply  $V_{dda}$  and the input voltage  $V_{inp}$ . Two PMOSs, namely  $MH_3$  and  $MH_5$ , are used to rectify the errors caused by the charge injection and clock feedthrough because these switches operate interactively. If  $CLK_s = 0$ , then the NMOSs  $MH_4$ ,  $MH_7$ , and  $MH_{11}$  are turned on simultaneously. The voltage  $V_G$  is set to 0 V after it has passed through  $MH_6$  and  $MH_7$ . Next, the PMOS  $MH_3$  is turned on due to the gate voltage  $V_G$  (0 V). The sampling capacitor  $C_S$  is rapidly charged to  $V_{dda}$ . Meanwhile,  $MH_5$  is turned off upon its connection to  $V_{dda}$  through  $MH_1$  and two NMOSs, namely  $MH_8$  and  $MH_9$ , are turned off upon their connection to the gate voltage  $V_G$  (0 V). By contrast, if  $CLK_s = 1$ , then the gate voltage of  $MH_5$  is set to the ground voltage (0 V) to activate  $MH_5$ . Subsequently, the gate voltage  $V_G$  is charged to  $V_{dda}$ . The voltage difference between the power supply voltage ( $V_{dda}$ ) and ground voltage ( $V_{ssa}$ ) is stored in the sampling capacitor  $C_S$ . When the positive

input voltage  $V_{inp}$  is fed to  $MH_8$ , the voltage  $V_G$  is charged upward to  $(V_{dda} + V_{inp})$ . Next, the gate-to-source voltage  $V_{gs8}$  of  $MH_8$  is fixed to  $V_{dda}$  regardless of the variation of the input voltage  $V_{inp}$ . That is, the positive output voltage  $S_{outp}$  is not adversely affected by the errors in  $MH_8$  and  $MH_9$ , which are induced by charge injection and clock feedthrough. Notably, a dummy switch  $MH_{10}$  is added to increase precision by reducing the coupling effect and on-resistance [11].

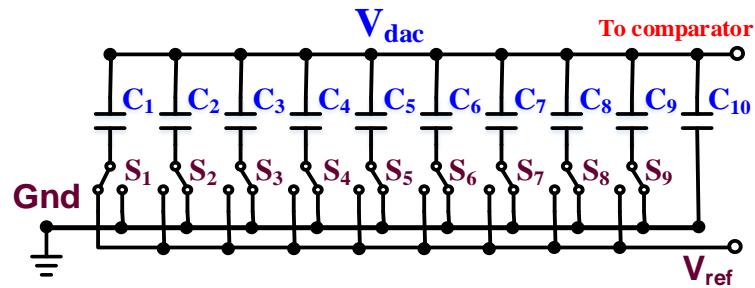


**Figure 7.** Modified sample-and-hold circuit with modified bootstrapped switch, including a dummy switch and a dummy transistor.

As illustrated in Figure 7, the positive output voltage  $S_{outp}$  is achieved at the corresponding inputs of  $V_{inp}$  and  $V_{inn}$  after passage through  $MH_9$  and  $MH_{10}$ , respectively. The corresponding inputs  $V_{inn}$  and  $V_{inp}$  are connected to  $MH_9$  and  $MH_{10}$ , respectively, to obtain the negative output voltage  $S_{outn}$ . A dummy switch  $MH_{10}$  is added to reduce the clock feedthrough and eliminate voltage disturbance, which is induced by the parasitic capacitance  $C_{ds}$  at the S/H capacitor  $C_H$  [2]. Furthermore, a dummy transistor  $MH_{11}$ , driven by  $\overline{CLKs}$ , is added to the circuit such that after  $MH_9$  and  $MH_{10}$  are turned off and  $MH_{11}$  is turned on, the channel charge deposited on  $C_H$  is absorbed by the dummy transistor  $MH_{11}$  to alleviate the error induced by charge injection and to improve the switch linearity [14].

### 2.3. Binary-Weighted Capacitor Array DAC

The DAC is used to convert the digital codes at the output of the SAR logic into an analog signal. The analog signal is then compared with the input signal with a comparator. The DAC is generally composed of resistors or capacitor arrays. To reduce power consumption, a 10-bit binary-weighted capacitive DAC (CDAC) is considered herein, as illustrated in Figure 8. This DAC is composed of 10 binary-weighted capacitors ( $C_1$ – $C_{10}$ ) and a set of switches ( $S_1$ – $S_9$ ). The capacitance relationship is  $C_i = 2 \times C_{i+1}$  and  $C_9 = C_{10}$ , where  $i = 1$ –8.



**Figure 8.** Proposed 10-bit binary-weighted capacitive DAC.

The maximum settling time of a DAC is usually determined by the charge and discharge procedure of the most significant bit (MSB) and by the conversion speed of the MSB with the maximum offset. Thus, the decoding error is greater than all of the noise sources, which reduces the SNR if the DAC is poorly designed. To realize a high-resolution DAC, these mismatches, which are induced by practical capacitors and parasitic capacitors, must be analyzed and eliminated. If the maximum capacitor  $C_1$  is connected to  $V_{ref}$  with an error rate of  $\varepsilon$  and the remaining capacitors ( $C_2$ – $C_{10}$ ) are connected to the ground, the output voltage of the DAC with a mismatch capacitor can be expressed as follows:

$$V_{dac}(mis) = V_{ref} \times \frac{C_1(1 + \varepsilon)}{\sum_{i=2}^{10} C_i + C_1(1 + \varepsilon)} \quad (1)$$

Let us assume that the reference voltage  $V_{ref}$  is 3.3 V and the resolution is 10 bits; the ideal output voltage of the DAC  $V_{dac}$  (ideal) is thus 1.65 V, which is half of the reference voltage. The maximum error rate  $\varepsilon$  can be calculated as follows.

$$V_{dac}(mis) - V_{dac}(ideal) \leq 1LSB \quad (2)$$

$$\Rightarrow 3.3 \times \frac{C_1(1 + \varepsilon)}{C_1 + C_1(1 + \varepsilon)} - 1.65 \leq \frac{3.3}{2^{10}} \quad (3)$$

$$\Rightarrow \varepsilon \leq 0.0039139 = 0.39139\% \quad (4)$$

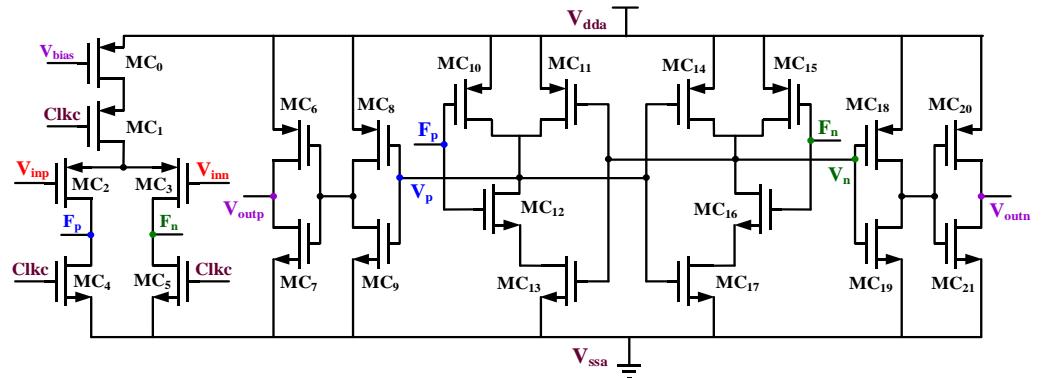
The DAC is extremely sensitive to switch ratio and capacitor mismatch, especially in case of the minimum capacitor  $C_0$ . The capacitor layout must be designed carefully to eliminate the mismatch effect [15].

#### 2.4. Modified Two-Stage Dynamic Comparator

A dynamic latch-type comparator is used to rapidly latch the voltage difference between the two inputs  $V_{inn}$  and  $V_{inp}$  to the high level (1) or low level (0) through positive feedback. The dynamic latch comparator does not consume static power, unlike the open-loop amplifier. For a single capacitor, the comparator has a pull-down switching design. That is, the common-mode voltage at the comparator input is switched between  $V_{ref}/2$  and  $V_{ssa}$ . This means that the dynamic comparator must be operated at a low voltage. To this end, a differential pair, which is established in the PMOSs, is a good choice.

Figure 9 illustrates a modified two-stage dynamic comparator [16]. When the clock signal  $Clkc$  is high, two n-type metal oxide semiconductor field-effect transistors (NMOS-FETs or NMOSs)  $MC_4$  and  $MC_5$  are turned on. The dynamic comparator operates in the reset mode, and the two float voltages  $F_p$  and  $F_n$  are connected to the ground. Next, two PMOSFETs,  $MC_{10}$  and  $MC_{15}$ , are turned on, and the power voltage  $V_{dda}$  is directly connected to two internal voltages  $V_p$  and  $V_n$ . When passing through two NOT gates, the two output voltages  $V_{outp}$  and  $V_{outn}$  are high. Notably, the NMOSFET  $MC_1$  is turned off when  $Clkc = 1$  (high), as is the dynamic comparator. Therefore, it does not consume any static current. By contrast, when the clock signal  $Clkc$  is low (0),  $MC_4$  and  $MC_5$  are turned off and  $MC_1$  is turned on. The dynamic comparator operates in the comparison mode. The

two float voltages  $F_p$  and  $F_n$  are then determined according to the two inputs  $V_{inp}$  and  $V_{inn}$ . If  $V_{inp} > V_{inn}$ , then  $F_p < F_n$ . When passing through two inverters, MC<sub>10</sub>–MC<sub>13</sub> and MC<sub>14</sub>–MC<sub>17</sub>,  $V_p > V_n$ . Finally, the positive output voltage  $V_{outp}$  is higher than the negative output voltage  $V_{outn}$ . A higher input voltage  $V_{inp}$  corresponds to a higher output voltage  $V_{outp}$ . The modified two-stage dynamic comparator can prevent kickback noise and is insensitive to the input signal.



**Figure 9.** Detailed circuit of the modified two-stage dynamic comparator.

Taking the input-stage of the dynamic comparator as an example, the input offset voltage  $V_{os}$  can be expressed as follows [17]:

$$V_{os} = \Delta V_{TH2,3} + \frac{(V_{GS} - V_{TH})_{2,3}}{2} \left( \frac{\Delta S_{2,3}}{S_{2,3}} + \frac{\Delta R}{R} \right) \quad (5)$$

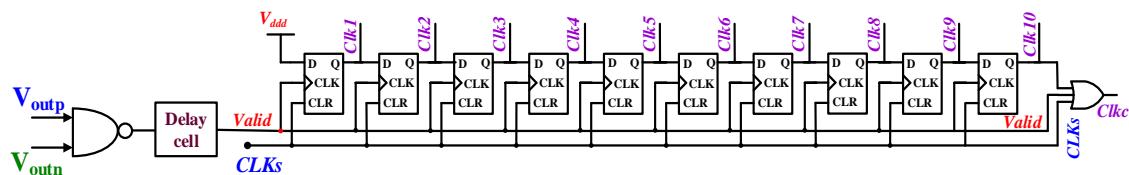
where  $\Delta V_{TH2,3}$  is the threshold voltage mismatch of the two input PMOSFETs MC<sub>2</sub> and MC<sub>3</sub>.  $\Delta S_{2,3}$  is the mismatch in physical dimensions between MC<sub>2</sub> and MC<sub>3</sub>.  $\Delta R$  is the resistor mismatch of the load resistance, which is contributed by the two NMOSFETs MC<sub>4</sub> and MC<sub>5</sub>. As expressed in (5), the first term represents a static offset, which does not affect the performance of the ADC, whereas the second term is a dynamic offset, which is affected by variation in the common-mode voltage. The offset voltage  $V_{os}$  can be reduced through a decrease in the overdrive voltage ( $V_{GS} - V_{TH}$ )<sub>2,3</sub> through MC<sub>2</sub> or MC<sub>3</sub>. Thus, the gate of MC<sub>0</sub> is connected to  $V_{bias}$  to reduce the offset error in the second term. Moreover, the two NMOSFETs, MC<sub>12</sub> and MC<sub>16</sub>, are added not only to reduce the offset error but also to enhance the linearity of the modified dynamic comparator.

## 2.5. Modified SAR Control Logic

The continuous progressive controller is implemented with CMOS circuits. The designed functions of the SAR control logic include controlling the reset signal of the dynamic comparator, managing the switching action of the DAC, storing the comparison result of the comparator, and exporting the digital codes.

A modified asynchronous SAR control logic circuit is proposed to generate the necessary clock signals through the addition of a delay cell to guarantee that the output clock signals are asynchronous [10]. Figure 10 shows a schematic of the modified asynchronous SAR control logic circuit with the digital power supply  $V_{ddd}$ , which is used not only to accept the two control signals *Valid* and *CLKs* but also to generate a comparison signal *Clkc* and 10 asynchronous clock signals *Clk1*–*Clk10*. The signal *CLKs* is fed through the TG to reset the control logic. The signal *Valid* is generated from two output voltages of the modified dynamic comparator  $V_{outp}$  and  $V_{outn}$ . The clock signals *Clk1*–*Clk10* sample the digital output codes of the two-stage dynamic comparator and furnish them to the capacitor arrays to execute the monotonic switching procedure. Table 1 summarizes the state table of the SAR control logic for controlling the DAC switches. As the dynamic comparator completes the comparison, the signal *Valid* is sent to the asynchronous SAR control logic

circuit to trigger the clock signals in order and maintain them at a high level ( $V_{dd}$ ). If the reset signal (*Clear*) starts at  $CLks = 1$  (high), the clock signals  $Clk1$ – $Clk10$  are reduced to the low level (Gnd). A delay cell is added to the asynchronous control logic circuit to guarantee that the output level of the capacitor array remains stable. This means that the time delay of the delay cell must be longer than the settling time of the DAC capacitor array.

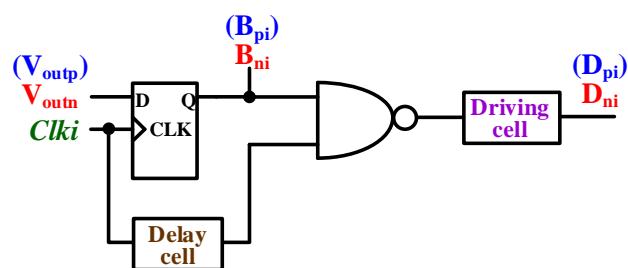


**Figure 10.** Schematic of the modified asynchronous SAR control logic circuit.

**Table 1.** State table of SAR control logic for controlling the DAC switches.

Clock Signals	State of SAR Control Logic										
	ST <sub>0</sub>	ST <sub>1</sub>	ST <sub>2</sub>	ST <sub>3</sub>	ST <sub>4</sub>	ST <sub>5</sub>	ST <sub>6</sub>	ST <sub>7</sub>	ST <sub>8</sub>	ST <sub>9</sub>	ST <sub>10</sub>
CLks	0	0	0	0	0	0	0	0	0	0	1
Clk1	1	1	1	1	1	1	1	1	1	1	0
Clk2	0	1	1	1	1	1	1	1	1	1	0
Clk3	0	0	1	1	1	1	1	1	1	1	0
Clk4	0	0	0	1	1	1	1	1	1	1	0
Clk5	0	0	0	0	1	1	1	1	1	1	0
Clk6	0	0	0	0	0	1	1	1	1	1	0
Clk7	0	0	0	0	0	0	1	1	1	1	0
Clk8	0	0	0	0	0	0	0	1	1	1	0
Clk9	0	0	0	0	0	0	0	0	1	1	0
Clk10	0	0	0	0	0	0	0	0	0	1	0

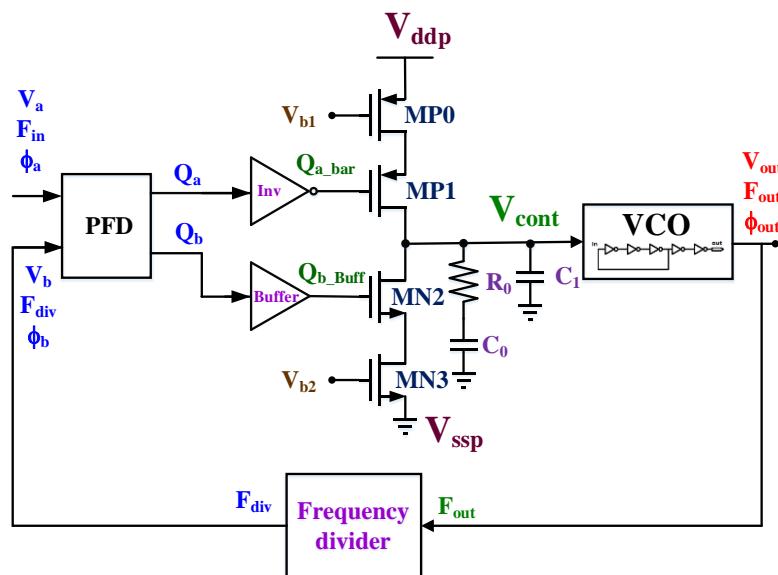
The designed DAC control circuits are divided into two categories: N-type and P-type. Each type operates with 10 DAC control circuits. That is, there are 20 DAC control circuits in the asynchronous SAR control logic circuit. Figure 11 presents the modified DAC control circuit [10], which includes  $V_{outn}/V_{outp}$ ,  $Clki$ ,  $B_{ni}/B_{pi}$ , and  $D_{ni}/D_{pi}$ . The integer  $i$  refers to an  $i$ -bit control signal. The output voltages  $V_{outn}$  and  $V_{outp}$  are captured using the dynamic comparator circuit. The output clock signal  $Clki$  of the asynchronous SAR control logic circuit is used to control the switching procedure of the DAC. Because  $Clki$  is positive-edge triggered, the captured output voltage  $V_{outn}/V_{outp}$  is transferred to the output voltage of a D-type flip-flop (DFF)  $B_{ni}/B_{pi}$ . After passage through the NAND gate, the output control signal  $D_{ni}/D_{pi}$  for controlling the DAC capacitor array is obtained. For example, if  $V_{outp} = 1$  (high), then  $D_{pi} = 0$ . The lower plate of the capacitor is connected to  $V_{ssa}$  from  $V_{ref}$ . If  $V_{outn} = 0$ , then  $D_{ni} = 1$  (high). That is, the lower plate of the capacitor operates without action. Notably, a driving cell is added to alleviate the switching error of the high binary-weighted DAC capacitor array.



**Figure 11.** Modified DAC control circuit with  $V_{outn}/V_{outp}$ ,  $Clki$ ,  $B_{ni}/B_{pi}$ , and  $D_{ni}/D_{pi}$ .

## 2.6. Fundamental PLL

A fundamental PLL was adopted to guarantee that the frequency ( $F$ ) and the phase ( $\phi$ ) of the input reference signal  $V_a$  and the feedback signal  $V_b$  are the same. Figure 12 depicts the adopted fundamental PLL, which includes a phase frequency detector (PFD), CP, loop filter, voltage-controlled oscillator (VCO), and frequency divider (FD) [18,19]. The operating principle of the fundamental PLL can be described as follows: the PFD detects the phase difference ( $\Delta\phi$ ) between the input reference signal ( $V_a$ ) and the feedback signal ( $V_b$ ) and transmits two output signals  $Q_a$  and  $Q_b$  to the CP for the subsequent stage. The inverse voltage  $Q_{a\_bar}$  passing through the inverter and the buffer is used to control the PMOSFET  $MP_1$ , and the buffer voltage  $Q_{b\_Buff}$  is used to control the NMOSFET  $MN_2$ . That is, two control signals  $Q_{a\_bar}$  and  $Q_{b\_Buff}$  are connected to the gates of  $MP_1$  and  $MN_2$ , respectively, to charge or discharge the loop filter, which is composed of a resistor  $R_0$  and two capacitors  $C_0$  and  $C_1$ . A control voltage  $V_{cont}$  is then generated to change the output frequency  $F_{out}$  of the VCO. The output frequency  $F_{out}$  passing through the FD is divided to generate a feedback frequency  $F_{div}$ , which is close to the input reference frequency  $F_{in}$  and reduces the phase difference ( $\Delta\phi$ ) between  $\phi_a$  and  $\phi_b$ . This procedure is repeated until  $\Delta\phi = 0$ . The function of the fundamental PLL is to guarantee that the frequency and phase of  $V_a$  are identical to those of  $V_b$ . However, only a clock signal appears in the traditional SAR ADC. It requires an external clock generator and fails to guarantee the synchronous operation between  $V_a$  and  $V_b$ .

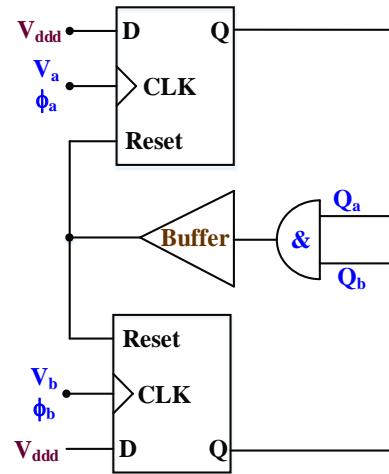


**Figure 12.** Adopted fundamental PLL.

VCO generates an output frequency  $F_{out}$  based on the control voltage  $V_{cont}$ . The ring oscillator is a popular oscillator, and it is implemented without passive components. This feature is suitable for fabrication in the CMOS process. In general, a ring oscillator is composed of an odd number of inverters. The delay time  $t_d$  is inherent in the inverter from the input to the output, and vice versa. When a ring oscillator is initiated, the oscillation frequency  $f_{osc}$  is equal to  $1/(2 \times t_d)$ . The greater the odd number of inverters, the lower the oscillation frequency.

Figure 13 illustrates the adopted PFD, which is composed of two DFFs, a buffer, and an AND gate. If the CLK is triggered by the input reference voltage  $V_a$ , then the output  $Q_a$  is high because the data (D) are connected to the digital power supply  $V_{ddd}$ . The same mechanism is executed with the feedback voltage  $V_b$ . The PFD used herein can correctly detect the phase difference between  $\phi_a$  and  $\phi_b$ . If the phase of  $\phi_a$  is ahead relative to that of  $\phi_b$ , a pulse waveform is generated at  $Q_a$ , and the pulse width of this waveform is proportional to  $\Delta\phi$ . By contrast,  $Q_b$  generates a pulse waveform if the phase of  $\phi_b$  is

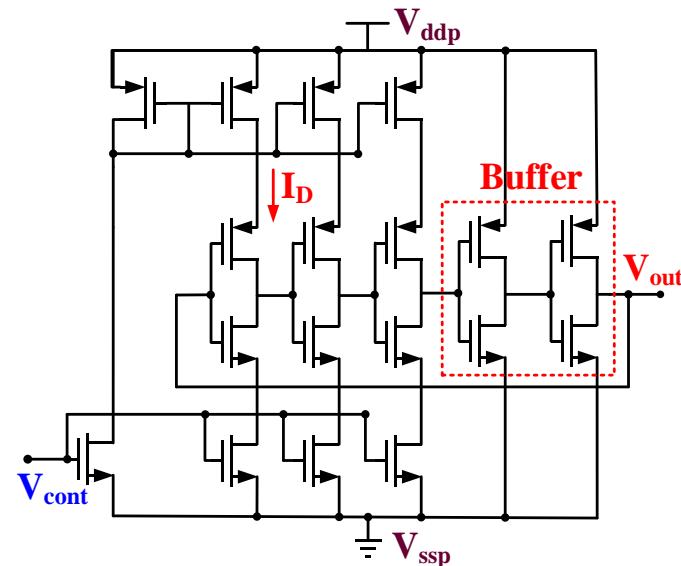
ahead relative to that of  $\phi_a$ . A buffer is used to drive the reset signal when both  $Q_a$  and  $Q_b$  are high.



**Figure 13.** Adopted PFD with two DFFs, a buffer, and an AND gate.

Figure 14 shows the modified three-stage current-starved VCO (CS-VCO) with a buffer, which offers low power dissipation, low phase noise, and high oscillation frequency [20]. If a certain drain current  $I_D$ , number of inverter stages  $N$ , and total capacitance  $C_{tot}$  of a single-stage inverter circuit are known, then the oscillation frequency  $f_{osc}$  can be calculated using the digital power supply  $V_{ddd}$ .

$$f_{osc} = \frac{I_D}{N \times C_{tot} \times V_{ddd}} \quad (6)$$

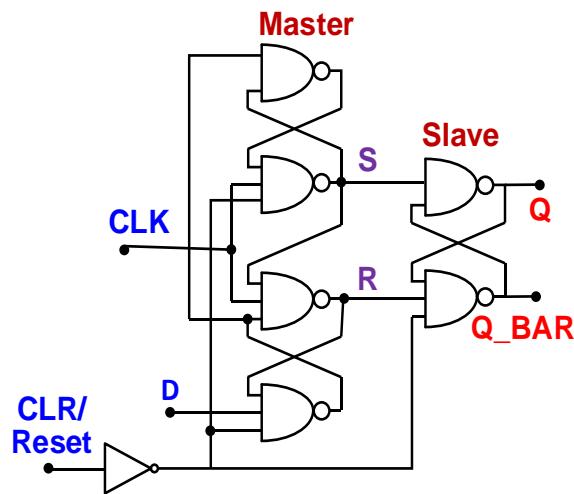


**Figure 14.** Modified three-stage CS-VCO with a buffer.

If both  $N$  and  $f_{osc}$  are selected according to the designed CS-VCO, then the drain current  $I_D$  can be calculated with (6). The transistor sizes ( $W/L$ ) can then be set based on the aforementioned calculated drain current. A buffer is added to improve the output swing voltage based on the two inverters. There is usually a tradeoff between the output swing voltage and the oscillation frequency. The FD of the PLL is implemented using a six-stage DFF circuit [21]. The divide ratio of the divider circuit is set to 64. If the output

frequency of the CS-VCO is 320 MHz, with a divide ratio of 64, then the feedback frequency  $F_{div}$  is 5 MHz.

Figure 15 shows the adopted DFF with the asynchronous reset circuit, which is composed of two master R-S latches and a slave latch [22]. When the reset signal is set to 1, the data (D) and clock (CLK) inputs are simultaneously overridden with a logic low (0). S is then forced to high (1), and R is forced to low (0). The output Q is forced to low (0), and Q\_BAR is forced to high (1). Because the rising edge of the clock is used to load the value at the D input, which causes the two master R-S latches to briefly toggle states, the two master R-S latches must be cleared at the same instant. The function of the reset pin should be clean and glitch-free at the outputs Q and Q\_BAR. That is, Q should be set to low (0) if it is high (1), and Q\_BAR becomes high (1) with almost no skewing.



**Figure 15.** Adopted DFF with asynchronous reset circuit design.

### 3. Simulation and Measurement Results

According to (5), the larger the physical dimension  $S_{2,3}$ , the smaller the offset error  $V_{os}$ . However, the enlarged dimensions of MC<sub>2</sub> and MC<sub>3</sub> reduce the operating speed and increase power consumption. Another method involves adding a serial NMOSFET MC<sub>12</sub> to MC<sub>13</sub>, as illustrated in Figure 9. This design not only reduces the offset error but also enhances the linearity of the modified dynamic comparator. If an offset error  $V_{os}$  occurs at the input node, then the change in the drain voltage  $F_p$  of MC<sub>4</sub> is significant, and the variation of the gate-to-source voltage  $\Delta V_{GS12}$  of MC<sub>12</sub> is large. However, the drain-to-source voltage  $V_{DS12}$  of MC<sub>12</sub> varies marginally because MC<sub>12</sub> operates in the saturation mode. The internal voltage  $V_p$  thus changes insignificantly. Furthermore, the common-mode input voltage  $V_{inp}$  of MC<sub>2</sub> is equal to that of  $V_p$  with perfect matching. This design improves the linearity of the modified dynamic comparator.

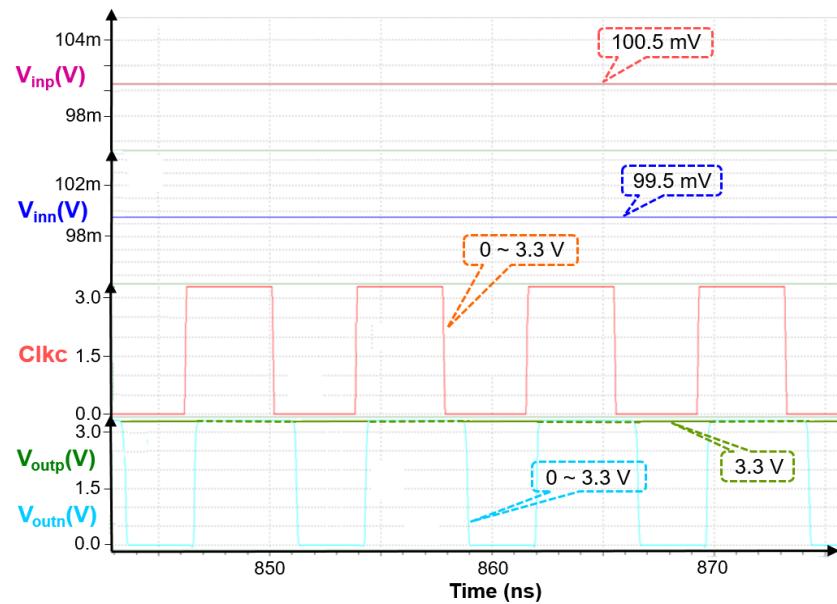
$$\begin{cases} V_{inp} = V_{ov2} + F_p - |V_{GS2}| \\ F_p = V_{GS12} + V_{ov13} \end{cases} \quad (7)$$

$$\Rightarrow V_{inp} = V_{ov2} + (V_{GS12} + V_{ov13}) - |V_{GS2}| \approx V_{ov2} + V_{ov13} \approx V_{ov12} + V_{ov13} \approx V_p \quad (8)$$

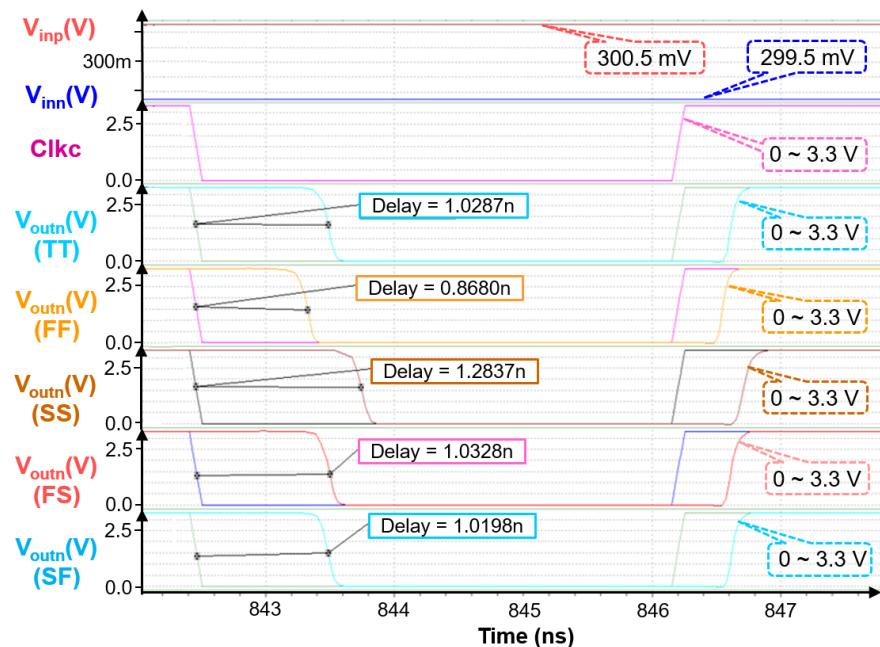
where  $V_{inp}$  is the positive input voltage,  $V_{ovi}$  the overdrive voltage of MC<sub>i</sub>, and  $V_{GSi}$  is the gate-to-source voltage of MC<sub>i</sub>.

Figure 16 shows the simulated output waveforms of the modified dynamic comparator at a constant common-mode voltage of 100 mV and a differential input voltage of 1 mV. In the 10-bit PLL-SAR ADC, the differential input voltage of 1 mV is approximately 0.25 LSBs. Moreover, the simulated power spectrum density (PSD) shows that the resolution is approximately 12 bits, which fulfills the requirement of the 10-bit PLL-SAR ADC. Figures 17 and 18 illustrate the propagation delays at five process corners with two

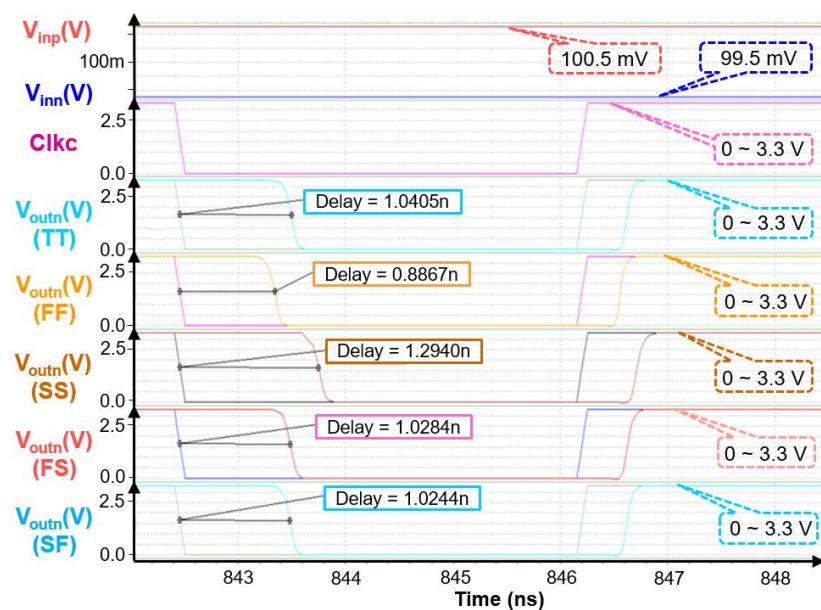
common-mode voltages of 300 and 100 mV, respectively. Notably, the propagation delays between FF and SS at the common-mode voltages of 300 and 100 mV are of 415.7 and 407.3 ps, respectively. These values imply that the aforementioned propagation delays are nearly constant and are unrelated to the common-mode voltage.



**Figure 16.** Simulated output waveforms  $V_{outp}$  and  $V_{outn}$  of the modified dynamic comparator at the constant common-mode voltage of 100 mV and differential input voltage of 1 mV.

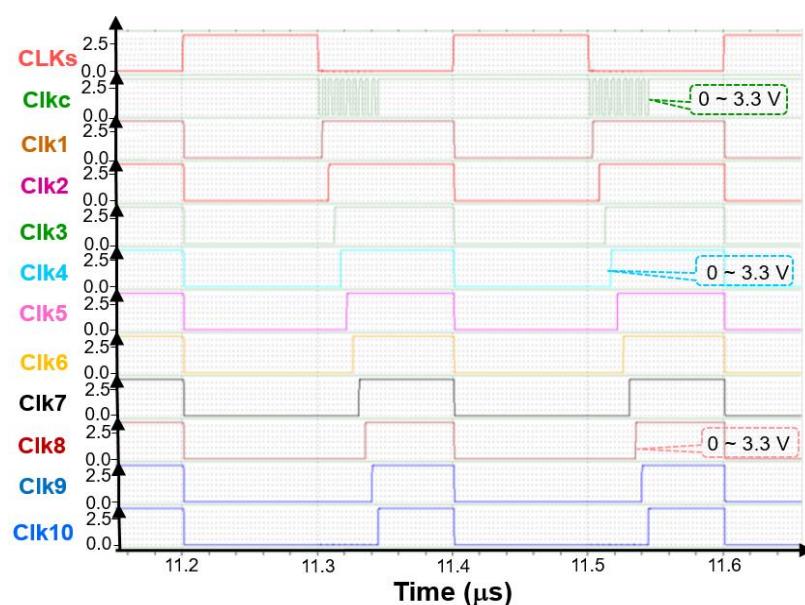


**Figure 17.** Simulated propagation delays at five process corners with common-mode voltage of 300 mV.



**Figure 18.** Simulated propagation delays at five process corners with common-mode voltage of 100 mV.

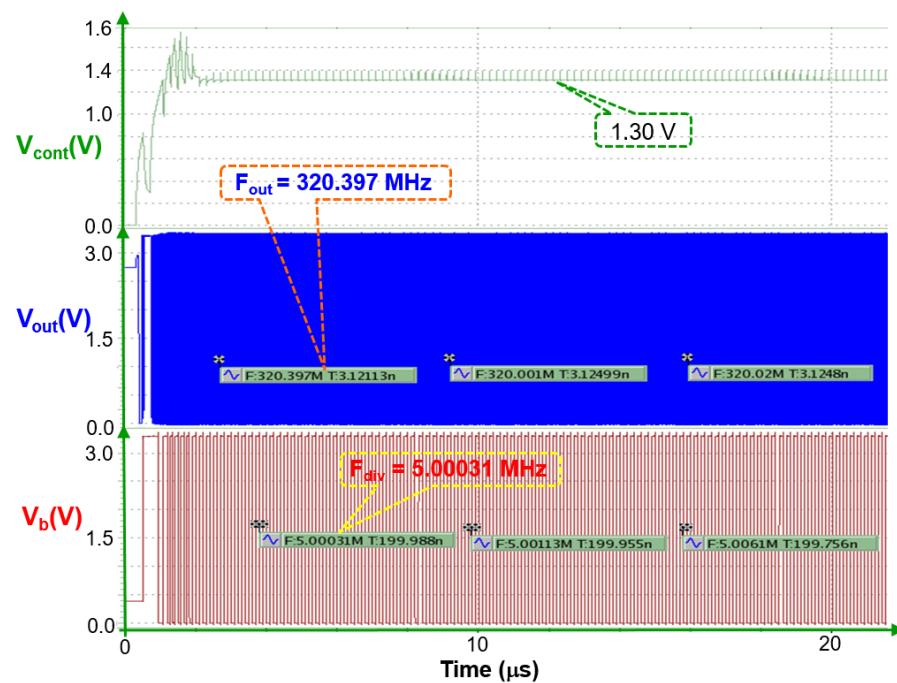
As shown in Figure 2, the clock signal  $CLK_s$  is used to control the switching states of the DAC switches  $S_0$ – $S_{10}$  and generate a comparison signal  $Clk_c$  after its passage through the SAR control logic. Because  $Clk_c$  is low, the comparison function is executed in the proposed dynamic comparator, and the reset function is activated. Figure 19 shows the simulated waveforms of the asynchronous control logic circuit.



**Figure 19.** Simulated waveforms of asynchronous control logic circuit.

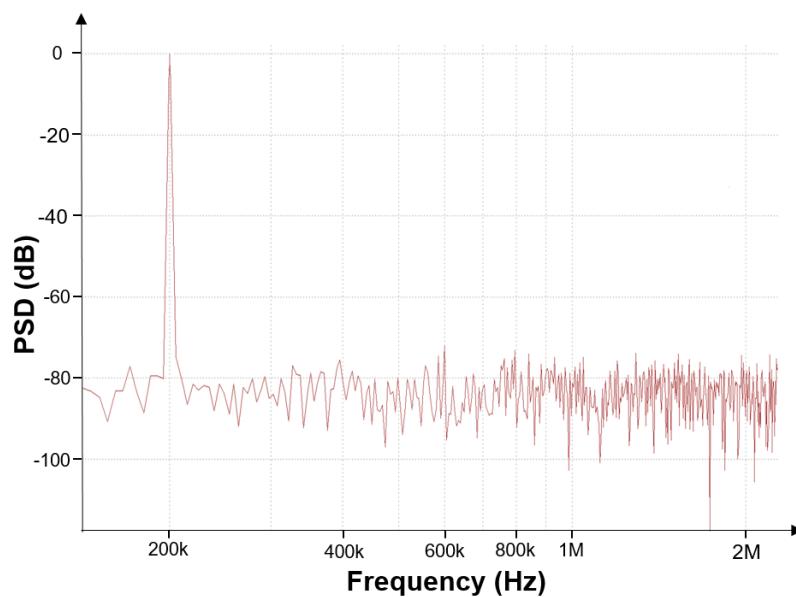
As shown in Figure 12, a six-stage DFF circuit was used to implement an FD for the PLL. The divide ratio of the divider circuit was set to 64. Figure 20 shows the simulated waveforms of the adopted FD at the control voltage  $V_{cont}$  of 1.30 V. The output frequency  $F_{out}$  of CS-VCO was 320.397 MHz, and the resulting feedback frequency  $F_{div}$  was 5.00031 MHz. Thus, the simulated divide ratio was approximately 64.075, which is close to the theoretical value of 64. These simulated results indicate that the designed FD circuit works correctly.

The feedback frequency  $F_{div}$  of 5.00031 MHz is fed to the clock signal  $CLKs$  in the S/H circuit and the asynchronous SAR control logic circuit, as illustrated in Figure 2.



**Figure 20.** Simulated waveforms of the adopted FD at the control voltage  $V_{cont}$  of 1.30 V.

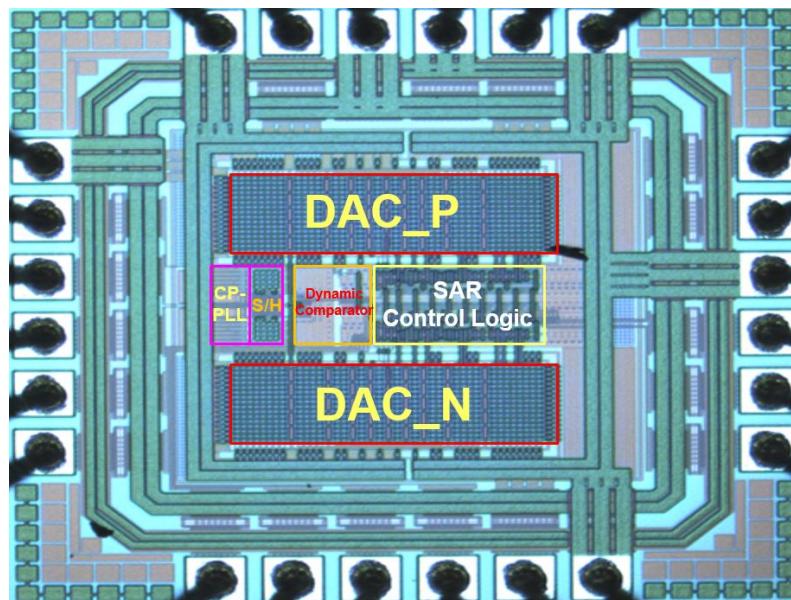
Figure 21 illustrates the post-layout simulated PSD of the proposed PLL-SAR ADC. According to the 32,768-point FFT simulation, the simulated SNDR was 58.23 dB, which is equal to 9.38 bits, at the input frequency of 200 kHz, sampling frequency of 5 MS/s, power supply of 3.3 V, and power consumption of 1256  $\mu$ W. Table 2 summarizes the post-layout simulated results of the proposed PLL-SAR ADC with three design corners, namely typical (TT), fast (FF), and slow (SS). The simulated DNL located between the  $-1.23$  and  $+1.81$  LSBs and the INL located between the  $-1.22$  and  $+1.81$  LSBs at the TT corner based on the input voltage varied from 0 to  $V_{DD}$ . The simulated resolution satisfied the PWM channel with an 8-bit resolution [23] and a 10-bit ADC [24] for BLDC motor control applications. Unfortunately, the DNL and INL perform with missing code because they are larger than 1.0 LSB. Figure 22 shows a chip microphotograph of the proposed PLL-SAR ADC. A separation alignment is considered to divide the large capacitor into two small capacitors and place them symmetrically. The small capacitor is placed at the center of the circle, whereas the large capacitor is in alignment outside of the circle. The parasitic impedance and capacitance can be reduced through adoption of a symmetric layout. Furthermore, temperature variation does not affect the resolution of the proposed SAR ADC between  $-40$  and  $100$  °C.



**Figure 21.** Post-layout simulated PSD of the proposed PLL-SAR ADC.

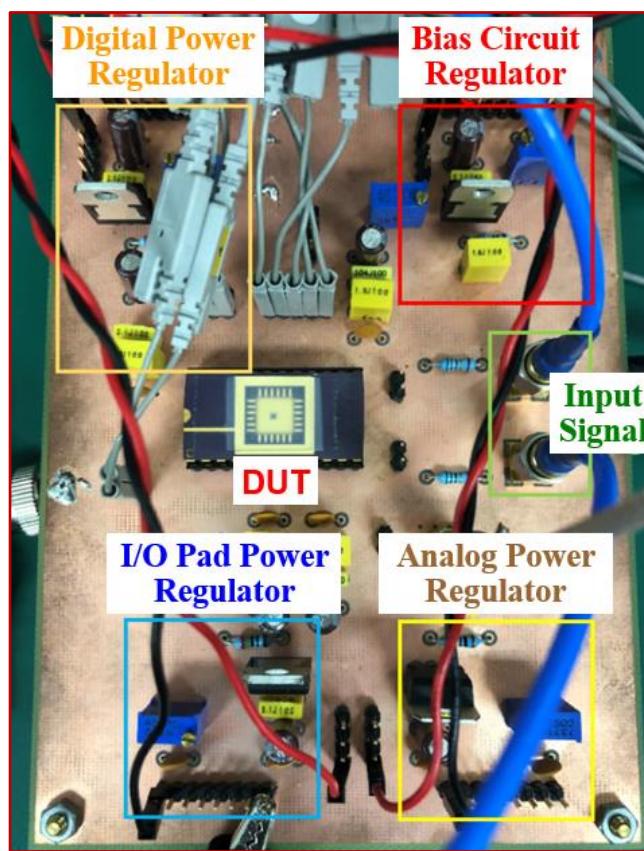
**Table 2.** Post-layout simulated results of the proposed PLL-SAR ADC circuit with three design corners.

Corners	TT	FF	SS
Technology ( $\mu\text{m}$ )	TSMC 0.25		
Power Supply (V)	$3.3 (V_{ddA})/2.5 (V_{ddd})$		
Input Range (V)	0–3.3		
$f_S$ (MS/s)	5		
$f_{in}$ (kHz)	200		
DNL (LSB)	+1.81 / -1.23	+1.57 / -0.92	+1.90 / -1.34
INL (LSB)	+1.81 / -1.22	+1.57 / -1.08	+1.90 / -1.28
SFDR (dB)	75.92	76.22	73.41
SNDR (dB)	58.23	58.65	57.51
ENOB (bits)	9.38	9.45	9.26
Power (mW)	1.256	1.482	1.025



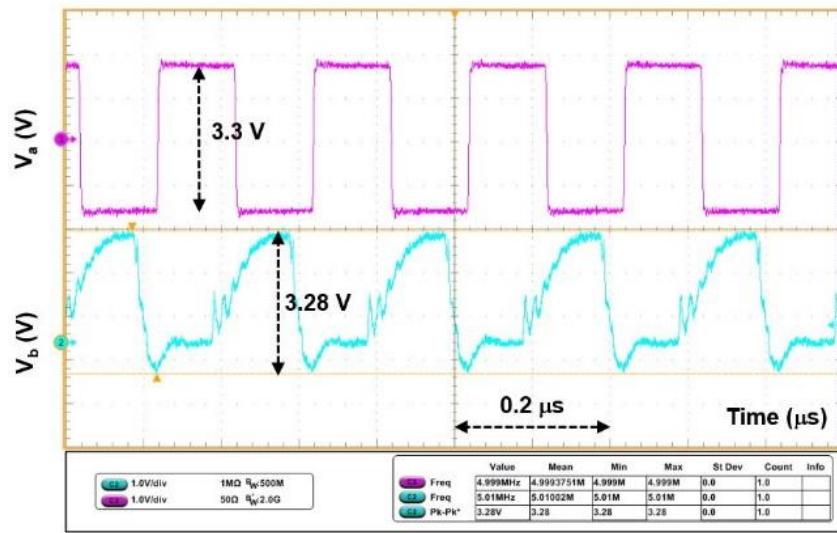
**Figure 22.** Chip microphotograph of the proposed PLL-SAR ADC.

Figure 23 presents the measured printed circuit board (PCB) of the proposed PLL-SAR ADC with the device under test (DUT). The function generator (SRS DS360, Harpenden, UK) provided an input frequency of 200 kHz, the pulse data generator (Agilent 81130A, Ferrara, Italy) generated a clock frequency of 5 MS/s, and the power supply (Keysight E3631A, Santa Rosa, CA, USA) and reference voltage (Keysight N6761A, Santa Rosa, CA, USA) provided a power supply of 3.3 V and bias voltage of 2.25 V, respectively. The digital output code was captured with a logic analyzer (Agilent 16902B, Ferrara, Italy) and imported into the MATLAB environment to calculate the SNDR and ENOB. The digital power, bias power, I/O pad power, and analog power were separated to prevent power interference in the DUT, which was mounted onto the PCB. Many three-terminal adjustable voltage regulators LM317 can supply more than 1.5 A over an output voltage range of 1.25–37.0 V. This includes current limiting, thermal overload protection, and safe operating area protection [25].



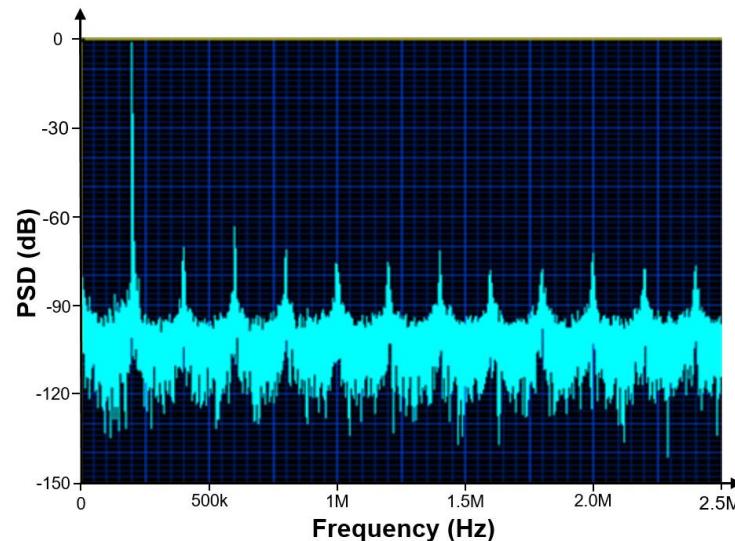
**Figure 23.** Measured PCB of the proposed PLL-SAR ADC with DUT.

Figure 24 illustrates the measured waveforms of input signal and feedback signal of the proposed PLL. The magnitudes of the input signal  $V_a$  and the feedback signal  $V_b$  are 3.3 V and 3.28 V, respectively, at the sampling frequencies of 4.999 MHz and 5.01 MHz. The measured results also prove that the proposed PLL works successfully. Because of the correct PLL design, an internal clock signal of the PLL ( $PLL_{out}$ ) is provided to guarantee that a correct clock signal ( $CLKs$ ) is obtained. That is, this study does not directly use the reference 5 MHz signal as the  $CLKs$ .

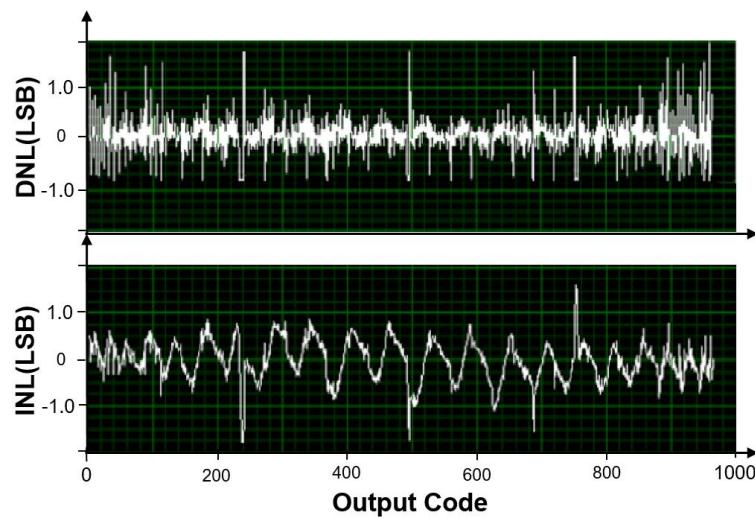


**Figure 24.** Measured waveforms of input signal  $V_a$  and feedback signal  $V_b$  of the proposed PLL.

Figure 25 presents the measured output 32,768-point PSD of the proposed PLL-SAR ADC at the input frequency of 200 kHz, sampling frequency of 5.0 MS/s, power supply of 3.3 V, and reference voltage of 2.25 V. When a full-scale input sine wave was considered at the input frequency of 200 kHz, the proposed PLL-SAR ADC yielded an SNDR of 53.82 dB, which was approximately 8.65 bits. The measured ENOB of 8.65 bits is inferior to the simulated ENOB of 9.45 bits. The reason is that the output voltage performs with nonlinearity in capacitive DAC. Fortunately, the measured resolution of 8.65 bits fulfills the specification of the PLL-SAR ADC in the BLDC motor drive because the PWM register contains an 8-bit channel with clock frequencies of 0.25–8.0 MHz [24]. The DNL and INL are depicted in Figure 26. The measured DNL varied from  $-0.80$  LSB to  $+1.94$  LSB, and the measured INL varied from  $-1.80$  LSB to  $+1.62$  LSB. The proposed PLL-SAR ADC operated with missing code because the measured DNL and INL were larger than 1.0 LSB. Fortunately, most of the measured DNL and INL values varied from  $-1.00$  LSB to  $+1.00$  LSB, and the few relatively large INL/DNL values can be attributed to the parasitic capacitance and the clock feedthrough phenomenon from the N- and P-type input stages. Moreover, the second-order effects such as channel-length modulation and mismatch effects inside the S/H circuit must be addressed in future studies [26].

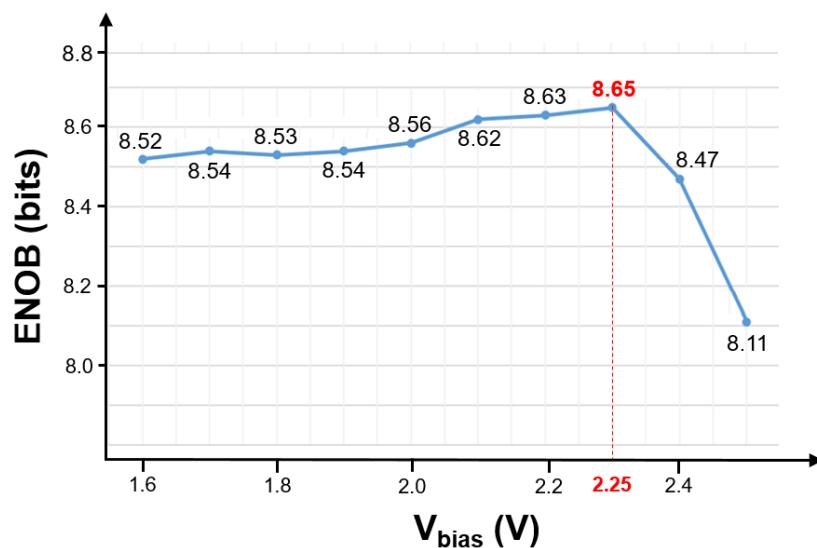


**Figure 25.** Measured 32,768-point PSD of the proposed PLL-SAR ADC at input frequency of 200 kHz.



**Figure 26.** Measured DNL and INL of the proposed PLL-SAR ADC.

Figure 27 shows the measured ENOB with respect to the bias voltages of 1.6–2.4 V at the input frequency of 200 kHz and sampling frequency of 5.0 MS/s. The measurements for the ENOB were uniform from 1.6 to 2.25 V, and the maximum ENOB of 8.65 was observed at 2.25 V. The ENOB decreased sharply when the bias voltage exceeded 2.25 V. As summarized in Table 2, the post-layout simulated SNDR of 58.23 dB can be compared with the measured SNDR of 53.82 dB. The difference is small because the modified two-stage dynamic comparator can prevent kickback noise, whereas the modified S/H circuit reduces the clock feedthrough with a dummy switch and eliminates charge injection with a dummy transistor.



**Figure 27.** Measured ENOB with respect to bias voltages of 1.6–2.4 V at the input frequency of 200 kHz and sampling frequency of 5.0 MS/s.

All characteristics of the proposed 10-bit 5-MS/s PLL-SAR ADC with modified bootstrapped switch for BLDC motor drive were successfully verified. Table 3 summarizes the measured properties of the proposed PLL-SAR ADC developed herein and compares them with those of other SAR ADCs. The performance comparison proved that the power consumption of this chip is lower than that of the SAR ADCs developed in [7,27] and that the measured ENOB in this study is superior to that reported in [7,13,28]. The proposed CDAC consumes a power of 660  $\mu$ W, which is approximately 52.5% of total power

consumption. Furthermore, the FoM of 0.625 pJ/conv-step measured in this study is superior to the reported value of 3.317 pJ/conv-step in [13], 7.403 pJ/conv-step in [27], and 30.873 pJ/conv-step in [28]. Notably, the proposed PLL-SAR ADC achieves the highest sampling rate (5.0 MS/s). Unfortunately, the measurements for the DNL and INL of this study were inferior to those of the compared SAR ADCs. The post-layout simulated SNDR was 58.23 dB, which is equivalent to an ENOB of 9.38, whereas a lower ENOB of 8.65 was measured for our implemented chip. That is, the chip fabricated in this study is affected by nonlinear CDAC, clock feedthrough error, process variation, and thermal noise.

**Table 3.** Performance summary and comparison with other SAR ADCs.

Reference (Year)	[27] (2008)	[7] (2018)	[28] (2020)	[13] (2021)	This Work (2021)
Technology	0.25-μm	0.18-μm	40-nm	0.25-μm	0.25-μm
Supply Voltage (V)	3.3/2.5	1.8	1.0	3.3/2.5	3.3/2.5
Resolution (bits)	12	—	—	10	10
Sampling Rate (MS/s)	0.0555	20	0.0028	0.909	5.0
Measured ENOB (bits)	—	7.8	6.4	8.11	8.65
Measured DNL (LSB)	—	+0.30/-0.60	+1.9/-0.3	-0.50/0.99	+1.94/-0.80
Measured INL (LSB)	—	+0.25/-0.62	+1.5/-1.5	-0.17/1.28	+1.62/-1.80
Power (mW)	1.683	2.460	0.0073	0.833	1.256
Core Area (mm <sup>2</sup> )	2.558	0.945	0.003	1.323	1.229
FoM * (pJ/conv-step)	7.403	0.552	30.873	3.317	0.625

$$* \text{FoM} = \frac{\text{Power (pJ)}}{2^{\text{ENOB}} \times f_s}.$$

#### 4. Conclusions

In this paper, we propose a 10-bit 5.0 MS/s PLL-SAR ADC with a modified bootstrapped switch for BLDC motor drives. The monotonic capacitor-switching procedure reduced power consumption and switching noise. In the proposed sample-and-hold circuit, a dummy switch and dummy transistor were added to reduce clock feedthrough and eliminate charge injection. This design eliminated the disturbed input voltage and enhanced the antinoise capability. Next, a two-stage dynamic comparator was developed to prevent kickback noise caused by the parasitic capacitance and achieve insensitivity to the input signal. The difference between the pre-layout simulated PSD and the post-layout simulated PSD was limited to 3 dB, which is equivalent to 0.5 bits. Moreover, this simulated result demonstrates that the chip layout can be completed carefully with separation alignment through division of the large capacitor into two small capacitors and their placement at a common centroid. A comparison with previously reported SAR ADCs revealed that the main advantages of the proposed PLL-SAR ADC are its high sampling rate of 5.0 MS/s, low power consumption of 1.256 mW, and high measured resolution of 8.65 bits. The FoM of 0.625 pJ/conv-step measured in this study is superior to the values reported in [13,27,28]. Unfortunately, the measured DNL and INL noted in this study were inferior to those of the compared SAR ADCs. To meet the system-on-chip (SOC) and industrial requirements, we need to integrate the proposed SAR ADC and the control circuits of electric vehicle into a single chip. It includes a digital controller, a channel register, an ADC controller, a gate driver, various detectors, a designed SAR ADC, a direct current–direct current (DC–DC) buck converter, and an inverter and is implemented in a TSMC 0.25-μm high-voltage complementary metal oxide semiconductor (CMOS). Further, two clock signals, an external clock signal and an internal clock signal from the CP-PLL, are provided to guarantee that a correct clock signal is fed. This design improves the robustness of the designed system. In this study, the authors were limited to designing the SAR ADC by using the TSMC 0.25-μm 1P3M CMOS process. The main limitation is that an N-type buried layer is used to withstand high voltage through sharing of the bodies of all PMOSFETs. This study needs to avoid shorting the source and body in the PMOSFETs, especially in circuit design and chip layout. The use of a more advanced CMOS process can significantly improve the performance of the SAR ADC developed in this study, such as the use 65-nm CMOS technology [29].

**Author Contributions:** Conceptualization, G.-M.S., C.-C.H., X.X. and S.-Y.H.; methodology, C.-C.H. and S.-Y.H.; formal analysis, C.-C.H. and S.-Y.H.; investigation, C.-C.H. and S.-Y.H.; writing, review, and editing, G.-M.S., C.-C.H. and S.-Y.H.; supervision, G.-M.S. and X.X.; project administration, G.-M.S.; funding acquisition, G.-M.S. and X.X. All authors have read and agreed to the published version of the manuscript.

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## References

1. Liu, M.; Ma, R.; Liu, S.; Ding, Z.; Zhang, P.; Zhu, Z. A 5-GHz low-power low-noise integer-N digital subsampling PLL with SAR ADC PD. *IEEE Trans. Microw. Theory Tech.* **2018**, *66*, 4078–4087. [[CrossRef](#)]
2. Liu, C.C.; Kuo, C.H.; Lin, Y.Z. A 10 bit 320 MS/s low-cost SAR ADC for IEEE 802.11ac applications in 20 nm CMOS. *IEEE J. Solid-State Circuits* **2015**, *50*, 2645–2654. [[CrossRef](#)]
3. Sathyan, A.; Milivojevic, N.; Lee, Y.J.; Krishnamurthy, M.; Emadi, A. An FPGA-based novel digital PWM control scheme for BLDC motor drives. *IEEE Trans. Ind. Electron.* **2009**, *56*, 3040–3049. [[CrossRef](#)]
4. Oh, J.; Heo, S.; Kim, M.; Suk, J.H.; Yang, Y.; Kim, J. High performance of PMSM driver IC integrated sensorless and current sensing circuits. In Proceedings of the 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Prague, Czech Republic, 12–16 June 2016; pp. 251–254.
5. Akin, B.; Clearman, C. *Digital Motor Control Methodology for C2000<sup>TM</sup> Real-Time Control Microcontrollers*; Texas Instruments (TI): Dallas, TX, USA, 2010; pp. 1–11.
6. Roy, A.; Agarwal, N.; Kulkarni, P.K.; Boosi, P.J. MCU-integrated PGA in 65nm CMOS with sub-1% gain error, 180ns acquisition window, and programmable output filter for motor control. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 27–30 May 2018; pp. 1–5.
7. Suna, A.; Çevik, I.; Yelten, M.B. A high speed 180 nm CMOS cryogenic SAR ADC. In Proceedings of the 18th Mediterranean Microwave Symposium (MMS), Istanbul, Turkey, 31 October–2 November 2018; pp. 116–119.
8. Lai, W.C.; Korkmaz, S.A. ADC and PLL for optical sensors in depth and virtual reality augmented reality applications. In Proceedings of the IEEE Int. Conf. on Consumer Electronics-Taiwan (ICCE-TW), Taichung, Taiwan, 19–21 May 2018; pp. 1–2.
9. Du, J.; Siriburanon, T.; Hu, Y.; Govindaraj, V.; Staszewski, R.B. A 2.02–2.87-GHz –249-dB FoM 1.1-mW digital PLL exploiting reference-sampling phase detector. *IEEE Solid-State Circuits Lett.* **2020**, *3*, 158–161. [[CrossRef](#)]
10. Liu, C.C.; Chang, S.J.; Huang, G.Y.; Lin, Y.Z. A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure. *IEEE J. Solid-State Circuits* **2010**, *45*, 731–740. [[CrossRef](#)]
11. Fayomi, C.J.B.; Roberts, G.W.; Sawan, M. Low-voltage CMOS analog bootstrapped switch for sample-and-hold circuit: Design and chip characterization. In Proceedings of the IEEE International Symposium on Circuits and Systems, Kobe, Japan, 23–26 May 2005; pp. 2200–2203.
12. Swindlehurst, E.; Jensen, H.; Petrie, A.; Song, Y.; Kuan, Y.C.; Chang, M.C.F.; Wu, J.T.; Chiang, S.H.W. An 8-bit 10-GHz 21-mW time-interleaved SAR ADC with grouped DAC capacitors and dual-path bootstrapped switch. *IEEE Solid-State Circuits Lett.* **2019**, *2*, 83–86. [[CrossRef](#)]
13. Huang, C.C.; Sung, G.M.; Xiao, X.; Sung, S.H.; Huang, C.H. Ten-bit 0.909-MHz 8-Channel dual-mode successive approximation ADC for a BLDC motor drive. *Electronics* **2021**, *10*, 830. [[CrossRef](#)]
14. Razavi, B. *Design of Analog CMOS Integrated Circuits*; McGraw-Hill Companies: New York, NY, USA, 2001; pp. 421–422.
15. Nitinaware, S.R.; Tijare, A.D.; Matey, M.M. Design of binary architecture for successive approximation analog-to-digital converter. In Proceedings of the Int. Conf. on Communications and Signal Processing (ICCP), Melmaruvathur, India, 2–4 April 2015; pp. 0512–0516.
16. Li, S.; Guo, Y.; Liu, Y.; Chen, J.; Xu, Q.; Zhang, J. A 1.2 V 12 bits SAR ADC with a two stages amplifier full-scale differential dynamic comparator. In Proceedings of the 10th International Conference on Communications, Circuits and Systems, Chengdu, China, 22–24 December 2018; pp. 22–24.
17. Jiang, S.; Do, M.A.; Yeo, K.S.; Lim, W.M. An 8-bit 200-MS/s pipelined ADC with mixed-mode front-end S/H circuit. *IEEE Trans. Circuits Syst.* **2008**, *55*, 1430–1440. [[CrossRef](#)]

18. Mann, A.; Karalkar, A.; He, L.; Jones, M. The design of a low-power low-noise phase lock loop. In Proceedings of the 11th Int. Symp. on Quality Electronic Design (ISQED), San Jose, CA, USA, 22–24 March 2010; pp. 528–531.
19. Chen, X.; Cai, L.; Xu, Y.; Ou, J.C.; Liao, J.W. A 0.13um low phase noise and fast locking PLL. In Proceedings of the IEEE 4th Advanced Information Technology, Electronic and Automation Control Conf. (IAEAC), Chengdu, China, 20–22 December 2019; pp. 1468–1471.
20. Mishra, A.; Sharma, G.K. Design of power optimal, low phase noise three stage current starved VCO. In Proceedings of the Annual IEEE India Conference (INDICON), New Delhi, India, 17–20 December 2015; pp. 1–4.
21. Wei, H.J.; Meng, C.; Chang, Y.W.; Lin, Y.C.; Huang, G.W. A high-speed HBT prescaler based on the divide-by-two topology. In Proceedings of the Asia-Pacific Microwave Conference, Bangkok, Thailand, 11–14 December 2007; pp. 1–4.
22. Muller, M. D Flip Flop with Asynchronous Reset Circuit Design, Electrical Engineering Stack Exchange Network. Available online: <https://electronics.stackexchange.com/questions/509643/d-flip-flop-with-asynchronous-reset-circuit-design> (accessed on 6 January 2022).
23. Kramolis, J. 3-Phase Sensorless BLDC Motor Control Development Kit with MC9S12G128 MCU; Application Note, AN4558, NXP; Freescale Semiconductor Inc.: Austin, TX, USA, 2012; pp. 1–40.
24. 3 Phase PMSM/BLDC Motor Controller, RT7100, BLDC Motor Drivers, Richtek Technology Corporation, Hsinchu, Taiwan. Available online: [https://www.richtek.com/Products/Motor/Motor%20controller/RT7100?sc\\_lang=en&fixLang=zh-TW](https://www.richtek.com/Products/Motor/Motor%20controller/RT7100?sc_lang=en&fixLang=zh-TW) (accessed on 6 January 2022).
25. LM317 3-Terminal Adjustable Regulator Datasheet. Texas Instruments (TI): Dallas, TX, USA, 2020; pp. 1–32. Available online: <https://www.ti.com> (accessed on 6 January 2022).
26. Hong, H.C.; Lee, G.M. A 65-fJ/conversion-step 0.9-V 200-kS/s rail-to-rail 8-bit successive approximation ADC. *IEEE J. Solid-State Circuits* **2007**, *42*, 2161–2168. [[CrossRef](#)]
27. Chiang, C.T.; Huang, Y.C. A 12-bit multi-channel non-calibrating dual-mode successive approximation ADC for power management bus (PMBus) devices. In Proceedings of the IEEE Instrumentation Instrumentation and Measurement Technology Conference, Victoria, BC, Canada, 12–15 May 2008; pp. 568–572.
28. Aiello, O.; Crovetti, P.; Alioto, M. Fully synthesizable low-area analogue-to-digital converters with minimal design effort based on the dyadic digital pulse modulation. *IEEE Access* **2020**, *8*, 70890–70899. [[CrossRef](#)]
29. Sunny, S.; Chen, Y.; Boon, C.C. A 4.06 mW 10-bit 150 MS/s SAR ADC with 1.5-bit/cycle operation for medical imaging applications. *IEEE Sens. J.* **2018**, *18*, 4553–4560. [[CrossRef](#)]