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The Analysis of High-Speed Low-Power Dynamic Comparators

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Abstract. This article reviews 5 different articles on optimizing comparators and focuses on their innovations. Many innovative methods are used to get a higher comparison speed, lower power consumption and degraded noise comparator. Many novel methods such as connecting the conventional two-stage dynamic comparator to a transconductance-enhanced latching stage, adding a charge pump to the Miyahara's comparator, engendering two propagating edges in two inverter loops and measuring the distance between the two edges to compare different input voltage and using an inverter-based input pair which is powered by a floating reservoir capacitor can significantly achieve these goals. What's more, a three-stage feedforward fully dynamic comparator with an extra parallel feedforward path, which is a completely innovatory and newly designed comparator, is also proposed.

1. Introduction

Comparators are the basic components of analog-to-digital converters, linking the analog and digital domains. They can not only work in an arithmetic logic circuit but also have extensive applications in many digital units. Thus, improving the parameters of a comparator can lead to a great effect on most ADC circuits. There are a multitude of parameters influencing the performance of a comparator, such as speed, power and noise. Actually, focusing on improving speed and power is a trend nowadays. Lots of work has been done these years. The change of speed and power of a comparator is attributed to various factors and the most prosperous way is to improve the circuit architecture. So many proposed comparators are manly focused on this aspect.

This paper demonstrates 5 previous structures mainly focusing on speed and power optimization between 2019 and 2020, summarizing their effort on the comparators. Then by using these summaries to present advanced circuits compared with traditional ones, which will inspire people and enhance the development of future comparator design. The second part shows the preview of each design, concisely introducing every work in each paper. While the detailed information is proposed in the third part. Finally, there is a conclusion part, it compares all these proposed comparators and analyses advantages and disadvantages of each work.

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2. Preview

Lots of work has improved the architecture based on the conventional comparators to optimize the performance.

Later, Yao Wang and his team represented a comparator with a transconductance-enhanced latching stage. The design had strong feedback thanks to its cross-coupled latch, making the PMOS dominant the delay. Therefore, Yao made some improvements in the topology.

Xiyuan Tang proposed the architecture of a pre-amplifier with a special capacitor in 2020. The design was focused on the energy-efficiency, which can indicate the power of a comparator. The structure was an improvement on DB integration which has a bad effect on differential-mode input.

Also, in 2020, Haoyu Zhuang and his colleagues showed a 60% faster speed comparator using a charge pump. The design was completely focusing on the speed but ignored the noise performance so that it could only be used in a special situation. However, it still provided an idea for future arts.

Some other work has made an innovation in the comparators.

In 2019, a three-stage feedforward fully comparator was proposed by Athanasios T.Rankaj. The latch part had 3 stages with a feedforward path. Each latch played a different role in the architecture, consequently making the delay lower than before. The structure was an evolution that provided a new way to reduce the delay.

Haoyu Zhuang also represented another design called edge-race comparator. Instead of speed, his team paid attention to low-power this time. Meanwhile, it can adjust different situations such as delay and noise automatically. The structure was a way to reduce the power consumption of LSB.

3. Proposed comparator

3.1. FIA

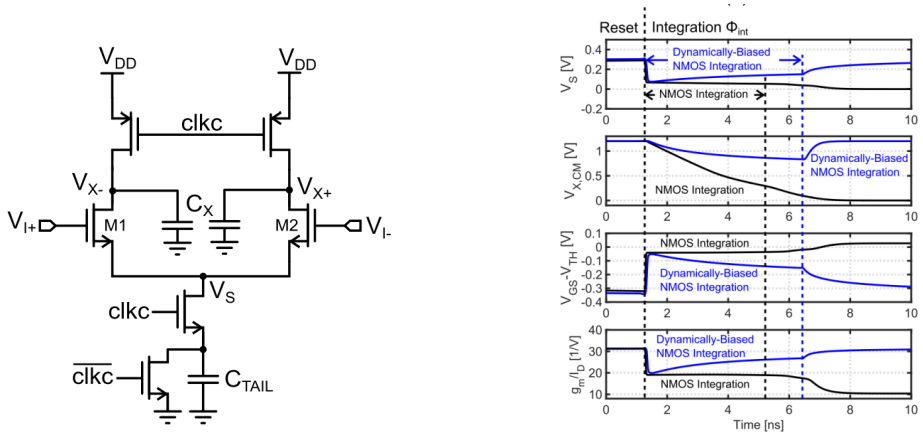
A comparator consists of a pre-amplifier and an SA-latch. Focusing on the pre-amplifier section [1], Xiyuan Tang's team suggests a new structure of the comparators in 2020 called Floating Inverter Pre-Amplifier with Reservoir Capacitor (FIA) [2]. It is energy-efficiency that the new structure has improved.

Energy efficiency can be expressed as the product of energy and noise power, where noise power can be influenced by g_m/I_d and loading capacitor C_X.

$$\sigma^2_{n,int} \approx \frac{I_D}{g_m} \cdot \frac{4kT\gamma}{V_{THN} C_X}. \quad (1)$$

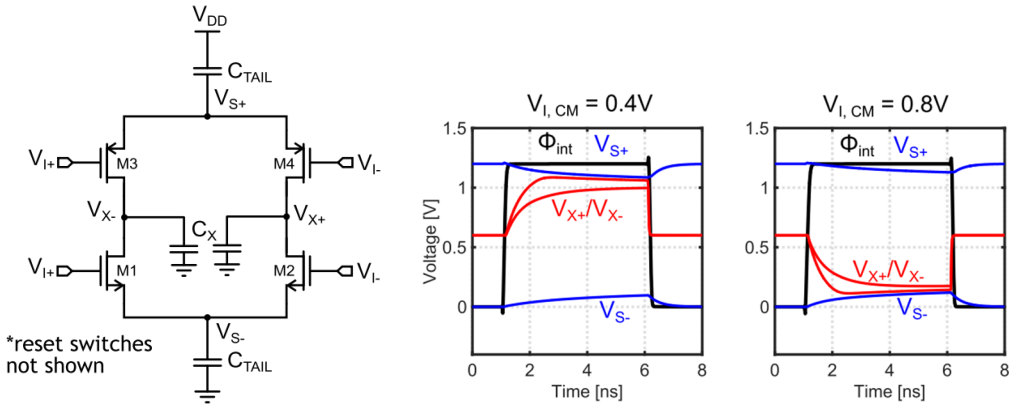
It is DB integration that improves both the 2 parameters above. As shown in Fig.1, DB integration adds a capacitor C_{TAIL} to the NMOS. In this way, g_m/I_d increases, and full discharging of C_X is prevented, making the energy efficiency better.

In this situation, adding another C_{TAIL} to PMOS seems possible to improve the energy efficiency of NMOS. Thus, CMOS DB integration is presented in Fig.2 (a). This will shorten the area between the bottom source node VS- and the upper source node VS+. As a result, the overdrive voltage of input pairs reduces. Consequently, the average gm/Id increases by about 2.5 times. However, the output voltage will have great disturbances due to VI, CM as shown in Fig.2 (b), which means NMOS or PMOS leads the whole manipulation.



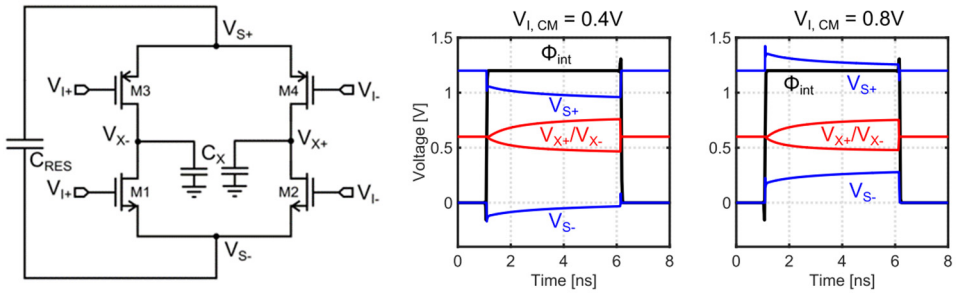
(a) (b)

Fig.1 (a) DB NMOS integration pre-amplifier model. (b)Simulated pre-amplifier behaviour.



(a) (b)

Fig.2 (a) Proposed CMOS DB integration model. (b) input common-mode voltage variation.



(a) (b)

Fig.3 (a) Proposed FIA powered by a floating reservoir capacitor. (b) $V_{I,CM}$ variation.

To overcome the difficulty, FIA is proposed in Fig.3(a). It is the great consideration that combining two C_{TAIL} into one C_{RES} prevents the common-mode variations and creates an area that is isolated from other parts of the comparator for the pre-amplifier. In this architecture, thanks to C_{RES}, I_{AMP+} is enforced to be equal to I_{AMP-}, diminishing the side effect of being short of CMFB. Besides, the isolated area will balance NMOS and PMOS automatically, preventing the common-mode variations further, as presented in Fig.3(b).

As described above, noise power has improved. Its analysis is based on the conventional one, which is related to the power spectral density (PSD) $S_i(t)$ and the magnitude squared impulse response ($|h_n(\tau)|^2$).

$$\sigma_o^2(t) = \frac{1}{2}\int_0^t S_i\,(t-\tau)\cdot|h_n(\tau)|^2 d\tau. \quad (2)$$

The formula can easily compute the noise of conventional NMOS integration pre-amplifier, DB integration pre-amplifier, and FIA.

$$\sigma_{in,SA}^2(T_{INT}) = \frac{2nKT}{V_{THN}\cdot C_X}\cdot\frac{I_D}{g_m}. \quad (3)$$

$$\sigma_{in,DB}^2(T_{INT}) = \frac{2nKT}{C_p\cdot\Delta V_{X,CM}(T_{INT})}\cdot\frac{I_D}{g_m}. \quad (4)$$

$$\sigma_{in,FIA}^2(T_{INT}) = \frac{2nKT}{C_{RES}\cdot\Delta V_S(T_{INT})}\cdot\frac{I_D}{G_m}. \quad (5)$$

Thanks to high Gm and CRES. FIA achieves the smallest noise.

Since noise reduces. Energy efficiency will be better. To calculate it, FoM is introduced as:

$$FoM = Energy\cdot(NoisePower). \quad (6)$$

It can be inferred that low FoM stands for high energy efficiency. Therefore, 3 types of the pre-amplifier's analysis are:

$$FoM_{SA} = \frac{4nKT\cdot V_{DD}^2}{V_{THN}}\cdot\frac{I_D}{g_m}. \quad (7)$$

$$FoM_{DB} = 4nKT\cdot V_{DD}\cdot\frac{I_D}{g_m}. \quad (8)$$

$$FoM_{FIA} = 4nKT\cdot V_{DD}\cdot\frac{I_D}{G_m}. \quad (9)$$

Since V_{DD} and G_m are always larger than V_{THN} and g_m, FoM_{FIA} will be the smallest one among the three. However, C_{RES} brings parasitic capacitance, which may influence the performance. Fig.4 shows its impact. Therefore, it can be inferred that its impact can be ignored.

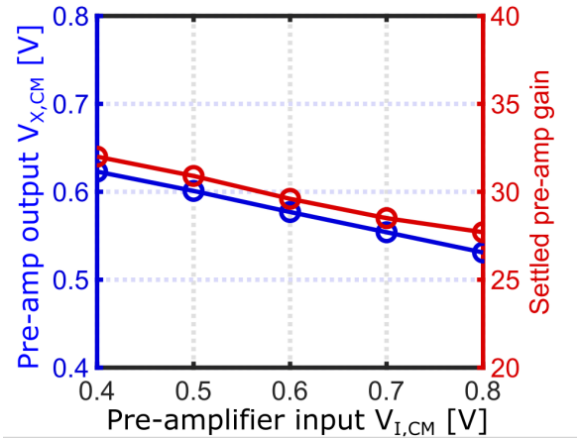
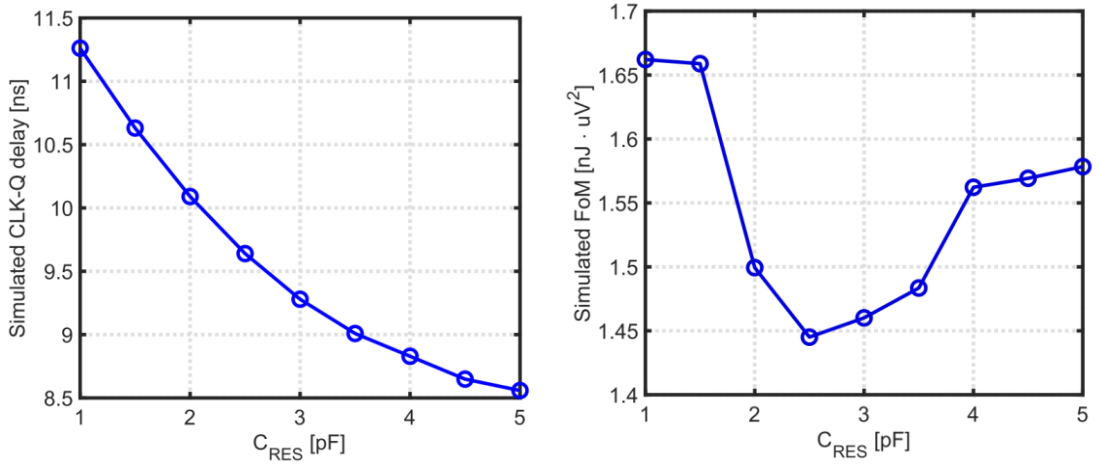


Fig.4 Simulated pre-amplifier output common-mode voltage and gain as a function of the input common-mode voltage.

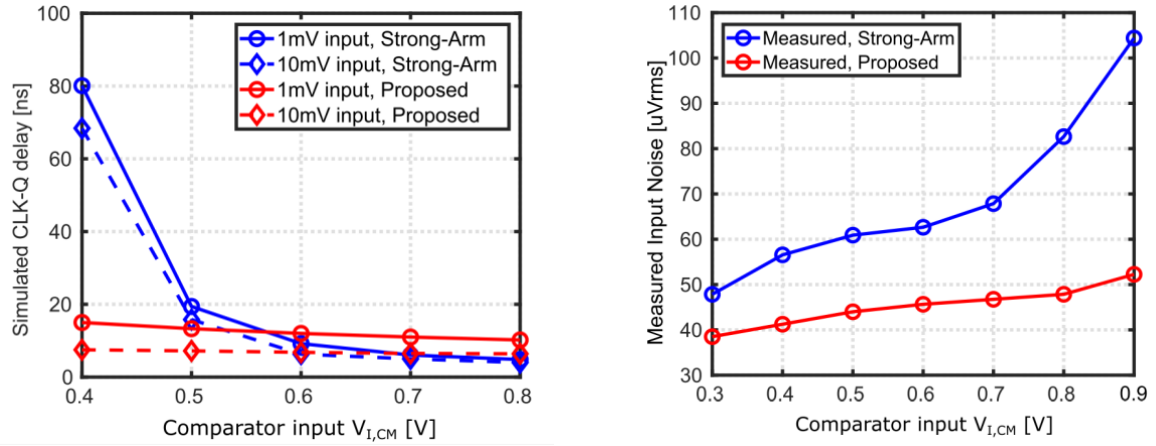
Besides energy efficiency, the delay is another important standard while designing. C_{RES} can directly influence the CLK-Q delay and FoM shown in Fig.5. It is clear that with C_{RES} increasing, the CLK-Q delay is decreasing. However, FoM fluctuates when C_{RES} changes, as presented in Fig.5 (b), which implies that neither a small C_{RES} nor a big one can optimize energy efficiency.

To identify the simulation above, 180-nm CMOS is used in the experiment. Fig.6 (a) and (b) compare CLK-Q delay and input noise as input $V_{I,CM}$ changing. Fig.7 presents the output probability with 1.2-V supply and 0.6-V input common-mode voltage.



(a) (b)

Fig.5 Simulated (a) CLK-Q delay with a 1-mV differential input and (b) energy efficiency of the proposed comparator versus CRES value.



(a) (b)

Fig.6 (a) Simulated CLK-Q delay versus input common-mode voltage. (b) Measured input-referred noise versus input common-mode voltage for the SA latch and proposed comparator.

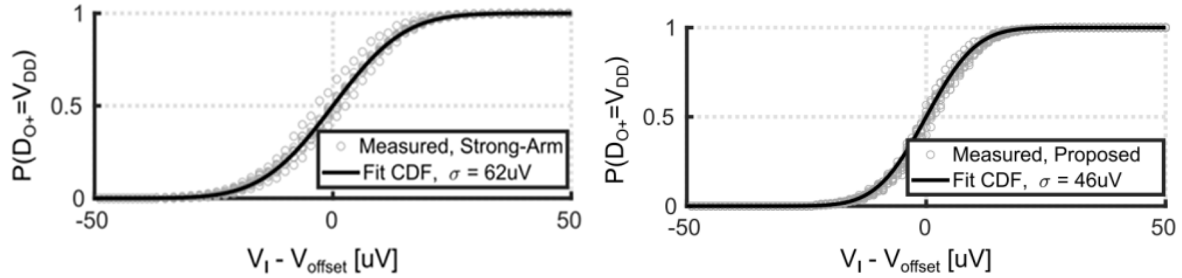


Fig.7 Measured cumulative probability density distribution and fit to Gaussian distribution for proposed comparator and SA latch with 1.2-V supply and 0.6-V input common-mode voltage.

3.2. A Triple-Latch Feedforward Dynamic Comparator

A three-stage feedforward fully dynamic comparator with an extra parallel feedforward path is introduced by Athanasios T.Ramkaj et al. [3].

The double-tail latch-type amplifier is demonstrated in Fig.8 [4]. It uses one tail for input stage and another for latching stage. Even at low $V_{DD,}$ it still works. Also, the double tail allows to tolerate a large current. However, it can't deal with a large delay. So, the three-stage comparator is based on this design.

The schematic of the proposed comparator is shown in Fig.9. The comparator consists of three cross-coupled latches and a feedforward. Stage-1 works as an amplifier totally, and stage-2 works as an amplifier and a latch. Finally, stage-3 just works as a latch to reduce the time of regeneration.

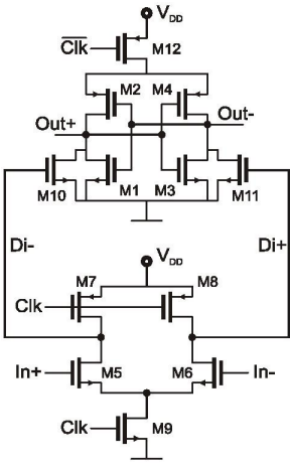


Fig.8 Double-tail latch-type amplifier.

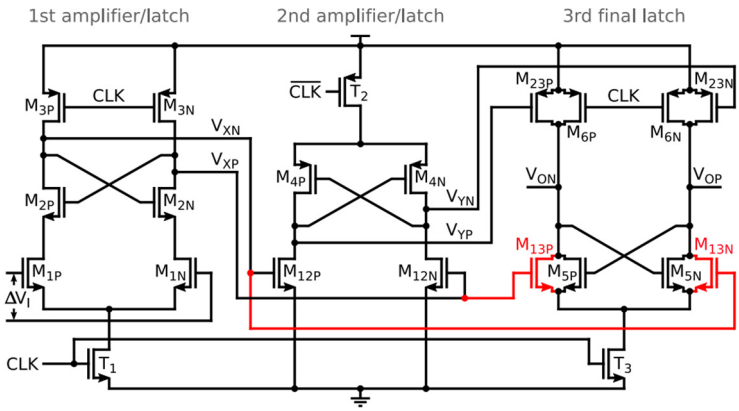


Fig.9 Schematic of the proposed comparator.

When CLK=0 V, T_1-T_3 cannot work while M_{3P}, M_{23P} and M_{6P} turn on. Then M_{12P}/M_{12N} and M_{23P}/M_{23N} work as reset and gain stages. When CLK=VDD, T_1-T_3 turn on, the direct path and the feedforward path both amplify the voltage difference generated at the drains of the input pair. When V_I is large enough, the signal transmits via the feedforward path more quickly than through stage-2, minimizing delay. Then after a while, signal from stage-2 can also enhance the difference. According to the analysis of the different decision paths, delay can be expressed as

$$\tau_{FF} \approx \begin{cases} \dfrac{\tau_2}{(1+g_{m12}/g_{m4})} + \dfrac{\tau_3}{(1+g_{m23}/g_{m5})} & small V_I \\ \dfrac{\tau_3}{(1+g_{m13}/g_{m5})} & large V_I \end{cases} \tag{10}$$

where g_{m12}, g_{m4}, g_{m13}, g_{m23}, g_{m5} are the transconductances of M_{12P}/M_{12N}, M_{4P}/M_{4N}, M_{13P}/M_{13N}, M_{23P}/M_{23N}, M_{5P}/M_{5N}, respectively, and τ_2, τ_3 are the time constants of stages-2 and 3. Based on Eq. (10), the delay is inversely proportional to g_{m12}/g_{m4}, g_{m23}/g_{m5}, g_{m13}/g_{m5}. So, the ratio of transconductances of different transistors considerably has a great impact on the delay. Then it can be concluded that a larger V_I can help decrease the delay. In other words, the proposed circuit works more quickly in the case of large V_I.

Fig.10 presents the simulated delay versus $\triangle V_I$ for different comparators [5]. Because V_{CM} and V_{DD} influence delay. The delay is simulated with fixed V_{CM}(0.5 V) and V_{DD}(1.0 V). All delays decrease with $\triangle V_I$ goes up. Obviously, the proposed comparator always behaves the best no matter what the $\triangle V_I$ is, benefiting from the new architecture. However, when $\triangle V_I$ is less than 10 mV, there is a slight difference between delays of the proposed one(TLFF) and 3-stage w/o FF. But after 10 mV, TLFF has an obvious advantage as expected. For a $\triangle V_I$ of 200 mV, the maximum difference between TLFF and 3-stage w/o FF is about 6 ps. To conclude, the proposed comparator works more quickly in the case of large V_I.

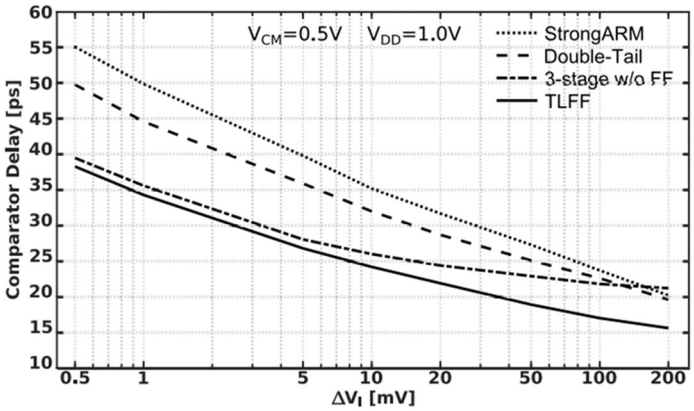


Fig.10 Simulated delay versus $\triangle V_I$ for different comparators.

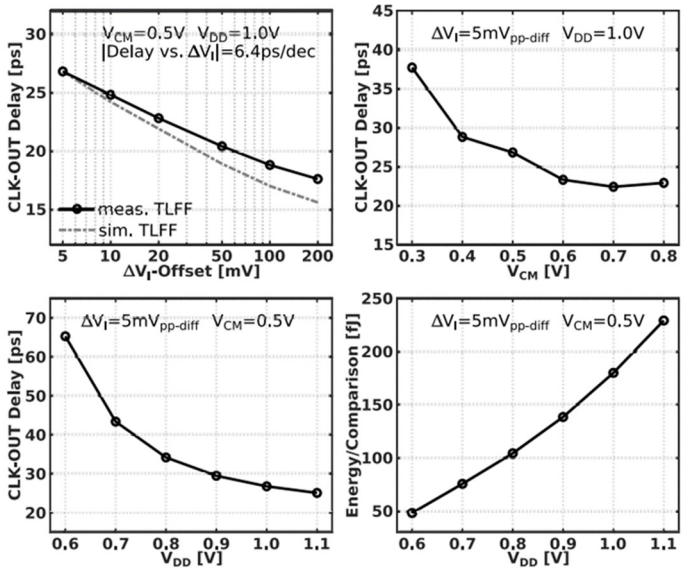


Fig.11 Measured TLFF comparator delay versus $\triangle V_I$ (top-left), VCM (top-right), VDD (bottom-left), and energy/comparison versus VDD (bottom-right).

Some essential design parameters are measured, including $\triangle V_I$, V_{CM} and V_{DD} in Fig.4. Firstly, the measured CLK–OUT TLFF delay versus$\triangle V_I$ is plotted in Fig. 11 (top-left). At large $\triangle V_I$, extra parasitic effects contribute a lot to the delay.

Secondly, the top-right graph shows measured delays versus V_{CM}. Again, there is a stable trend between 0.6 V and 0.8 V, but V_{CM} is set to 0.5 V when discussing the measured delay and energy consumption versus V_{DD} (bottom).

Finally, as the two bottom pictures show, the delay is inversely proportional to $V_{DD,}$ while the energy consumption is proportional to V_{DD}. Therefore, the derivative of curve Delay-V_{DD} goes down with the increase in $V_{DD,}$ and from 0.9 V to 1.1 V, the delay is suitable. However, in the same case, energy consumption is increasing sustainably. So, it is hard to find the best V_{DD} for minimum values of delay and energy consumption. As a result, V_{DD} is set to 1.0 V by compromise, which is reasonable for design.

3.3. A Low-Power High-Speed Dynamic Comparator With a Transconductance-Enhanced Latching Stage

YAO WANG et al. introduce a novel low-power, high-speed dynamic comparator [6]. This comparator includes a new transconductance-enhanced latching stage.

The new comparator is proposed based on a conventional two-stage dynamic comparator. Fig.12 shows the traditional architecture. There is a preamplifier stage and a latching stage. With the cross-coupled latching structure providing strong positive feedback, the large current helps enhance the speed.

However, only PMOS transistors influence the delay, which results in a lower speed and a higher energy. So, the proposed comparator deals with the problem. The schematic diagram for it is shown in Fig.13. It consists the same preamplifier and a proposed regenerative stage. When OUT_p and OUT_n are discharged from *VDD*, while D_p and D_n are going up from GND, M0-1 and M4-5 will work in the triode region at first and then the $g_{m,eff}$ increases, which leads to a higher regeneration speed. What's more, the comparator consumes less power due to a shorter metastable period of the novel structure.

According to the analysis, the decrease of delay mainly comes from t_{latch}, t_{latch} can be expressed as

$$t_{latch} = \frac{C_{OUT}}{g_{m,eff}} \cdot ln\frac{\Delta V_{out}}{\Delta V_0} = \frac{C_{OUT}}{g_{m,eff}} \cdot ln\frac{V_{DD}/2}{\Delta V_0} \tag{11}$$

Then the total delay of the comparator is given by

$$t_{delay} = \frac{C_{OUT}}{g_{m,eff}} \cdot ln\frac{V_{DD}/2}{\Delta V_0} + \frac{V_{THN}C_{OUT} \cdot 2\mu_P C_{OX}\frac{W_1}{L_1}}{g^2_{m,\ eff}} \tag{12}$$

As is shown in the formula, t_{latch} decreases with the improvement of $g_{m,eff}$ and the decline of $C_{OUT.}$ In conclude, the added M2 and M3 help enhance the effective transconductance to minimize the delay.

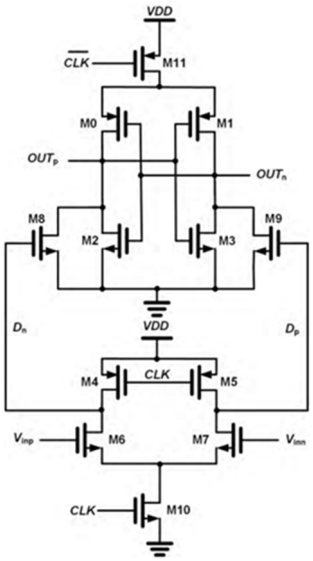


Fig.12 Conventional two-stage dynamic comparator.

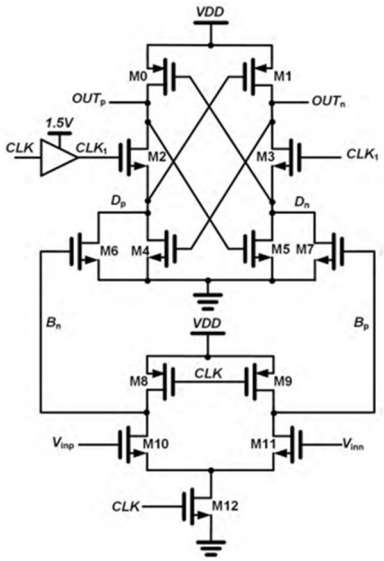


Fig.13 The proposed dynamic comparator

The widths of M2-3 are considered. Keeping bias voltage same, if the gate width increases, the conduction current will go up, leading to a smaller switch-on equivalent resistance and a larger parasitic capacitance. Then they can influence delay and power. But these are nonlinearity causes how they influence delay and power is not clear. Therefore, Fig.14 illustrates the simulated relationship between width of M2-3 and delay/power consumption. Considering when the width is larger than 1 μm, the delay keeps stable and the power consumption even grows. As a result, the designer chooses 1 μm as the width of M2-3 to keep a balance between the two performance indicators.

The writer generates a signal CLK1 that is a boosted and delayed signal from CLK, then the delay between CLK and CLK1 is t_{opm}. Different t_{opm} may have an impact on delay and power consumption. As shown in Fig.15. Energy keeps a decline. The delay decreases firstly and when t_{opm} is about 80 ps it surges. Obviously, we had better set t_{opm} to 95 ps. That is also the intersection of two curves, considering both delay and energy.

Fig.16 shows the simulated delay of different comparators and energy consumption versus V_{cm} at V_{id} = 50 mV and VDD=1.2 V. It shows that the new comparator works considerably faster than others by over 150 ps. Therefore, a suitable V_{cm} should also be considered to cater to delay and energy.

Then Fig.17 depicts the relationship between *VDD* and delay when V_{id} = 50 mV and V_{cm} = *VDD* – 0.1 V. Delay is the lowest from 1.1 V to 1.3 V while energy increases always. VDD is chosen as 1.2V.

Moreover, Fig.18 presents that simulated delay will decrease with the increase in different input voltages. So a larger V_{id} can be considered. The larger multiple input common-mode voltages also reduce the delay. When V_{cm}=0.7 V to 1.1V, there is not too much difference. As a consequence, the input common-mode voltage range is 0.7-1.2 V.

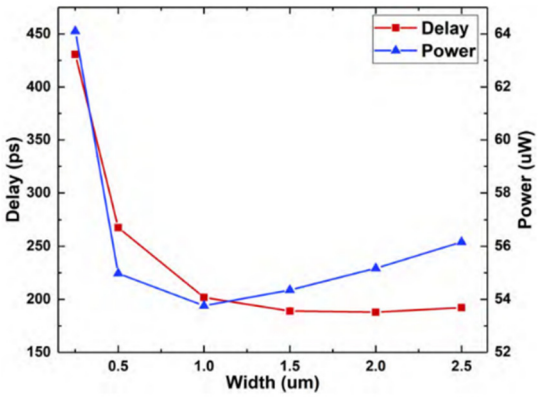


Fig.14 The relationship between the width of M2-3 consumption and delay/power consumption.

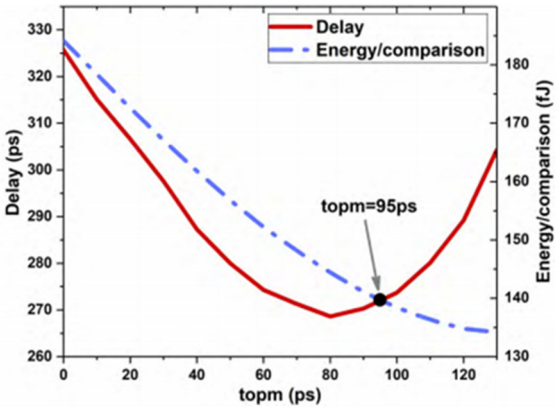


Fig.15 Simulated delay and energy versus t_{opm}.

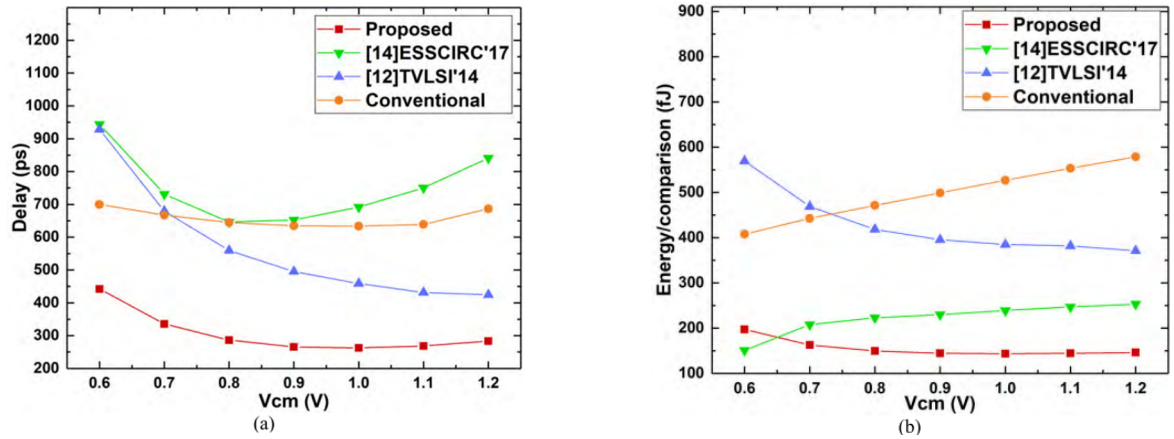


Fig.16 (a)The simulated delay of different comparators versus V_{cm} (b) energy consumption versus V_{cm} at V_{id}=50 mV and VDD=1.2 V.

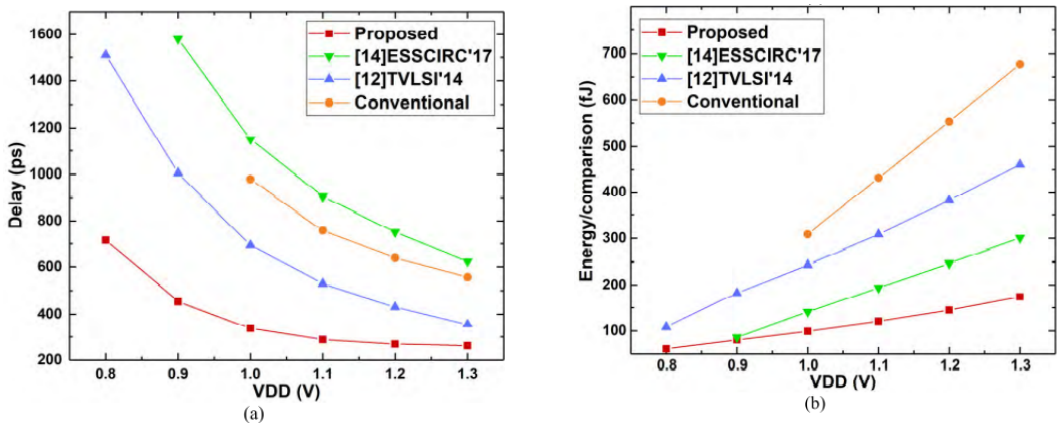


Fig.17 (a)the relationship between VDD and delay (b)VDD and energy when Vid = 50 mV and Vcm = VDD-0.1 V.

Considering the analysis about parameters before, different results between the measured and simulated should be considered to verify the design, as viewed in Fig.19.It is concluded that the measured value and simulated value are different because of environment. There should be a large current to drive load capacitance, which means that some buffer stages are added at the output of the comparator. Therefore, all these changes have a great impact on the delay and power. However, the two trends are roughly the same. To sum up, the design can work properly.

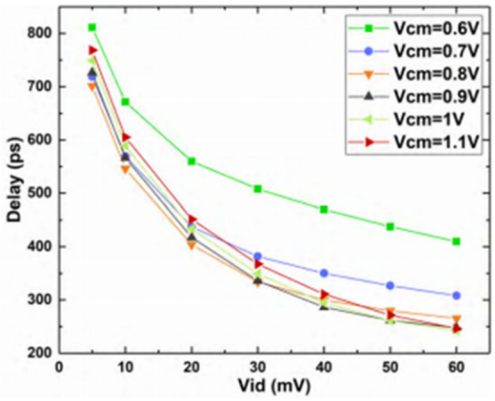


Fig.18 Post-layout simulated delay versus V_{id} (VDD = 1.2 V; V_{cm} = 0.7 V).

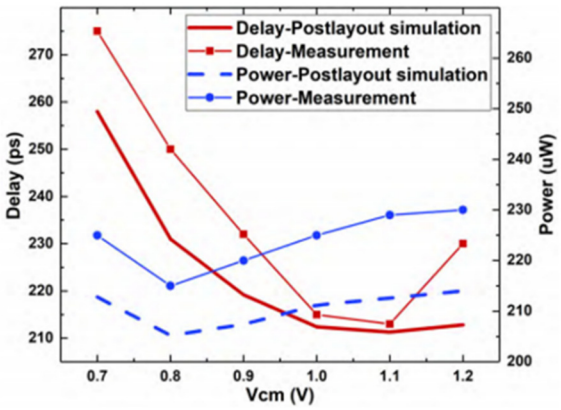


Fig.19 Delay and energy consumption versus Vcm (Vid = 0.1 V; VDD = 1.2 V; f = 2 GHz).

3.4. A novel comparator with a charge pump based on the conventional Miyahara's comparator

A voltage comparator with 60% faster speed by using a charge pump is proposed in this article [7]. The comparator, which can greatly increase the comparison speed while not degrading its noise performance, is well suited for SAR ADCs. Furthermore, an extra charge pump is added to the classic Miyahara's comparator [8], which significantly expedites the second-stage amplification and regeneration phases, leading to greatly accelerated comparison speeds. Meanwhile, the noise performance isn't degraded as the input pair transconductance of the second stage is increased while its integration time is decreased.

Fig.20 is the schematic of classic Miyahara's comparator. It's an optimized comparator based on the double-tail latch-type comparator, which has a shortcoming that the gain of the second stage is reduced. It will lead to a bigger input-referred noise of the comparator. By applying the PMOS input pair for the second stage, this problem is effectively solved in Miyahara's comparator. The second-stage input pair M6 ~M7 is in the saturation region at the start, which improves the second stage's gain significantly. As a result, there will be much smaller input-referred noise. Based on the analysis, the input-referred noise can be reduced by increasing input pair transconductance and integration time [7]. So, new technology is applied to Miyahara's comparator to improve speed and not degrade the noise performance.

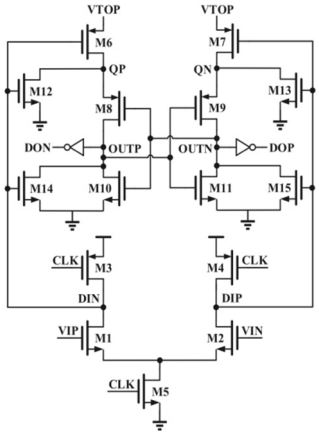
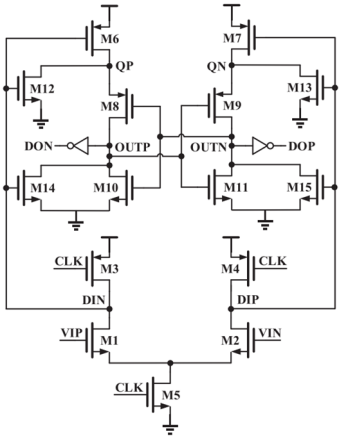


Fig.20 Miyahara's comparator.



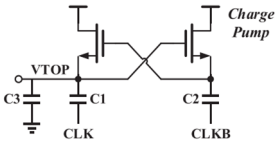


Fig.21 the novel comparator based on Miyahara's comparator.

Fig.21 is the schematic of the proposed comparator. The comparator process consists of three operation phases: the reset phase, the amplification phase, and the regeneration phase. In the reset phase (CLK = 0), DIP and DIN are reset to VDD, while OUTP, OUTN, QP, and QN are reset to GND.

In the amplification phase, DIP and DIN go down as CLK rises. At the same time, VTOP rises fleetly since CLK goes high, turning on M6~M7 and initializing the second-stage amplification phase. This process begins earlier than Miyahara's comparator because only when DIP and DIN go down to VDD-Vth to turn on M6~M7 will the second-stage amplification begins in Miyahara's comparator. Therefore, the proposed comparator puts second-stage amplification phase in advance, leading to an earlier beginning than Miyahara's comparator, which is helpful to improve the speed. Furthermore, because of bigger V_{gs} and the squared I-V relationship of the transistor, the current through M6~M7 is also bigger.

Fig.22 compared currents through M6, M12 and M14 for Miyahara's comparator and proposed comparator after CLK rises. From the simulation, not only does M6 turns on earlier in proposed comparator than that in the Miyahara's, and also the current I6 is about 600uA in proposed comparator, which is nearly 3 times bigger than Miyahara's comparator.Fig.23 shows the measured delay versus the differential input voltage, the delay of proposed comparator is 60% smaller than Miyahara's comparator.

When the second-stage amplification phase begins, DIP and DIN are nearly equal to VDD, rather than smaller than VDD − Vth in Miyahara's comparator. At this time, M12 ~ M13 have larger gate-source voltage, causing their larger current.It is also shown in the simulation chart of Fig.22 that the current I12 in the proposed comparator is about 3 times larger than Miyahara's comparator.

Totally, the proposed comparator has a larger current, which makes its amplification phase of the second stage faster. As a result, we can see from Fig.23 that the OUTP and OUTN of the proposed comparator rise more quickly than Miyahara's comparator. And this is also helpful to pick up the speed of comparison.

In the regeneration phase, M10 ~ M11 is turned on, and the comparison result is engendered by the positive feedback in the cross-coupled inverter. The regeneration speed in the proposed comparator is faster than Miyahara's comparator as it has a much larger current in M10 ~M11.

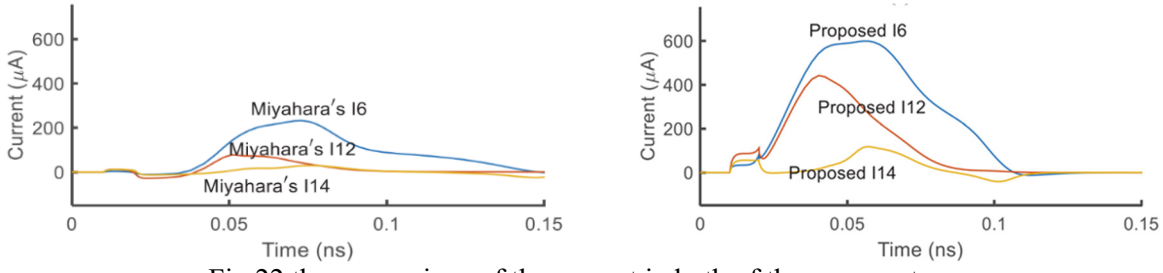


Fig.22 the comparison of the current in both of the comparators.

As we can see in Fig.23 that when the input voltage is equal to 0.5mV, the proposed comparator has a regeneration time 2 times shorter than Miyahara's comparator.

When it comes to the noise performance, although the integration time in the second stage decreases, which may have a negative effect on the noise performance, the promoted input pair transconductance of the second stage because of the larger current successfully offsetting the penalty. And by increasing the sizes of M12~M13 to expand the integration time of the second stage, the noise performance of the proposed comparator can be further optimized with ease.

To sum up, the proposed comparator can accelerate the comparison speed while not degrading the noise performance.

Fig.24 shows the measured delay versus the differential input voltage *VDIFF*. As can be known from the chart, the delay of the proposed comparator is 60% smaller than Miyahara's comparator because of the earlier, faster second-stage amplification phase and the accelerated regeneration phase when VDIFF is equal to 1mV, which perfectly correspond to the theoretical analysis and simulation experiment.

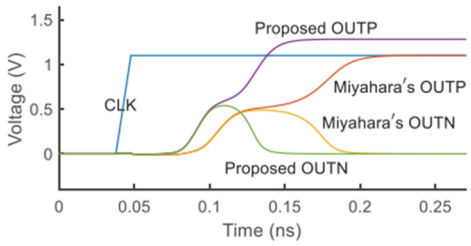


Fig.23 CLK, OUTP, and OUTN of the Miyahara's comparator and the proposed comparator.

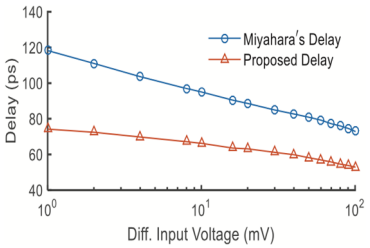


Fig.24 the measured delay versus the differential input voltage.

3.5. An edge-race comparator

An edge-race comparator (ERC), which is extremely suitable for low-power, high-resolution SAR ADCs, is proposed in this article [9]. It's not only low-power and low-noise but also doesn't need high-voltage headroom. Meanwhile, the comparator can adjust its power consumption, delay and noise automatically.

As for high-resolution SAR ADCs, a low-noise comparator that can recognize a small voltage difference at fine LSB decision is often needed. However, they're usually largely power-consuming at LSB decisions [10].

To overcome this problem, an edge-pursuit comparator (EPC) that can automatically adjust its delay, power and noise according to the comparator's input voltage is proposed. By this method, energy and time in coarse comparisons could be saved dramatically, and the noise in fine comparisons can be significantly degraded. However, the EPC still has a limitation that the delay in fine comparisons is so big that it only suits low-speed ADCs whose sampling rates is in the kS/s range. As a result, ERC is proposed in this article to solve this problem.

The proposed ERC consists of inverter delay units and NAND gates. The comparator inputs Vip and Vin control the delay of the delay units. In contrast to the circuit of EPC, we can find that the single loop in ERC is divided into two loops, which can accelerate the speed of comparison and reduce the interference between the two edges.

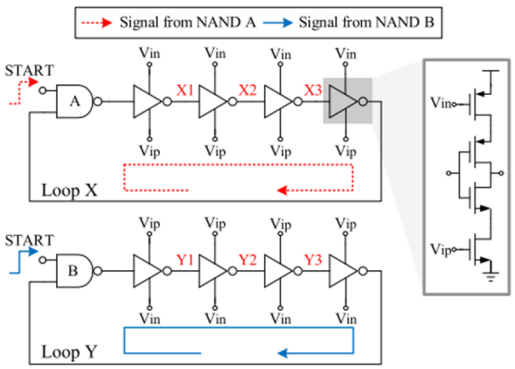


Fig.25 Circuit of ERC.

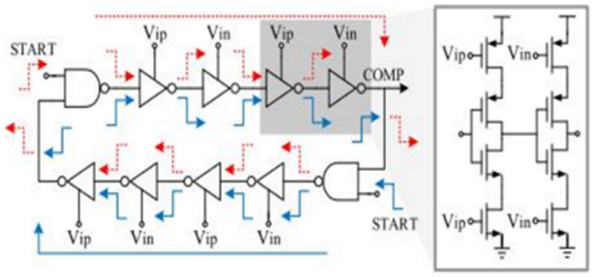


Fig.26 Circuit of EPC.

The process of the proposed ERC is as follows. The two loops are in the reset phase when START=0. Then, the two NAND gates generate two propagating edges in the two loops when START goes high to 1. The two edges start from the same starting line and race with each other, recursively propagating in the two loops. The distance between the two edges gradually increases as time goes on because of their different propagating speeds. At last, the race ceases when the distance exceeds a preset value d0, which is set to 2 inverter delays, and the winner, which is the comparison result, is determined. Then we have Vip >Vin when the edge in loop X is faster than loop Y, and vice versa.

In contrast, when START increases to 1, the two edges start from different positions in EPC loop. As a result, the initial distance between the two edges is equal to 5 inverter delays, and it can be concluded that the preset value d0 is 5 inverter delays for EPC.

From the analysis above, it's obvious that d0 in the proposed ERC is 2.5 times smaller than that in the EPC, leading to its faster comparison speed.

For both the EPC and the proposed ERC, the comparison time t_{comp} can be calculated as follow:

$$t_{comp} \approx \frac{C_L V_{DD} d_0}{g_{m(V_{ip}-V_{in})}} \tag{13}$$

As the energy consumption depends on comparison time t_{comp} greatly, which means the longer the comparison time is, the greater the energy consumption is. As a result, it can be seen from the formula that the comparator only consumes large energy when Vip-Vin is small, which is a fine comparison.

The noise of the proposed ERC is mostly generated by the inverter delay units in the loop. So the input-referred root mean square (rms) noise can be calculated as follows:

$$\sigma_n = \frac{1}{\sqrt{N \cdot C_L}} \frac{2I_{SS}\sqrt{\alpha k T}}{V_{DD} g_m} \tag{14}$$

It can be known from the formula that the noise of the proposed comparator can be decreased by increasing the length of the equivalent inverter chain.

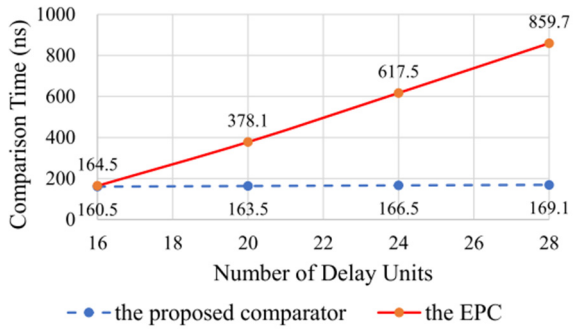


Fig. 27 Total number of delay units versus the comparison time.

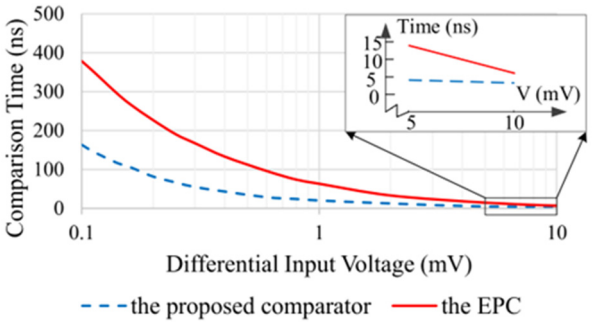


Fig. 28 Total number of delay units versus the comparison time.

Fig.27 is the simulation chart of total number of delay units versus the comparison time. The figureshows that the comparison time isn't related to the number of delay units in the proposed comparator because of the constant preset value d0. However, the comparison time raises linearly with the number of delay units in the EPC because of the increased preset value d0.

Fig.28 is the simulation chart of the differential input versus the comparison time (the total number of delay units is 20). The figure shows that the comparison time is inversely proportional to the differential input. And it's apparent that the comparison time of the proposed ERC is always about two times smaller than the EPC under different input voltages.

Fig.29 is the simulation chart of the differential input versus the energy per comparison. As the figure shows, the energy consumed by the proposed is about 1.6 times smaller than the EPC as the energy per comparison depends on the comparison time.

Fig.30 is the measurement chart of the average energy per comparison from the LSB to the MSB. At the LSB, the ERC energy is smaller than the EPC by 7.5 times because of the faster speed of the ERC.

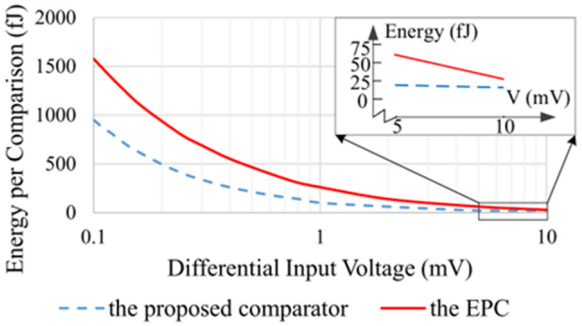


Fig.29 Energy per comparison versus differential input voltage.

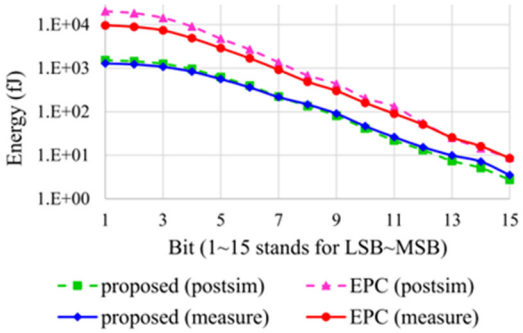


Fig. 30 Average energy per comparison versus SAR ADC bit position.

From both the simulation and measurement results, the conclusion that the proposed voltage comparator truly significantly accelerates the speed of comparison while reducing the power consumption compared to the EPC can be made.

Table Ⅰ illustrates the performance of five different comparators, which is organized as the CMOS technology [11]. The supply voltage doesn't change too much, but the delay and energy consumption has greatly improved. [7] decrease the delay considerably at the cost of larger energy consumption while [9] guarantees the energy consumption but ignore the delay. Therefore, different performances of a device should be compromised to adapt to various work environments. Also, most of these designs don't deal with the problem of noise. Only [9] and [2] consider it.

Table I. The performance of five comparators

	[3]	[9]	[6]	[2]	[7]
CMOS technology(nm)	28	40	180	180	——
Supply voltage(V)	1	——	1.2	1.2	——
Power consumption(μW)	2200	0.058	72.2	——	120000
Clock frequency(GHz)	13.5	——	2	——	1
Offset(mV)	——	1	7.3	——	1
Energy(fJ)	163	265.7	112.5	——	——
Noise(μV)	——	74	——	62	——
Area(μm^2)	——	——	252	7700	182
Delay(ps)	6.4ps/decade	54200	268.6		75

4. Conclusion

To conclude, a comparison of six comparators is given. As is shown in Table Ⅱ, some of the performance is optimized due to improvements in circuits. Most of these are proposed based on the conventional design. Then Y. Wang's work adds a new latch stage to the previous comparator circuit to further reduce the power and delay. H. Zhuang offers two innovations: one uses an extra charge pump to reduce delay, and the other utilizes inverter delay units together with NAND gates to achieve low-power and low-noise. Finally, X. Tang's work uses a floating inverter pre-amplifier with a reservoir capacitor to improve the energy efficiency of a comparator.

In particular, A. T. Ramkaj's work is totally different from others. The circuit is an innovation instead of an improvement on the basic circuit. Firstly, the circuit consists of three latch stages to guarantee a certain power's best gain and speed. Secondly, an extra parallel feedforward path between the second and third stages is chosen to reduce the delay. So it is an innovation of technology, which is different from other improvements of the circuit topology.

Finally, the balance between power consumption, delay, offset, etc., is still the fundamental problem of dynamic comparators. Therefore, it is concluded that the tendency of future research will consistently attach importance to the improvement of performance and integration.

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