COM4506/6506: Testing and Verification in Safety Critical Systems

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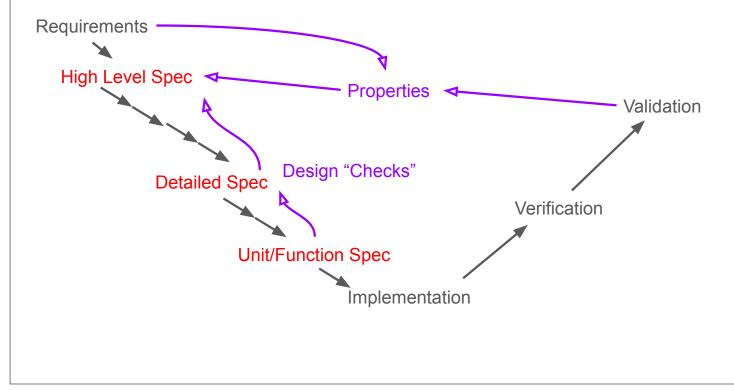


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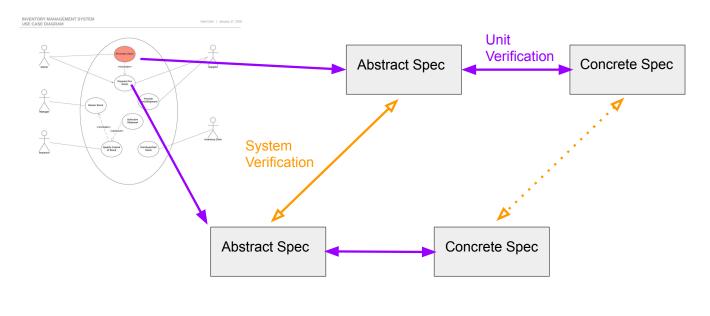
- Iterative Specifications in a Formal setting
- Formal Properties
- Refinement

Requirements High Level Spec Validation Unit/Function Spec Implementation

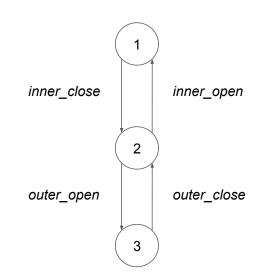
Iterative Specifications



System Components and Units



Formal Properties

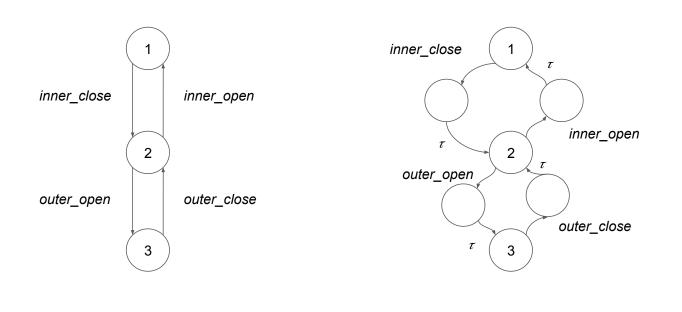


Linear Temporal Logic is one language for *expressions* of properties.

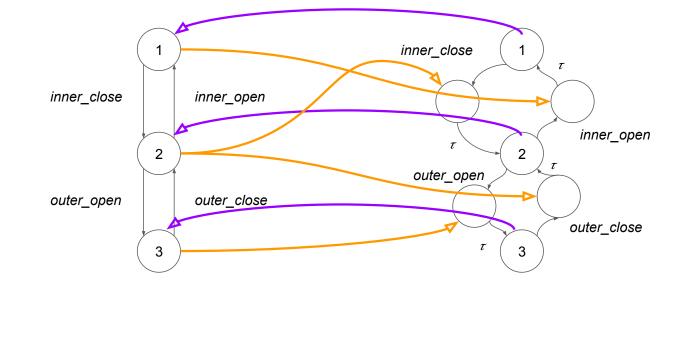
 \Box (inner_open \rightarrow \neg outer_open U inner_close)

Regular Expressions are another way to describe *traces of a system*. We will come back to that in a minute!

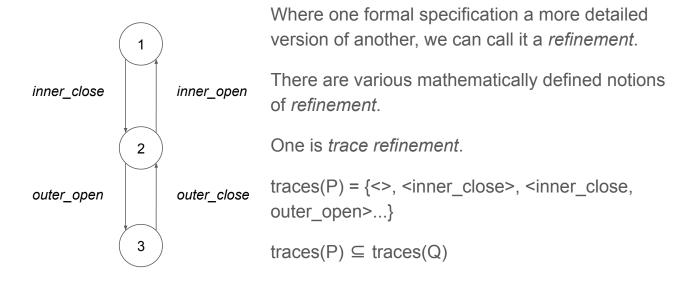
Formal Properties



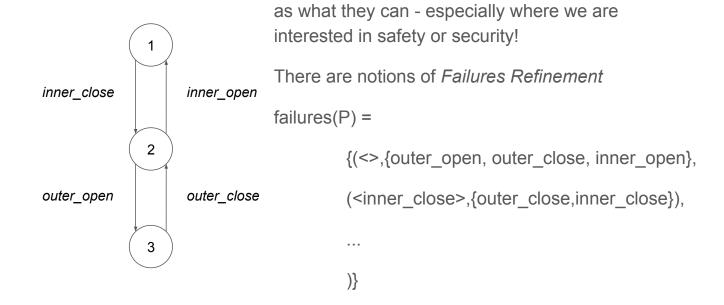
Formal Properties



Refinement



Refinement



Systems are defined as much by what they can't do

Refinement

There are also *State and Operation Refinement* concepts.

These generally involve *Reducing Non-determinism*

This is usually *predictable* and doesn't break the *specified properties*

... but that doesn't make it perfect!

Summary

- Design is an iterative process of more and more detailed Specifications
- We can make those specifications formal and then do various *comparisons* to check that the more detailed specifications *conform* the the higher level ones.
- Refinement (in various forms) is one method for handling this.
- There are others (LTL, ...)