08:00 **Carry look thead adder : (CLA)**

09:00 It improves the speed of arithmetic operations by addressing the slow processes
10:00 of carry propagation in conventional adders like RCA.

11:00

→ CLA reduces the delay by calculating
12:00 carry bits in advance, based on the input bits, without waiting from the
13:00 previous stages.

14:00 → it computes the carries directly from the inputs and uses them to compute the
15:00 sum faster.

16:00 CLA is based on generating two signals.

17:00 1. Generate (G_i)
2. propogate (P)

18:00

Generate - A bit pair will always generate
19:00 a carry, regardless of the Carry in.

Eve. → This happens when both i/p bit pair are "1"

$C_g = a \& b$

May 2023

05 Friday

(125 - 240) Wk 19

May

Su	Mo	Tu	We	Th	Fr	Sa
•	1	2	3	4	5	6
7	8	9	10	11	12	13
14	15	16	17	18	19	20
21	22	23	24	25	26	27
28	29	30	31	•	•	•

08:00 **propogate** - A bit pair will propagate a carry from the previous stage

09:00 if either of the bits is 1,

10:00 i.e if carry in is present, it will be paused on.

11:00

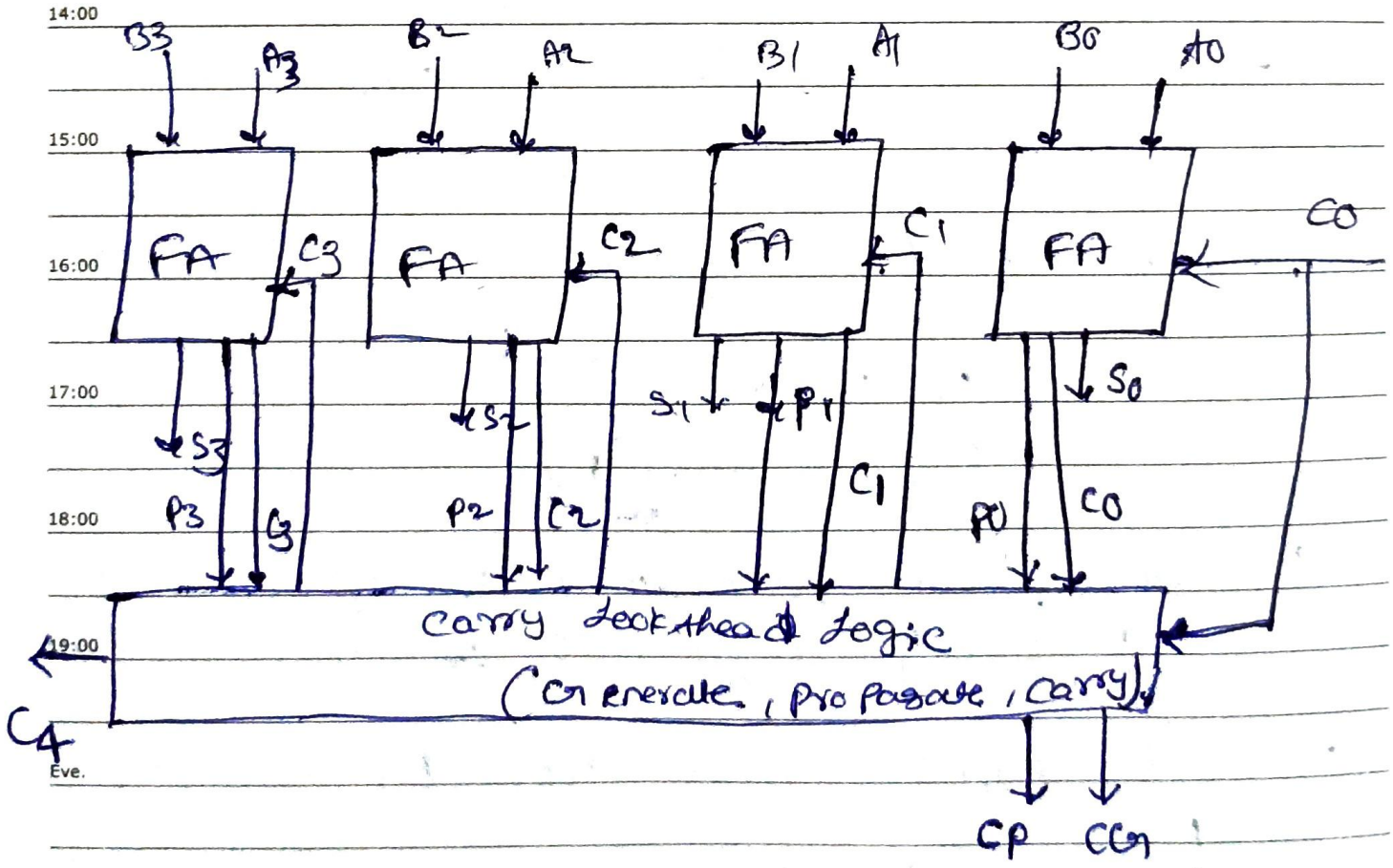
$$P = a + b$$

12:00

CLA — uses parallel computation for carries, reducing delay significantly.

13:00

14:00



May 2023

08 Monday

(128 - 237) Wk 20

08:00

Sum — $P_i \oplus G_i$ — Sum logic

09:00

C_{i+1} — $C_i P_i + G_i$

10:00

carry logic

$\therefore C_1 = C_0 P_0 + G_{10}$

11:00 $C_2 = C_1 P_1 + G_{11}$

$C_3 = C_2 P_2 + G_{12}$

12:00 $C_4 = C_3 P_3 + G_{13}$

13:00

14:00

15:00