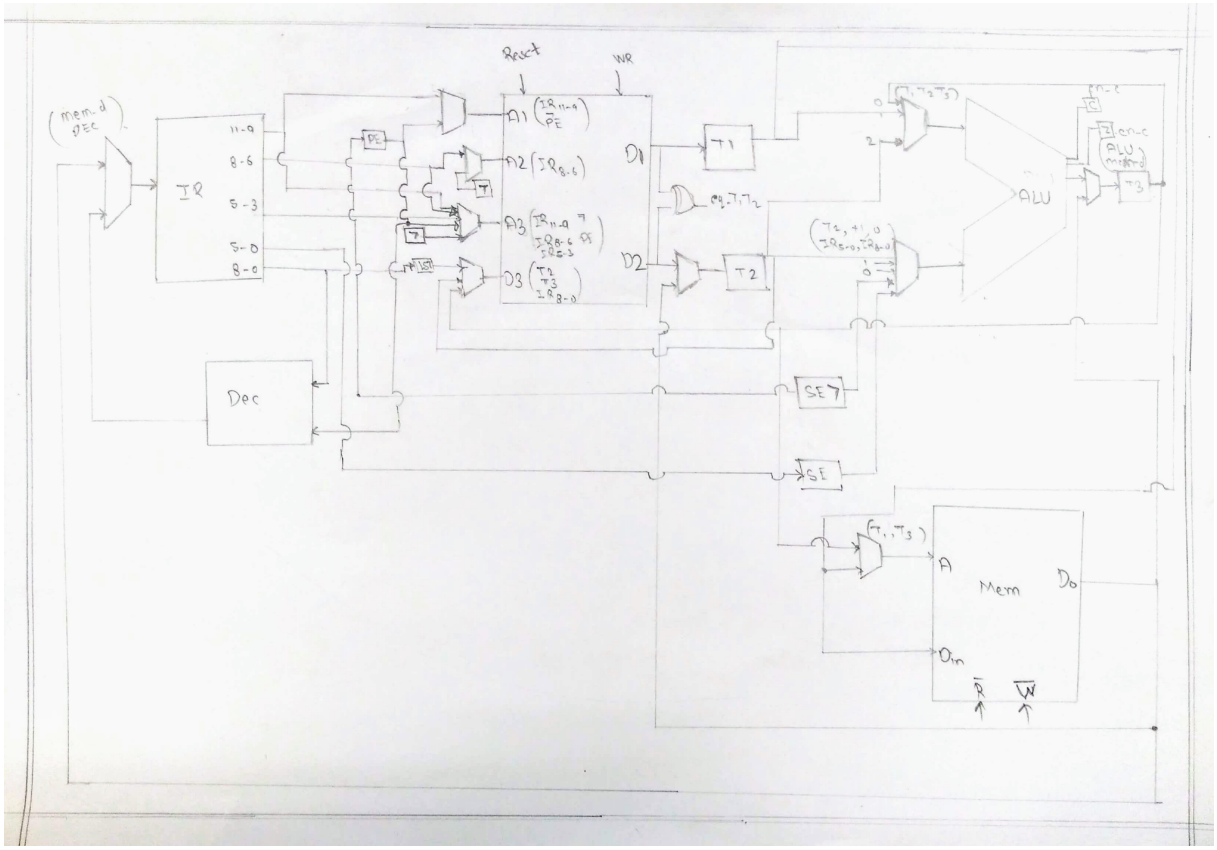
EE 309 : Microprocessor Project 1 : IITB RISC

Pranav Sankhe, Sachin Goyal, Srivatsan Shridhar, Tanya Chaudhary 8/11/2017

1 Datapath Design & Description

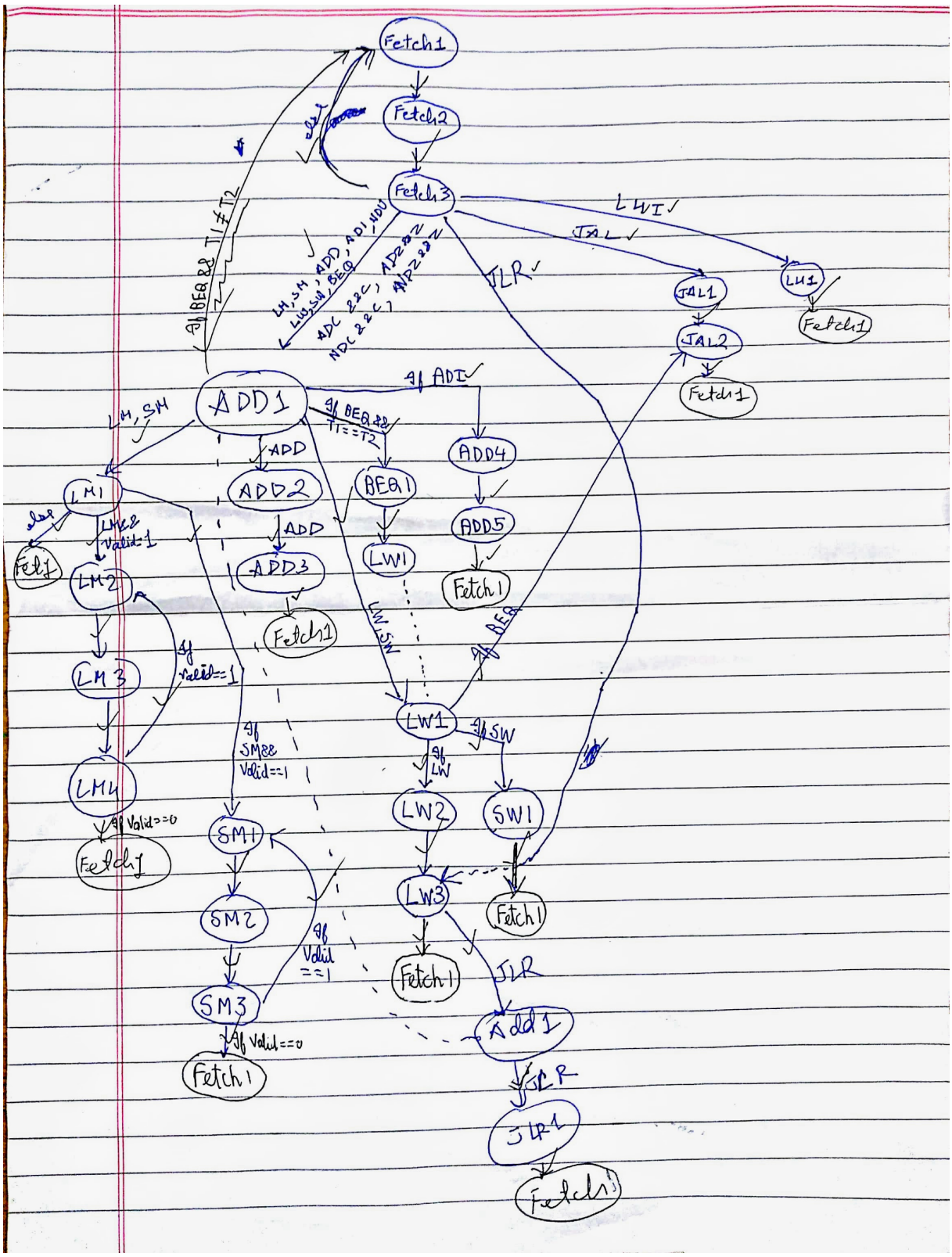
1.1 Datapath Design



1.2 Description

- **Memory**
  We have 16 bit addresses in memory, and each address stores 16 bit data in it. The memory block is controlled by R and W signals.
- **Register File**
  Register file has 4 inputs A1, A2, A3, D3 and 2 outputs D1 and D2. It is controlled by 2 signals Reset and WR.
- **ALU**
  Our ALU supports AND and NAND instructions. It sets the Z(zero) and C(carry) flag after instruction.

2 Flowchart Design



3 Test Cases