Compact Modeling of the Effects of Parasitic Internal Fringe Capacitance on the Threshold Voltage of High-k Gate-Dielectric Nanoscale SOI MOSFETs

M. Jagadesh Kumar, *Senior Member, IEEE*, Sumeet Kumar Gupta, *Student Member, IEEE*, and Vivek Venkataraman, *Student Member, IEEE*

***Abstract*—A compact model for the effect of the parasitic internal fringe capacitance on the threshold voltage of high-k gate-dielectric silicon-on-insulator MOSFETs is developed. The authors' model includes the effects of the gate-dielectric permittivity, spacer oxide permittivity, spacer width, gate length, and the width of an MOS structure. A simple expression for the parasitic internal fringe capacitance from the bottom edge of the gate electrode is obtained and the charges induced in the source and drain regions due to this capacitance are considered. The authors demonstrate an increase in the surface potential along the channel due to these charges, resulting in a decrease in the threshold voltage with an increase in the gate-dielectric permittivity. The accuracy of the results obtained using the authors' analytical model is verified using two-dimensional device simulations.**

***Index Terms*—High-k gate dielectric, insulated gate field effect transistors (FETs), internal fringe capacitance, silicon-on-insulator (SOI) MOSFET, threshold voltage, two-dimensional (2-D) modeling.**

I. Introduction

The gate oxide thickness in modern small geometry MOSFETs is approaching the tunneling limit for electrons, resulting in an increase in the gate leakage current. Scaling the effective gate-dielectric thickness will require alternative materials with higher permittivities ($\varepsilon_{\rm ox}$) and greater physical thicknesses [a factor of ($\varepsilon_{\rm ox}/\varepsilon_{\rm SiO_2}$)] to prevent direct gate tunneling. However, the use of a high-k gate material may result in dielectric thicknesses comparable to the device gate length, resulting in increased fringing fields from the gate to the source/drain regions compromising the short-channel performance [1], [2].

Kamchouchi and Zaky [3] developed a model for the parasitic capacitance associated with the bottom edge of the gate electrode in which it is assumed that 1) the dielectric is the same throughout and 2) its thickness ($t_{\rm ox}$) is much less than the gate length (L_g). However, in scaled-down MOSFETs, the gate dielectric and the spacer oxide have different permittivities. In this paper, we develop a simple expression for the internal fringe capacitance ($C_{\rm bottom}$) considering different gate and spacer dielectric constants ($\varepsilon_{\rm ox} \neq \varepsilon_{\rm sp}$) and a gate-dielectric thickness comparable to the gate length.

Young [4] developed a model for the surface potential along the channel for silicon-on-insulator (SOI) MOSFETs without considering the effect of the internal fringe capacitance ($C_{\rm bottom}$). In this paper, we have demonstrated the effect of $C_{\rm bottom}$ on the surface potential by considering the charges induced on the source and drain regions (due to fringing field lines from the bottom of the gate electrode) and the potential developed due to these charges in the channel region.

Kumar and Chaudhry [5] and Reddy and Kumar [6] have earlier developed a model for the threshold voltage ($V_{\rm th}$) for dual material gate SOI MOSFETs. Using a similar approach, we have developed a model for the threshold voltage for the single material gate (SMG) SOI MOSFETs by including the effect of the internal fringe capacitance on the threshold voltage, which can be easily solved using a few iterations. Thus, this model provides an efficient tool for the design and characterization of high-k gate-dielectric SOI MOSFETs including the effects of parasitic internal fringe capacitance. The effects of varying device parameters can easily be investigated using the simple models presented in this paper. The model results are verified by comparing them with the two-dimensional (2-D) simulated results from MEDICI [10].

II. Model for Internal Fringe Capacitance ($C_{\rm bottom}$)

A schematic cross-sectional view of an SOI MOSFET with a high-k gate dielectric is shown in Fig. 1, with the fringing field lines from the bottom of the gate electrode to the drain and source regions. For simplicity, we assume circular field lines as shown in Fig. 2, similar to the approach used in earlier studies for the other components of parasitic capacitance [7]–[9]. The infinitesimal capacitances in the high-k and spacer regions, respectively, can be written as

$$dC_1 = \frac{\varepsilon_{\rm ox} W\, dy}{\left(\frac{\pi}{2}\right) y} \quad \text{and} \quad dC_2 = \frac{\varepsilon_{\rm sp} W\, dy}{\left(\frac{\pi}{2}\right)(t_{\rm ox} - y)}$$

where $\varepsilon_{\rm ox}$ is the permittivity of the gate dielectric, $\varepsilon_{\rm sp}$ is the permittivity of spacer material, W is the width of the MOS structure and $t_{\rm ox}$ is the gate-dielectric thickness. Since dC_1

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The authors are with the Department of Electrical Engineering, Indian Institute of Technology, New Delhi 110 016, India (e-mail: mamidala@ieee.org).

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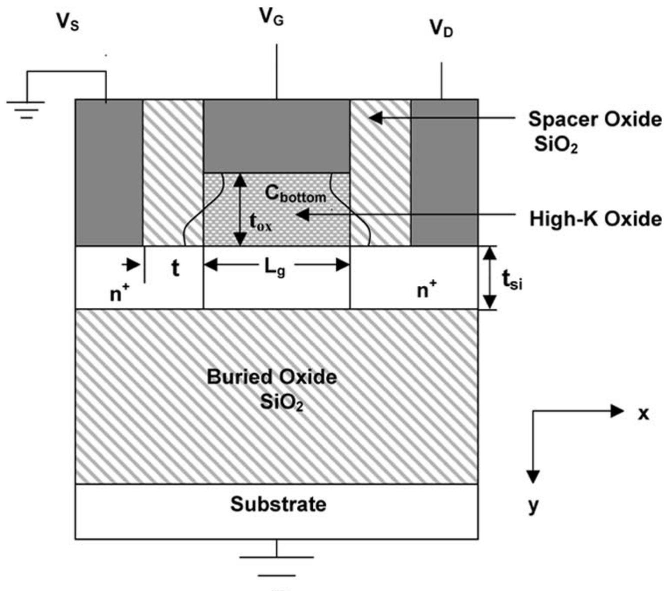

Fig. 1. Cross-sectional view of an SOI MOSFET showing the internal parasitic fringe capacitance.

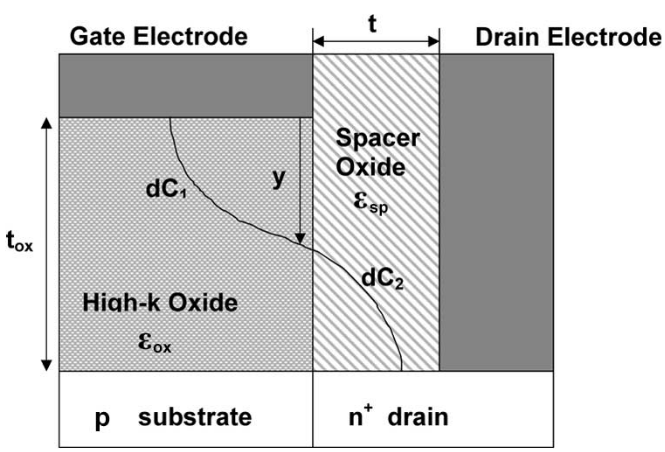

Fig. 2. Fringing field from the bottom of the gate electrode to the drain (or source).

and dC_2 are in series, the net infinitesimal capacitance can be written as

$$dC = \frac{dC_1 dC_2}{dC_1 + dC_2} = \frac{2\varepsilon_{\rm ox}\varepsilon_{\rm sp} W\,dy}{\pi(\varepsilon_{\rm ox}t_{\rm ox} + \varepsilon_{\rm sp}y - \varepsilon_{\rm ox}y)}. \quad (1)$$

The total internal fringe capacitance can be obtained by integrating (1) over the gate-dielectric thickness as

$$C_{\rm bottom} = \int_0^{t_{\rm ox}} \frac{2\varepsilon_{\rm ox}\varepsilon_{\rm sp} W\,dy}{\pi(\varepsilon_{\rm ox}t_{\rm ox} + \varepsilon_{\rm sp}y - \varepsilon_{\rm ox}y)} = \frac{2\varepsilon_{\rm ox}\varepsilon_{\rm sp}W}{\pi(\varepsilon_{\rm ox} - \varepsilon_{\rm sp})}\ln\left(\frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm sp}}\right). \quad (2)$$

Equation (2) is refined below in order to take care of the imperfect circularity of the fringing field lines.

The model by Kamchouchi and Zaky [3] gives the parasitic capacitance per unit length considering the electric field lines fringing from the entire perimeter of the bottom edge of the gate electrode as

$$C = \frac{(2 - \ln 4)\varepsilon_{\rm ox}}{2\pi} \quad \text{for} \quad \varepsilon_{\rm ox} = \varepsilon_{\rm sp} \quad \text{and} \quad \frac{t_{\rm ox}}{L_g} \ll 1 \quad (3)$$

where L_g is the gate length. The total fringe capacitance can be obtained by multiplying (3) with the perimeter of the bottom edge of the gate electrode [3]. Since we need to account for electric field lines fringing from the bottom edge of the gate to either the source or the drain region only, the internal fringe capacitance can be written as

$$C_{\rm bottom} = \frac{(2 - \ln 4)\varepsilon_{\rm ox}W}{2\pi} \cong \frac{(0.3)\varepsilon_{\rm ox}W}{\pi} \quad \text{for} \quad \varepsilon_{\rm ox} = \varepsilon_{\rm sp} \quad \text{and} \quad \frac{t_{\rm ox}}{L_g} \ll 1. \quad (4)$$

It can be seen that (2) reduces to (4) in the limit $\varepsilon_{\rm ox} \to \varepsilon_{\rm sp}$ but for a constant factor. This difference arises because of the assumption of the fringing electric field lines being circular while deriving (2). Thus, (2) is multiplied by the above factor $(0.3/2 = 0.15)$ to obtain

$$C_{\rm bottom} = \frac{(0.3)\varepsilon_{\rm ox}\varepsilon_{\rm sp}W}{\pi(\varepsilon_{\rm ox} - \varepsilon_{\rm sp})}\ln\left(\frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm sp}}\right). \quad (5)$$

The above expression reduces to (4) in the limit $\varepsilon_{\rm ox} \to \varepsilon_{\rm sp}$.

The Kamchouchi and Zaky model in (4), and hence (5), assumes that the separation between the electrodes is very small in comparison to the length of the electrodes. This is certainly not the case in short channel high-k dielectric SOI MOSFETs. Hence, (5) is further modified to represent the true picture.

The fringing field from the gate to the source/drain regions increases as a function of $(t_{\rm ox}/L_g)$ [1]. This is the effect of the increased crowding of field lines in the spacer region for large gate-dielectric thicknesses, i.e, for $t_{\rm ox}$ comparable to L_g. Hence, the fringe capacitance in the spacer region is more than what has been assumed while deriving (5). To account for this, an effective spacer dielectric constant is defined as

$$\varepsilon'_{\rm sp} = \left(1 + \frac{t_{\rm ox}}{L_g}\right)\varepsilon_{\rm sp}. \quad (6)$$

Substituting (6) in place of $\varepsilon_{\rm sp}$ in (5), we can obtain the final expression for the parasitic internal fringe capacitance as

$$C_{\rm bottom} = \frac{(0.3)\varepsilon_{\rm eff}W}{\pi} \quad (7)$$

where

$$\varepsilon_{\rm eff} = \frac{\varepsilon_{\rm ox}\varepsilon'_{\rm sp}}{\varepsilon_{\rm ox} - \varepsilon'_{\rm sp}}\ln\left(\frac{\varepsilon_{\rm ox}}{\varepsilon'_{\rm sp}}\right).$$

III. Effect of the Parasitic Internal Fringe Capacitance on the Surface Potential

To include the effect of the internal fringe capacitance on the surface potential, we assume the charge distribution induced in the source and drain regions due to the fringing electric field lines as in a uniformly charged plate as shown in Fig. 3, with the charge density σ given by

$$\sigma = \left(\frac{C_{\text{bottom}} V_p}{W \cdot t}\right)$$

$$\text{with} \quad \begin{array}{ll} V_p = V_{\text{bi}} - V_G + V_{\text{FB}} & \text{for the source region} \\ V_p = V_{\text{bi}} + V_D - V_G + V_{\text{FB}} & \text{for the drain region} \end{array}$$

where $V_{\text{bi}} = (E_g/2) + V_T \ln(N_A/n_i)$ is the built-in potential across the body–source junction, E_g is the silicon bandgap, N_A is the body/substrate doping concentration, V_T is the thermal voltage, n_i is the intrinsic carrier concentration, V_G and V_D are the potentials applied to the gate and drain electrodes, respectively, V_{FB} is the flat-band voltage, W is width of the gate, and t is the spacer thickness.

The potential due to this uniform charge distribution is evaluated along the channel at the middle of the gate width W as the effect is maximum here. In an MOSFET, the field lines originating from the bottom of the charged plate only will contribute to the potential in the channel; therefore, only half the coulomb potential due to these charges is considered. Then, the potential at a distance "x" from the uniformly charged plate is given by (Fig. 3)

$$V(x) = \frac{1}{2}\int_0^t \int_{-\frac{W}{2}}^{\frac{W}{2}} \frac{\sigma dx_1 dx_2}{4\pi\varepsilon_{\text{Si}}\sqrt{(x+x_1)^2 + (x_2)^2}} \tag{8}$$

where ε_{Si} is the dielectric constant of silicon. Evaluation of the integral in (8) gives the expression for $V(x)$ as given in (9) shown at the bottom of the page.

Young [4] proposed a model for the surface potential along the channel (x-direction in Fig. 1) for a fully depleted (FD) SOI MOSFET, assuming a simple parabolic potential profile in the vertical direction (y-direction in Fig. 1) as

$$\phi_s(x) = A\exp(\lambda x) + B\exp(-\lambda x) - \delta \tag{10}$$

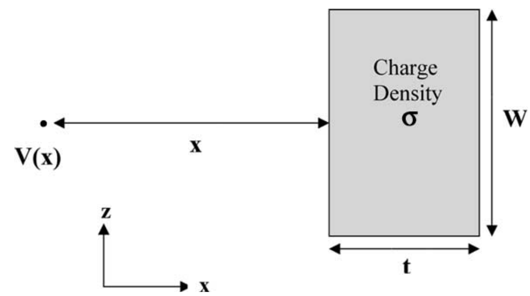

Fig. 3. Potential due to a uniformly charged plate.

where

$$\delta = \frac{qN_A t_{\text{Si}} t_{\text{ox}}}{\varepsilon_{\text{ox}}} - V_G + V_{\text{FB}}$$

and $\lambda = \sqrt{\varepsilon_{\text{ox}}/(t_{\text{ox}}\varepsilon_{\text{Si}} t_{\text{Si}})}$, V_{FB} is the flat-band voltage, t_{Si} is the silicon substrate thickness and ε_{Si} is the permittivity of silicon. The parameters A and B are given as

$$A = \left\{\frac{(V_{\text{bi}} + \delta + V_D) - (V_{\text{bi}} + \delta)\exp(-\lambda L_g)}{1 - \exp(-2\lambda L_g)}\right\}\exp(-\lambda L_g)$$

$$B = \left\{\frac{(V_{\text{bi}} + \delta) - (V_{\text{bi}} + \delta + V_D)\exp(-\lambda L_g)}{1 - \exp(-2\lambda L_g)}\right\}.$$

In the above analysis, we have assumed the buried oxide thickness to be large and hence neglected the corresponding capacitance.

The surface potential minimum is at

$$x = x_{\min} = \frac{1}{2\lambda}\ln\left(\frac{B}{A}\right)$$

and is given by

$$\phi_{s\,\min} = 2\sqrt{AB} - \delta. \tag{11}$$

To obtain the surface potential including the effect of the internal fringe capacitance, the potential due to the charges on the source and drain regions as given by (9), is added to (10) and the expression for surface potential is modified as

$$\phi'_s(x) = A\exp(\lambda x) + B\exp(-\lambda x) - \delta + \left(V(x)|_{\text{source}} + V(L_g - x)|_{\text{drain}}\right). \tag{12}$$

$$V(x) = \frac{\sigma}{8\pi\varepsilon_{\text{Si}}}\left[\left[(x+t)\cdot\ln\left\{\frac{\sqrt{(x+t)^2 + \left(\frac{W^2}{4}\right)} + \left(\frac{W}{2}\right)}{\sqrt{(x+t)^2 + \left(\frac{W^2}{4}\right)} - \left(\frac{W}{2}\right)}\right\} - x\cdot\ln\left\{\frac{\sqrt{x^2 + \left(\frac{W^2}{4}\right)} + \left(\frac{W}{2}\right)}{\sqrt{x^2 + \left(\frac{W^2}{4}\right)} - \left(\frac{W}{2}\right)}\right\}\right.\right.$$
$$\left.\left. + W\cdot\ln\left\{\frac{\sqrt{x^2 + \left(\frac{W^2}{4}\right)} + t + \sqrt{x^2 + t^2 + 2t\sqrt{x^2 + \left(\frac{W^2}{4}\right)}}}{\sqrt{x^2 + \left(\frac{W^2}{4}\right)} + x}\right\}\right]\right] \tag{9}$$

Here, $V(x)|_{\text{source}}$ is the potential along the channel due to the charges in the source region, and $V(L_g - x)|_{\text{drain}}$ is the potential along the channel due to the charges in the drain region.

The minimum of the modified surface potential is given by

$$\phi'_{s\,\min} = 2\sqrt{AB} - \delta + \left(V(x)|_{\text{source}} + V(L_g - x)|_{\text{drain}}\right)\big|_{x=x_{\min}}. \quad (13)$$

IV. Effect of the Parasitic Internal Fringe Capacitance on the Threshold Voltage

In [5], Kumar and Chaudhry proposed a model for the threshold voltage of dual-material gate (DMG)-SOI MOSFETs by equating the surface potential minimum given by (11) to twice the Fermi potential i.e.,

$$\phi_{s\,\min} = 2\phi_F \quad \text{where} \quad \phi_F = V_T \ln\left(\frac{N_A}{n_i}\right). \quad (14)$$

The model in [5] can be modified for SMG SOI MOSFETs as

$$V_{\text{th}} = \frac{\left(-V_{\phi 1} + \sqrt{V_{\phi 1}^2 - 4\xi V_{\phi 2}}\right)}{2\xi} \quad (15)$$

where

$$\begin{aligned}
\xi &= 2\cosh(\lambda L_g) - 2 - \sinh^2(\lambda L_g)\\
V_{\phi 1} &= V_{\text{bi1}}\left(1 - \exp(\lambda L_g)\right) + (4\phi_F - 2u)\sinh^2(\lambda L_g)\\
&\quad - V_{\text{bi2}}\left(1 - \exp(-\lambda L_g)\right)\\
V_{\phi 2} &= V_{\text{bi1}} V_{\text{bi2}} - (2\phi_F - u)^2 \sinh^2(\lambda L_g)\\
V_{\text{bi1}} &= (V_{\text{bi}} - u)\left(1 - \exp(-\lambda L_g)\right) + V_{DS}\\
V_{\text{bi2}} &= (V_{\text{bi}} - u)\left(\exp(\lambda L_g) - 1\right) - V_{DS}\\
u &= -\frac{q N_A t_{\text{Si}} t_{\text{ox}}}{\varepsilon_{\text{ox}}} - V_{\text{FB}}\\
\lambda &= \sqrt{\frac{\varepsilon_{\text{ox}}}{(t_{\text{ox}} \varepsilon_{\text{Si}} t_{\text{Si}})}}.
\end{aligned}$$

To incorporate the effect of the internal fringe capacitance, we modify (14) as

$$\phi'_{s\,\min} = 2\phi_F \quad (16)$$

where $\phi'_{s\,\min}$ is as given in (13). Solving (16) results in the same expression for the threshold voltage as given in (15), except for a modification in the expression for "u" given as

$$u = -\frac{q N_A t_{\text{Si}} t_{\text{ox}}}{\varepsilon_{\text{ox}}} - V_{\text{FB}} + \left(V(x)|_{\text{source}} + V(L_g - x)|_{\text{drain}}\right)\big|_{x=x_{\min}}. \quad (17)$$

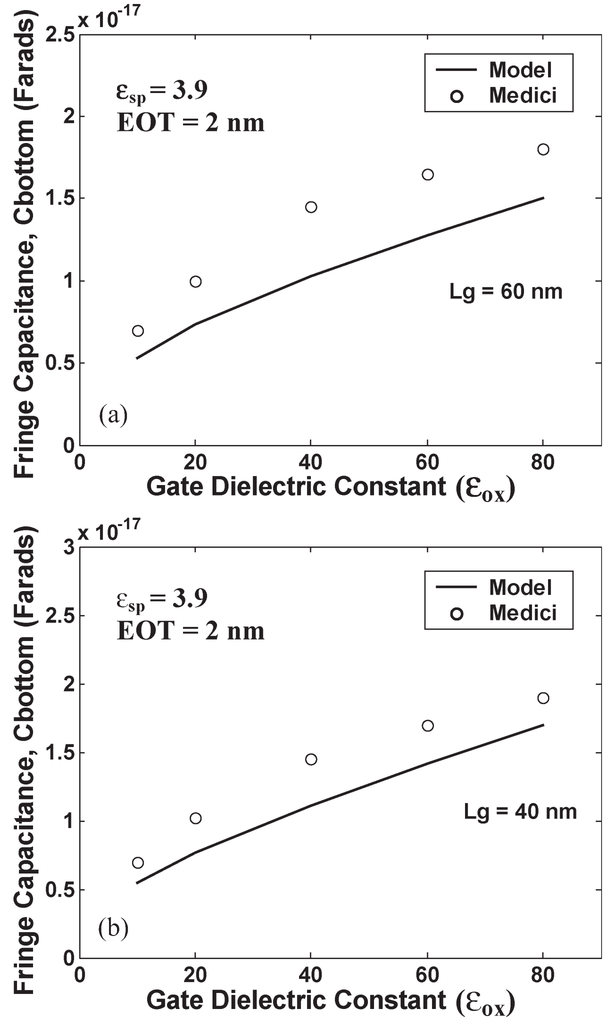

Fig. 4. Internal fringe capacitance variation with gate oxide permittivity for (a) $L_g = 60$; and (b) $L_g = 40$ nm. Gate width W is fixed at 1 μm, EOT $=$ 2.0 nm, $\varepsilon_{\text{sp}} = 3.9$.

Since $V(x)$ is dependent on V_G [see (9)] and V_{th} is the value of V_G at $\phi'_{s\,\min} = 2\phi_F$, the value of threshold voltage V_{th} can be easily obtained by iteratively solving (15).

V. Simulation Results and Discussion

Fig. 4 shows the variation of the internal fringe capacitance (C_{bottom}) versus the gate-dielectric permittivity evaluated using the proposed model and compared with MEDICI [10] simulations for channel lengths of 60 and 40 nm (see Table I for a description of the device parameters). The capacitance C_{bottom} is extracted from MEDICI in the following manner 1) the gate, source, and drain electrode heights are made negligible so that other components of the fringe capacitance that arise due to the finite electrode thickness are nullified and 2) the total capacitance as seen from the gate electrode for this MOSFET structure is extracted using the method of incremental charge due to the small increment in voltage $(\partial Q/\partial V)$. This gives the fringe capacitance plus the MOS gate capacitance (C_{ox}). Then, C_{ox} is subtracted from the capacitance obtained above to find the value of C_{bottom}. There is a difference of about 2×10^{-18} F between our calculated and simulated

TABLE I
DEVICE PARAMETERS USED IN THE SIMULATION

Parameter	Value
Source/Drain doping	2×10^{20} cm^{-3}
Channel doping	1×10^{16} cm^{-3}
Effective Oxide Thickness (EOT)*	2.0 nm
Work Function of gate material	4.5 V
Silicon film thickness	15 nm
Spacer oxide thickness	25 nm
BOX thickness	100 nm
Substrate Thickness	100 nm
Gate electrode thickness	25 nm
Source/drain – Gate overlap	5 nm

*(Physical oxide thickness = EOT×$\varepsilon_{ox}/\varepsilon_{SiO2}$)

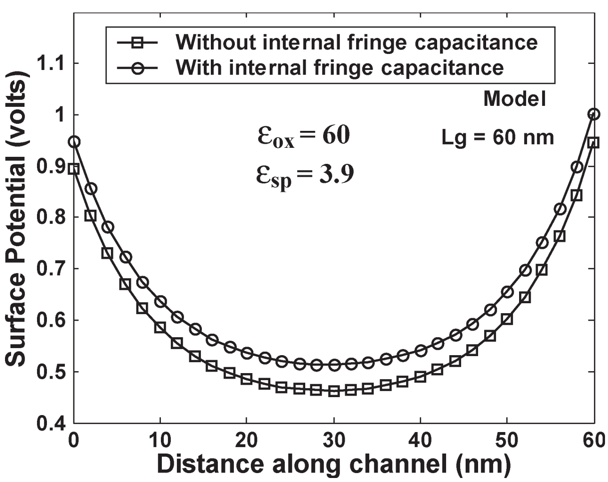

Fig. 5. Calculated surface potential variation along the channel for $\varepsilon_{\rm ox} = 60$ with and without the effect of the fringe capacitance. The parameters used are: $V_D = 0.05$ V, $V_G = 0.02$ V, EOT $= 2.0$ nm, $\varepsilon_{\rm sp} = 3.9$, $N_A = 1 \times 10^{16}$ cm^{-3}, W $= 1\mu$m.

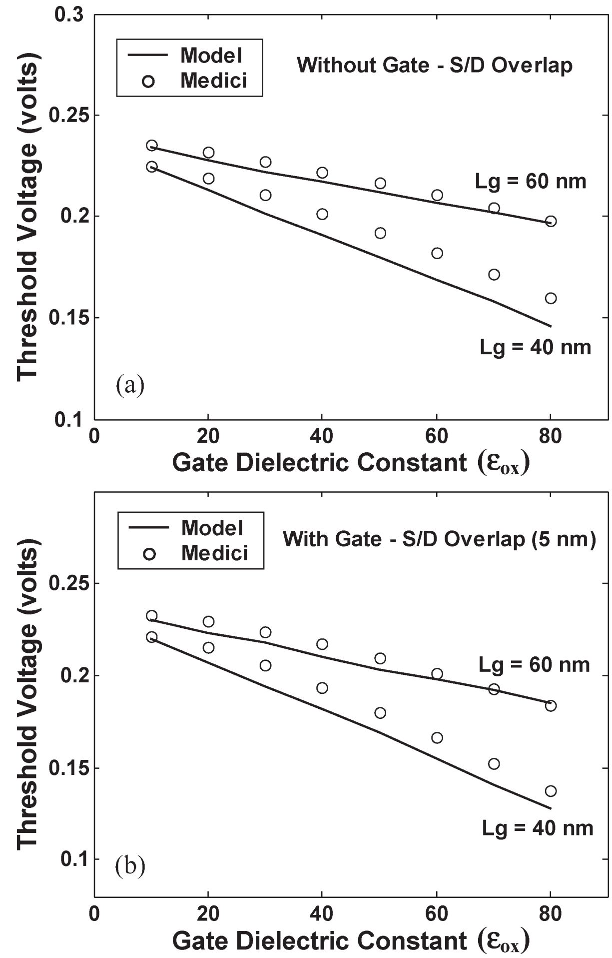

Fig. 6. Comparison of the simulated and calculated threshold voltage variation versus the gate-dielectric constant for (a) without the S/D-Gate overlap; and (b) with the S/D-Gate overlap. The parameters used are: $V_D = 0.05$ V, EOT $= 2.0$ nm, $\varepsilon_{\rm sp} = 3.9$, $N_A = 1 \times 10^{16}$ cm^{-3}, W $= 1\mu$m.

values. The values of the ideal MOS gate capacitance $C_{\rm ox} = (\varepsilon_{\rm ox}/t_{\rm ox})L_g W$ are 10^{-15} F for $L_g = 60$ nm and 7×10^{-16} F for $L_g = 40$ nm. It can be seen in the figure that the parasitic fringe capacitance increases with the increasing gate-dielectric permittivity. This is because the physical gate-dielectric thickness increases as the gate-dielectric permittivity increases [by a factor of $(\varepsilon_{\rm ox}/\varepsilon_{\rm SiO_2})$] for the same equivalent oxide thickness (EOT). This results in an increase in the fringing electric field lines from the bottom of the gate electrode to the source and drain regions.

In Fig. 5, the values of the surface potential with and without the effect of parasitic fringe capacitance are plotted against the horizontal distance x in the channel for a gate-dielectric permittivity of 60. In the figure, it is evident that the surface potential increases due to the effect of the fringe capacitance, resulting in an increase of the minimum surface potential. Furthermore, it can be seen that the effect of this potential is maximum roughly at the point of minimum surface potential; hence, one would expect a significant effect of $C_{\rm bottom}$ on the threshold voltage.

To verify the proposed model, the 2-D device simulator MEDICI [10] was used to simulate the threshold voltage. An FD n-channel SOI structure is implemented in MEDICI having uniformly doped source/drain and body regions. This structure is simulated both with and without the gate-source/drain (S/D) overlap.

In Fig. 6, the calculated values of the threshold voltage as a function of the gate-dielectric permittivity are compared with those obtained from the 2-D simulation. As can be seen from the figure, the threshold voltage obtained from the model tracks the simulation values well with a maximum offset of about 15 mV. The model gives a good agreement with the simulation even for the case of the gate-S/D overlap. It is evident that the threshold voltage decreases with the increasing $\varepsilon_{\rm ox}$. This is because of the increase in the surface potential as a result of the charges induced in the drain and source regions due to fringing field lines from the bottom of the gate electrode. This results in an early onset of inversion $(\phi_{s\,\rm min} = 2\phi_F)$ in the channel and hence a lower threshold voltage. The drop in the threshold voltage is as high as about 60–80 mV for $L_g = 40$ nm as $\varepsilon_{\rm ox}$ increases from 3.9 to 80.

To investigate the significance of quantum mechanical (QM) effects in the above analysis, the simulations were performed by including the QM effects in MEDICI [10]. In Fig. 7, the threshold voltage obtained with and without QM effects are compared. As is evident from the figure, there is a very small and insignificant difference between the two, suggesting that

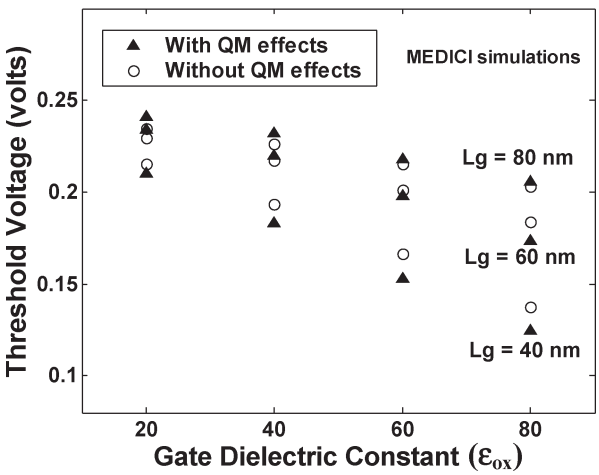

Fig. 7. Effect of including QM effects in the simulation. The parameters used are: $V_D = 0.05$ V, EOT $= 2.0$ nm, $\varepsilon_{\rm sp} = 3.9$, $N_A = 1 \times 10^{16}$ cm^{-3}, W $= 1 \mu$m.

the QM effects can be neglected in the threshold voltage calculations.

VI. Conclusion

We have examined the effects of the parasitic internal fringe capacitance on the threshold voltage of FD high-k SOI MOSFETs by developing a simple model for the internal fringe capacitance and obtaining expressions for the surface potential and threshold voltage including the effect of the internal fringe capacitance. We have compared the results with accurate 2-D simulations. The calculated values of the threshold voltage obtained from the proposed model agree well with the simulated results. There is a significant drop in the threshold voltage due to fringing field lines from the bottom edge of the gate electrode to the source and drain regions for higher gate-dielectric permittivities (i.e., higher physical gate-dielectric thickness for the same effective oxide thickness). This may affect the device characteristics and performance significantly; hence, it is important to recognize this effect especially for high-k gate-dielectric SOI MOSFETs. Our model can be easily implemented in a circuit simulator to include this effect.

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M. Jagadesh Kumar (M'95–SM'99) was born in Andhra Pradesh, India. He received the M.S. and Ph.D. degrees from the Indian Institute of Technology (IIT), Madras, India, all in electrical engineering.

From 1991 to 1994, he performed post-doctoral research in the modeling and processing of high-speed bipolar transistors with the Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, ON, Canada, where he also did research on amorphous silicon thin-film transistors. From July 1994 to December 1995, he was initially with the Department of Electronics and Electrical Communication Engineering, IIT. He then joined the Department of Electrical Engineering of the same university, where he became an Associate Professor in July 1997 and a Full Professor in January 2005. He is a reviewer for different journals including the *Institution of Electrical Engineers Proceedings on Circuits, Devices and Systems, Electronics Letters* and *Solid-State Electronics*. He is the author of more 100 publications in peer-reviewed journals and conferences. His research interests include VLSI device modeling and simulation for nanoscale applications, IC technology, and power semiconductor devices.

Dr. Kumar is a Fellow of the Institute of Electronics and Telecommunication Engineers, India. His teaching has often been rated as outstanding by the Faculty Appraisal Committee, IIT. He was the Chairman of the Fellowship Committee, The Sixteenth International Conference on Very-Large-Scale-Integration (VLSI) Design, January 4–8, 2003, New Delhi, India. He was the Chairman of the Technical Committee for High Frequency Devices, 12th International Workshop on the Physics of Semiconductor Devices, December 13–17, 2005, New Delhi, India. He is a reviewer for IEEE Transactions on Electron Devices.

Sumeet Kumar Gupta (S'05) is currently working toward the B.Tech. degree in electrical engineering at the Indian Institute of Technology, Delhi, India.

His current research interests include device modeling and simulation. He is also interested in low power very large scale design, and memory design and testing.

Vivek Venkataraman (S'05) is currently working toward the B.Tech. degree in electrical engineering at the Indian Institute of Technology, Delhi, India.

His research interests include semiconductor device physics, nanoscale device modeling and simulation, and organic semiconductors/electronics.