A New Pinched-Off Cold-FET Method to Determine Parasitic Capacitances of FET Equivalent Circuits

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***Abstract*—A new pinched-off cold FET method to extract the parasitic capacitances of FETs is proposed in this paper. The method is based on a physically meaningful depletion-layer model and the theoretical analysis of the two-port network for the pinched-off cold FETs. The parasitic gate capacitance ($C_{\rm pg}$) and the parasitic drain capacitance ($C_{\rm pd}$) of FETs are extracted using the linear regression technique associated with the frequency responses of Y-parameters. The extraction method can be applied to the small-signal equivalent-circuit modeling of the FETs including MESFETs, heterojunction FETs, and high-electron-mobility transistors. According to the new analytical method, the simulated S-parameters exhibit great agreement with the measured S-parameters for the equivalent-circuit models of FETs.**

***Index Terms*—Cold FET, HEMT, HFET, MESFET, parasitic capacitance.**

I. Introduction

THE fast and accurate method of parasitic parameter extraction is extremely important for FETs including MESFETs [1]–[3], heterojunction FETs (HFETs) [4]–[6], and high electron-mobility transistors (HEMTs) [7]–[10]. The efficient extraction method for determination of the FET parasitic parameters insures the correct equivalent-circuit model for evaluation of microwave performance of the FETs and design of monolithic microwave integrated circuits (MMICs) [11], [12]. Optimization methods have been usually used to determine the parasitic parameters of the FETs. The optimization results depend on the starting parameter values. The starting values without physical significance would generate errors. Instead of the extraction method using active bias conditions [13], the cold-FET (also known as zero drain bias) methods have been extensively studied to extract the parasitic parameters such as the resistances, inductances, and capacitances for FETs [14]–[30]. Curtice *et al.* used a cold-FET method to extract parasitic inductances of GaAs FETs [16]. Both parasitic resistances and inductances of the FETs can be extracted by the forward-gate-biased cold-FET methods [14], [17]–[22].

The parasitic gate capacitance ($C_{\rm pg}$) and the parasitic drain capacitances ($C_{\rm pd}$) of the FETs have been extracted by the pinched-off cold-FET methods [14], [15], [18]–[21], [23]–[27]. Under the pinched-off cold-FET condition, the gate of the FET was biased to turn the FET off and the drain-to-source bias was set to zero. A multiple pinched-off cold-FET bias measurement method has been reported to extract the parasitic capacitances [23]. The method was based on the assumption that the depletion-layer length is linearly dependent on the gate bias. However, the assumption of the linear dependence of the depletion-layer length on the gate bias cannot be physically realized for the common uniformly doped semiconductor because the depletion-layer extension of the uniformly doped semiconductor with the Schottky gate voltage is not linearly related [31].

Conventionally, the parasitic capacitances of the FETs were extracted by a single pinched-off cold-FET bias measurement according to the low-frequency Y-parameters of the devices [14], [15]. The conventional pinched-off cold-FET methods used identical capacitors to model the depletion layer under the gate. In Dambrine's method [14], two identical capacitors were used to describe the depletion-layer extension under the gate. The method has been applied to several cold-FET equivalent-circuit techniques [18]–[20], [24], [27]. The $C_{\rm pd}$ extracted by this method, however, are overestimated [15]. The incorrect $C_{\rm pd}$ will cause errors in the following extraction of the intrinsic parameters for active FETs [22]. White *et al.* proposed an improved pinched-off cold-FET method to extract the parasitic capacitances of the FETs [15]. They used three identical capacitors to represent the depletion-layer extension under the pinched-off cold-FET bias condition [15], [21]. The method was also employed in an optimization approach for determination of starting values [25]. However, the method cannot exactly describe the physical depletion-layer distribution because the physical geometry of the gate is not identical to those of the source and drain in a real FET. Unreasonable configuration for the intrinsic capacitors would lead to nonphysical results of parameter extraction for FET equivalent circuits [28]. Different capacitors are needed to represent the intrinsic depletion layer of a pinched-off cold FET.

In this paper, a new pinched-off cold-FET method for the extraction of the $C_{\rm pg}$ and $C_{\rm pd}$ is presented to solve the problems with the conventional methods. A physically meaningful depletion-layer model with different intrinsic capacitors is adopted for the pinched-off cold FETs. The two-port network for the pinched-off cold FETs is theoretically analyzed. We use a linear regression technique to extract the $C_{\rm pg}$ and $C_{\rm pd}$ in accordance with the measured imaginary Y-parameter frequency responses of the pinched-off cold FETs. The difference between our method and conventional methods is compared and discussed. The developed method has been successfully

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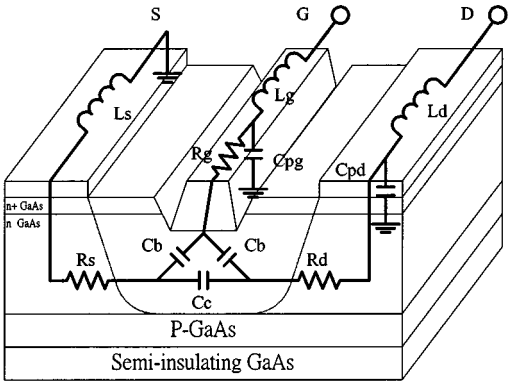

Fig. 1. Cross-sectional view and equivalent circuit for the pinched-off cold FET in this study.

applied to the small-signal equivalent-circuit modeling of the FETs for the further analysis of the microwave performance of the FETs.

II. Equivalent-Circuit Evaluation

In the equivalent-circuit model of the pinched-off cold FET proposed by Dambrine *et al.* [14], two identical capacitors were used to describe the depletion-layer distribution. The problem with the model is that two identical capacitors cannot fully describe the depletion-layer capacitance under the gate [15].

In the equivalent circuit of the White's method, three capacitors were used to represent the depletion-layer distribution [15]. The method was developed on the basis of the assumption that the depletion-layer capacitor associated with the gate is identical to those associated with the source and drain. The assumption, however, is not realistic because the physical geometry of the gate is not identical to those of the source and drain and the voltage bias of the gate is not the same as those of the source and drain under the pinched-off cold-FET bias conditions.

Fig. 1 shows the cross-sectional view and the equivalent circuit for the pinched-off cold FET in this study [23]. The $C_{\rm pg}$ is associated with the gate pad and the $C_{\rm pd}$ is associated with the drain pad. Two different intrinsic capacitors are used. The equivalent circuit consists of two parts, i.e., intrinsic and extrinsic elements. The intrinsic elements are capacitances C_b and C_c for description of the depletion-layer extension. The two identical capacitors labeled by C_b are used to express the symmetrical nature of the gate-to-source and gate-to-drain geometry and biases. The intrinsic capacitor C_c is used to describe the drain-to-source depletion-layer capacitance. The extrinsic elements include the gate resistance (R_g), the drain resistance (R_d), the source resistance (R_s), the gate inductance (L_g), the drain inductance (L_d), and the source inductance (L_s). The equivalent circuit effectively realizes the physical structure of pinched-off cold FETs.

III. Theoretical Analysis

According to the equivalent circuit with the physical cross section illustration in Fig. 1, we analyze the matrix representation of the pinched-off cold FET. The procedure flow of the theoretical analysis is shown in Fig. 2.

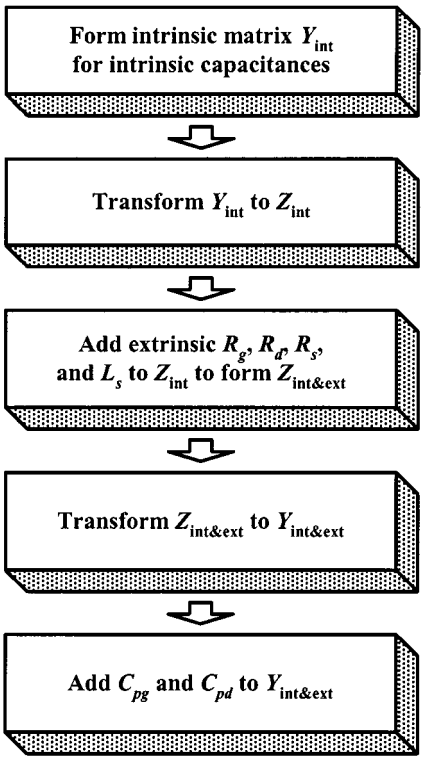

Fig. 2. Procedure flow of theoretical analysis.

A. Intrinsic Parameters

With the analysis procedure in Fig. 2, the intrinsic capacitances of the FET biased at the pinched-off cold-FET condition are expressed by the following Y-parameters (the matrix $Y_{\rm int}$):

$$Y_{\rm int11} = j\omega(2C_b) \tag{1}$$

$$Y_{\rm int12} = Y_{\rm int21} = -j\omega C_b \tag{2}$$

$$Y_{\rm int22} = j\omega(C_b + C_c). \tag{3}$$

The intrinsic Y-parameters are transformed to the intrinsic Z-parameters to form a matrix $Z_{\rm int}$ according to $Z_{\rm int} = Y_{\rm int}^{-1}$. We get

$$Z_{\rm int11} = \frac{-j(C_b + C_c)}{\omega(C_b^2 + 2C_bC_c)} \tag{4}$$

$$Z_{\rm int12} = Z_{\rm int21} = \frac{-jC_b}{\omega(C_b^2 + 2C_bC_c)} \tag{5}$$

$$Z_{\rm int22} = \frac{-j2C_b}{\omega(C_b + 2C_bC_c)}. \tag{6}$$

B. Intrinsic Parameters in Conjunction with Extrinsic R_g, R_d, R_s, and L_s

The intrinsic Z-parameters are combined with the extrinsic resistances R_g, R_d, and R_s, and the extrinsic source inductance L_s to form a matrix $Z_{\rm int\&ext}$. We have

$$Z_{\rm int\&ext11} = \frac{-j(C_b + C_c)}{\omega(C_b^2 + 2C_bC_c)} + R_g + R_s + jwL_s \tag{7}$$

$$Z_{\text{int\&ext12}} = Z_{\text{int\&ext21}} = \frac{-jC_b}{\omega(C_b^2 + 2C_bC_c)} + R_s + jwL_s \tag{8}$$

$$Z_{\text{int\&ext22}} = \frac{-j2C_b}{\omega(C_b^2 + 2C_bC_c)} + R_d + R_s + jwL_s. \tag{9}$$

The Z-parameters (7)–(9) are transformed to Y-parameters according to $Y_{\text{int\&ext}} = Z_{\text{int\&ext}}^{-1}$ as follows:

$$Y_{\text{int\&ext11}} = \frac{j\omega^5 A_{11} + j\omega^3 B_{11} + j\omega C_{11} + \omega^4 D_{11} + \omega^2 E_{11}}{\omega^4 F_{11} + \omega^2 G_{11} + 1} \tag{10}$$

$$Y_{\text{int\&ext12}} = Y_{\text{int\&ext21}} = \frac{j\omega^5 A_{12} + j\omega^3 B_{12} + j\omega C_{12} + \omega^4 D_{12} + \omega^2 E_{12}}{\omega^4 F_{12} + \omega^2 G_{12} + 1} \tag{11}$$

$$Y_{\text{int\&ext22}} = \frac{j\omega^5 A_{22} + j\omega^3 B_{22} + j\omega C_{22} + \omega^4 D_{22} + \omega^2 E_{22}}{\omega^4 F_{22} + \omega^2 G_{22} + 1} \tag{12}$$

where $A_{ij}, B_{ij}, C_{ij}, D_{ij}, E_{ij}, F_{ij}$, and G_{ij} $(i, j = 1, 2)$ are the constants related with device parameters. We have $A_{11} = A_{22}$, $C_{11} = 2C_b$, $C_{12} = -C_b$, $C_{22} = C_b + C_c$, $F_{11} = F_{12} = F_{22}$, and $G_{11} = G_{12} = G_{22}$. Note that the extrinsic L_g and L_d are not taken into account in (10)–(12).

C. Consideration of C_{pg} and C_{pd}

With consideration of the parasitic capacitances, C_{pg} and C_{pd} are added to the matrix $Y_{\text{int\&ext}}$ and the analytical Y-parameter equations (the matrix Y) for the pinched-off cold FET are derived as follows:

$$Y_{11} = j\omega C_{\text{pg}} + \frac{j\omega^5 A_{11} + j\omega^3 B_{11} + j\omega C_{11} + \omega^4 D_{11} + \omega^2 E_{11}}{\omega^4 F_{11} + \omega^2 G_{11} + 1} \tag{13}$$

$$Y_{12} = Y_{21} = \frac{j\omega^5 A_{12} + j\omega^3 B_{12} + j\omega C_{12} + \omega^4 D_{12} + \omega^2 E_{12}}{\omega^4 F_{12} + \omega^2 G_{12} + 1} \tag{14}$$

$$Y_{22} = j\omega C_{\text{pd}} + \frac{j\omega^5 A_{22} + j\omega^3 B_{22} + j\omega C_{22} + \omega^4 D_{22} + \omega^2 E_{22}}{\omega^4 F_{22} + \omega^2 G_{22} + 1}. \tag{15}$$

The resulting Y-parameter equations (13)–(15) represent the small-signal equivalent circuit of the pinched-off cold FET without L_g and L_d, as shown in Fig. 3. The frequency responses of the imaginary parts of the measured Y-parameters $\text{Im}(Y_{ij})$ $(i, j = 1, 2)$ are derived as follows:

$$\text{Im}(Y_{11}) = \omega C_{\text{pg}} + \frac{\omega^5 A_{11} + \omega^3 B_{11} + \omega C_{11}}{\omega^4 F_{11} + \omega^2 G_{11} + 1} \tag{16}$$

$$\text{Im}(Y_{12}) = \text{Im}(Y_{21}) = \frac{\omega^5 A_{12} + \omega^3 B_{12} + \omega C_{12}}{\omega^4 F_{12} + \omega^2 G_{12} + 1} \tag{17}$$

$$\text{Im}(Y_{22}) = \omega C_{\text{pd}} + \frac{\omega^5 A_{22} + \omega^3 B_{22} + \omega C_{22}}{\omega^4 F_{22} + \omega^2 G_{22} + 1}. \tag{18}$$

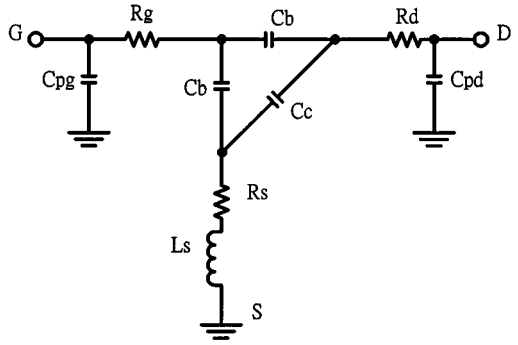

Fig. 3. Small-signal equivalent circuit of the pinched-off cold FET without L_g and L_d.

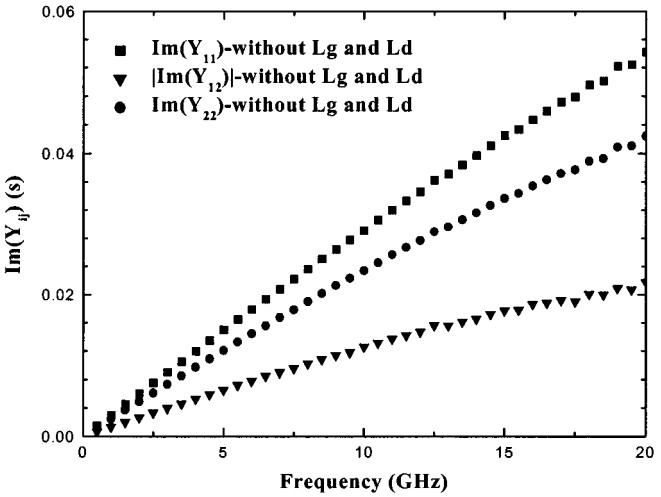

Fig. 4. Frequency responses of the imaginary parts of the measured Y-parameters without L_g and L_d.

IV. Measurement and Discussion

A. Determination of C_{pg} and C_{pd}

For verification of the theoretical expressions derived in Section III, the S-parameter characteristics of MESFETs were measured. As shown in the physical cross-sectional view of Fig. 1, the MESFETs tested have a directedly ion-implanted structure with an n^+-GaAs ohmic layer, an n-GaAs channel layer, and a p-GaAs buried layer for wireless applications [2]. The FETs with a gate length of 0.7 μm and a gatewidth of 1.5 mm were biased at a drain-to-source voltage of 0 V and a gate voltage of -5.5 V for the pinched-off cold-FET measurement. The S-parameter measurement was performed from 0.5 to 20 GHz.

The pinched-off cold-FET S-parameters were first transformed to Z-parameters. After subtracting the extrinsic L_g and L_d from the Z-parameters, the Z-parameters were then transformed to Y-parameters. The extrinsic L_g and L_d above were extracted by the forward gate-biased cold-FET measurement [14]. We obtained $L_g = 86.698$ pH, $L_d = 95.195$ pH, and $L_s = 1.879$ pH. The measured Y-parameter data exclusive of L_g and L_d are shown in Fig. 4. The frequency responses of the imaginary parts of the measured Y-parameters without L_g and L_d are nearly linear. The slight deviation from the linear relation in the imaginary part of the measured Y-parameters at high frequency can be explained by the nonlinear terms in

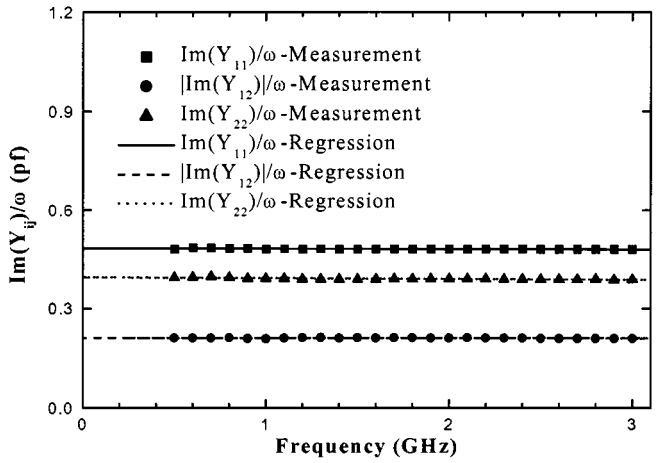

Fig. 5. Frequency responses of measured $\mathrm{Im}(Y_{ij})/\omega$ $(i, j = 1, 2)$ associated with the linear regression lines at the frequencies below 3 GHz. Measured $\mathrm{Im}(Y_{ij})/\omega$ data are indicated by solid symbols and linear regression data are indicated by lines.

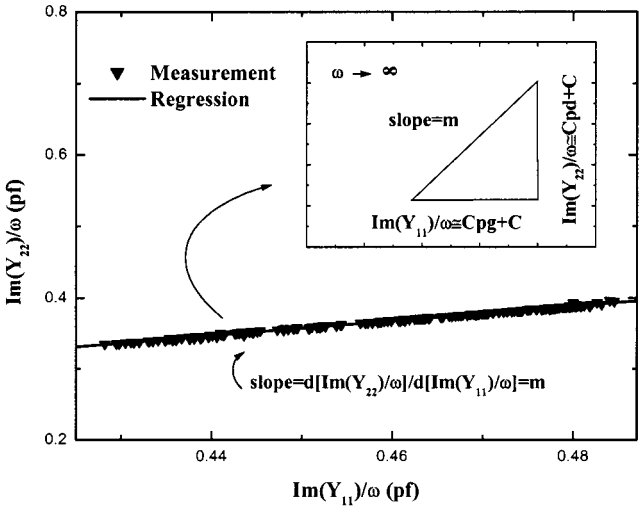

Fig. 6. Measurement characteristics of $\mathrm{Im}(Y_{22})/\omega$ versus $\mathrm{Im}(Y_{11})/\omega$ and associated linear regression line.

(16)–(18). The measured imaginary Y-parameter frequency responses agree with the derived expressions (16)–(18). The linear dependence of the measured Y-parameters on frequencies can be improved from the standpoint of the $\mathrm{Im}(Y_{ij})/\omega$ $(i, j = 1, 2)$.

The frequency responses of $\mathrm{Im}(Y_{ij})/\omega$ $(i, j = 1, 2)$ are

$$\frac{\mathrm{Im}(Y_{11})}{\omega} = C_{\mathrm{pg}} + \frac{\omega^4 A_{11} + \omega^2 B_{11} + C_{11}}{\omega^4 F_{11} + \omega^2 G_{11} + 1} \tag{19}$$

$$\frac{\mathrm{Im}(Y_{12})}{\omega} = \frac{\mathrm{Im}(Y_{21})}{\omega} = \frac{\omega^4 A_{12} + \omega^2 B_{12} + C_{12}}{\omega^4 F_{12} + \omega^2 G_{12} + 1} \tag{20}$$

$$\frac{\mathrm{Im}(Y_{22})}{\omega} = C_{\mathrm{pd}} + \frac{\omega^4 A_{22} + \omega^2 B_{22} + C_{22}}{\omega^4 F_{22} + \omega^2 G_{22} + 1}. \tag{21}$$

As the frequency approaches zero, (19)–(21) become

$$\frac{\mathrm{Im}(Y_{11})}{\omega} = C_{\mathrm{pg}} + C_{11} = C_{\mathrm{pg}} + 2C_b \tag{22}$$

$$\frac{\mathrm{Im}(Y_{12})}{\omega} = \frac{\mathrm{Im}(Y_{21})}{\omega} = C_{12} = -C_b \tag{23}$$

$$\frac{\mathrm{Im}(Y_{22})}{\omega} = C_{\mathrm{pd}} + C_{22} = C_{\mathrm{pd}} + C_b + C_c. \tag{24}$$

At low frequencies, effect of the nonlinear terms in (19)–(21) can be ignored. Fig. 5 shows the frequency responses of $\mathrm{Im}(Y_{ij})/\omega$ $(i, j = 1, 2)$ below 3 GHz. The frequency responses of $\mathrm{Im}(Y_{ij})/\omega$ $(i, j = 1, 2)$ are linear and constant at low frequencies. Using the linear regression technique, the intercept-point values of the regression lines associated with the measurement data at a zero frequency yield the constant terms in (22)–(24).

As the frequency approaches infinity, (19)–(21) become

$$\frac{\mathrm{Im}(Y_{11})}{\omega} = C_{\mathrm{pg}} + \frac{A_{11}}{F_{11}} = C_{\mathrm{pg}} + C \tag{25}$$

$$\frac{\mathrm{Im}(Y_{12})}{\omega} = \frac{\mathrm{Im}(Y_{21})}{\omega} = \frac{A_{12}}{F_{12}} \tag{26}$$

$$\frac{\mathrm{Im}(Y_{22})}{\omega} = C_{\mathrm{pd}} + \frac{A_{22}}{F_{22}} = C_{\mathrm{pd}} + C. \tag{27}$$

where

$$C = \frac{A_{11}}{F_{11}} = \frac{A_{22}}{F_{22}}. \tag{28}$$

An expression of $\mathrm{Im}(Y_{22})/\omega$ versus $\mathrm{Im}(Y_{11})/\omega$ can be derived from (25) and (27). We have

$$\frac{\mathrm{Im}(Y_{22})/\omega}{\mathrm{Im}(Y_{11})/\omega} = \frac{C_{\mathrm{pd}} + C}{C_{\mathrm{pg}} + C} = m \tag{29}$$

where m represents the slope of $\mathrm{Im}(Y_{22})/\omega$ versus $\mathrm{Im}(Y_{11})/\omega$.

Fig. 6 shows the measurement characteristics of $\mathrm{Im}(Y_{22})/\omega$ versus $\mathrm{Im}(Y_{11})/\omega$ from 0.5 to 20 GHz. $\mathrm{Im}(Y_{22})/\omega$ is linearly dependent on $\mathrm{Im}(Y_{11})/\omega$. Using the linear regression technique, the slope of the regression line associated with the measurement characteristics of $\mathrm{Im}(Y_{22})/\omega$ versus $\mathrm{Im}(Y_{11})/\omega$, indicated by m, can be calculated by

$$m = \frac{d\big[\mathrm{Im}(Y_{22})/\omega\big]}{d\big[\mathrm{Im}(Y_{11})/\omega\big]}. \tag{30}$$

The four analytical equations (22)–(24) and (29) associated with the four linear regression lines can solve C_{pg}, C_{pd}, C_b, and C_c simultaneously. We obtained $C_{\mathrm{pg}} = 0.059$ pF, $C_{\mathrm{pd}} = 0.065$ pF, $C_b = 0.211$ pF, and $C_c = 0.118$ pF.

B. Comparing with Conventional Methods

The parasitic capacitances of different samples were extracted in comparison with conventional methods [14], [15]. Table I shows the summary of the intrinsic and parasitic capacitances of the pinched-off cold FETs using different methods. For Dambrine's method [14], the C_{pd} values are much larger than the C_{pg} values and apparently overestimated [15]. On the other hand, the C_{pd} values extracted by White's method are underestimated so that some extracted C_{pd} values are negative. Compared with the two methods above, C_{pd} is close to C_{pg} in our method. The different results of these methods can be explained by the configurations of the equivalent circuits and the Y-parameter expressions for the pinched-off cold FETs.

TABLE I
SUMMARY OF INTRINSIC AND PARASITIC CAPACITANCES OF THE PINCHED-OFF COLD FETS EXTRACTED USING DIFFERENT METHODS

	Dambrine's Method [14]			White's Method [15]			This Method			
	Cb (pF)	Cpg (pF)	Cpd (pF)	Cb (pF)	Cpg (pF)	Cpd (pF)	Cb (pF)	Cc (pF)	Cpg (pF)	Cpd (pF)
Sample A	0.216	0.056	0.179	0.649	0.056	-0.038	0.211	0.118	0.059	0.065
Sample B	0.154	0.143	0.246	0.461	0.143	0.092	0.136	0.089	0.152	0.158
Sample C	0.153	0.135	0.249	0.458	0.135	0.096	0.135	0.104	0.148	0.148
Sample D	0.308	0.050	0.299	0.923	0.050	-0.009	0.306	0.158	0.044	0.011

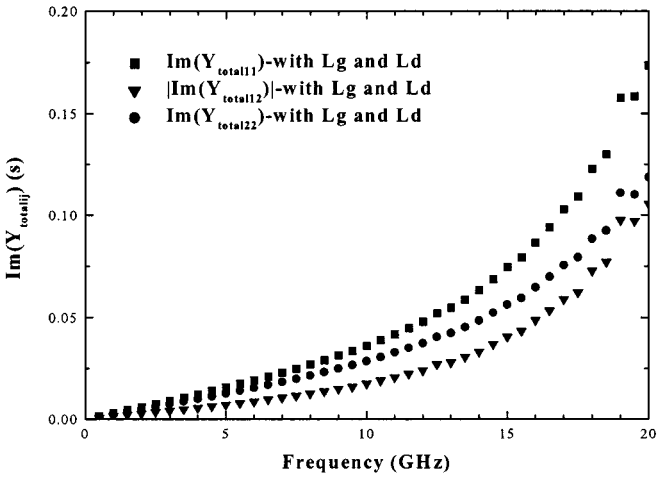

Fig. 7. Measured Y-parameters of the total two-port network including L_g and L_d for the pinched-off cold FET.

In conventional methods [14], [15], the parasitic capacitances were extracted according to the Y-parameters of the total two-port network (the matrix $Y_{\rm total}$) for the pinched-off cold FETs. Extrinsic L_g and L_d are included in $Y_{\rm total}$. Fig. 7 shows the measured $Y_{\rm total}$ data directly transformed from the measured S-parameters. The frequency responses of the imaginary parts of measured $Y_{\rm total}$ are nonlinear because of the effect of the extrinsic inductances. The difference between Figs. 7 and 4 tells us how strong the extrinsic inductance effect is. With regard to the matrix Y for (13)–(15), the matrix $Y_{\rm total}$ is derived as follows:

$$Y_{\rm total} = \left(Y^{-1} + Z_{\rm LgLd}\right)^{-1} \tag{31}$$

where the matrix $Z_{\rm LgLd}$ represents the Z-parameters of the extrinsic L_g and L_d, i.e.,

$$Z_{\rm LgLd} = \begin{bmatrix} j\omega L_g & 0 \\ 0 & j\omega L_d \end{bmatrix}. \tag{32}$$

Expression (31) is nonlinearly dependent on frequencies, as can be seen in Fig. 7. Low-frequency $Y_{\rm total}$ expressions were used in the conventional methods by ignoring the extrinsic inductances [14], [15].

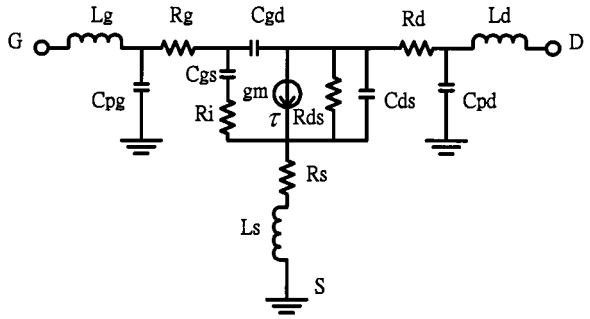

Fig. 8. Small-signal equivalent-circuit model of the FET in the active region.

In Dambrine's method [14], two identical capacitors were used to describe the depletion-layer extension under the gate. The imaginary parts of the $Y_{\rm total}$ expressions ignoring the extrinsic inductances and resistances are [14]

$$\mathrm{Im}(Y_{\rm total11}) = \omega(C_{\rm pg} + 2C_b) \tag{33}$$
$$\mathrm{Im}(Y_{\rm total12}) = \mathrm{Im}(Y_{\rm total21}) = -\omega C_b \tag{34}$$
$$\mathrm{Im}(Y_{\rm total22}) = \omega(C_{\rm pd} + C_b). \tag{35}$$

Due to the lack of an intrinsic capacitor to describe the depletion-layer extension between the drain and source, the capacitance effect of the drain-to-source depletion layer is reflected in the extracted $C_{\rm pd}$ values in Dambrine's method. Therefore, the $C_{\rm pd}$ values are overestimated, as shown in Table I.

In White's method [15], three identical capacitors were used to depict the depletion-layer extension. The imaginary parts of the $Y_{\rm total}$ expressions ignoring the extrinsic inductances and resistances are [15]

$$\mathrm{Im}(Y_{\rm total11}) = \omega\left(C_{\rm pg} + \frac{2}{3}C_b\right) \tag{36}$$
$$\mathrm{Im}(Y_{\rm total12}) = \mathrm{Im}(Y_{\rm total21}) = -\omega\frac{C_b}{3} \tag{37}$$
$$\mathrm{Im}(Y_{\rm total22}) = \omega\left(C_{\rm pd} + \frac{2}{3}C_b\right). \tag{38}$$

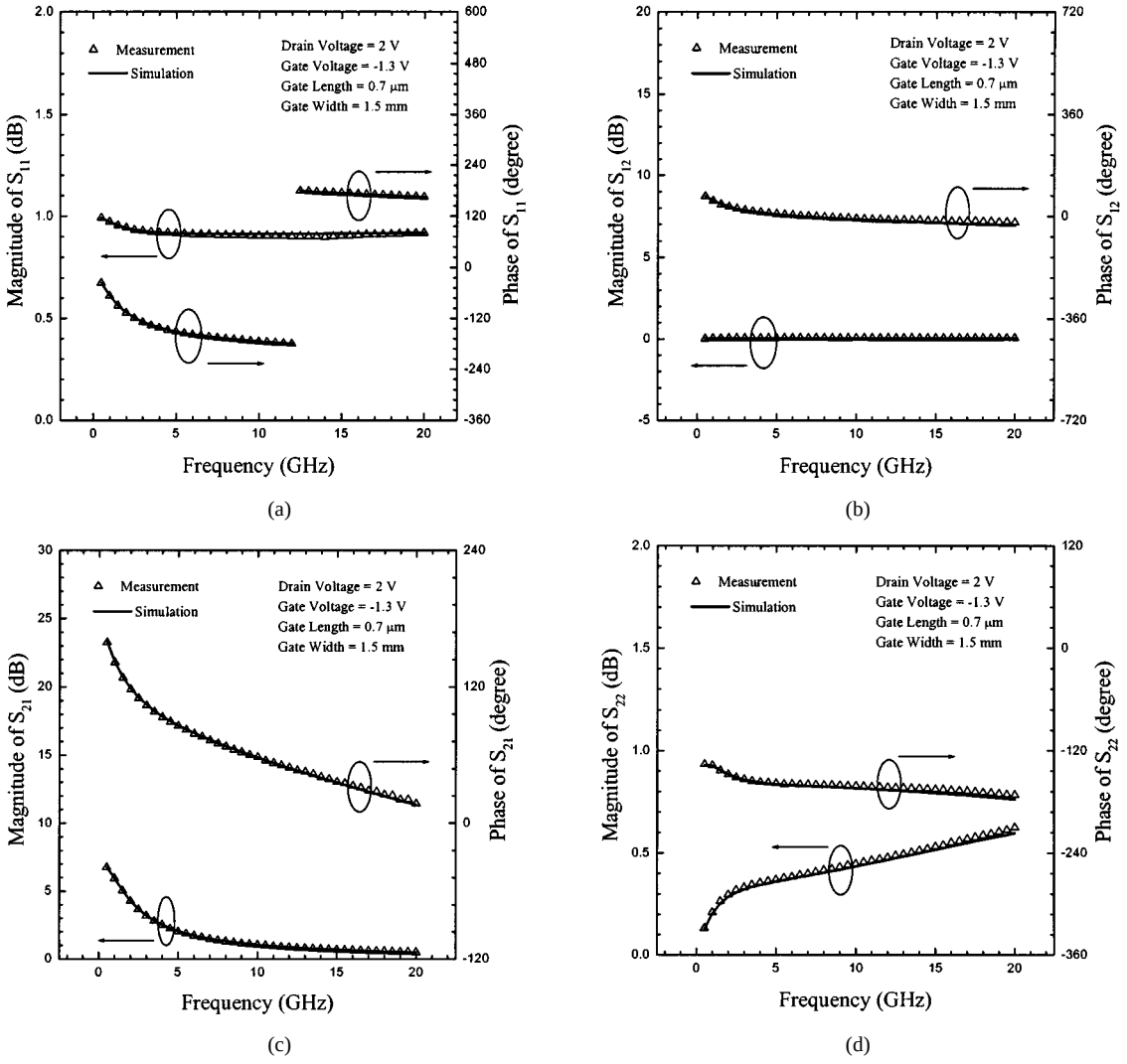

Fig. 9. Measured S-parameters (indicated by Δ) and simulated S-parameters (indicated by lines) of an active FET.

The drain-to-source depletion-layer capacitor was assumed to be identical to the gate-to-source and gate-to-drain depletion-layer capacitors in White's method. However, the fact is that the drain-to-source depletion-layer extension is not the same as the gate-to-source and the gate-to-drain depletion-layer extensions. Table I shows that the $C_{\rm pg}$ values in White's method are the same as those in Dambrine's method and the C_b values in White's method are always three times those in Dambrine's method, as indicated in (33)–(38). Since the drain-to-source depletion-layer capacitor values in White's method are overestimated, the extracted $C_{\rm pd}$ values are underestimated.

The reason the identical capacitors were used to describe the depletion-layer extension in the conventional methods is that the three low-frequency Y-parameter expressions $\mathrm{Im}(Y_{\rm total11})$, $\mathrm{Im}(Y_{\rm total12}) = \mathrm{Im}(Y_{\rm total21})$, and $\mathrm{Im}(Y_{\rm total22})$ can only uniquely solve three capacitance variables, i.e., $C_{\rm pg}$, $C_{\rm pd}$, and C_b. There is no way to have more different depletion-layer capacitors other than C_b being solved by conventional methods.

In this study, an intrinsic capacitor C_c is used to represent the drain-to-source depletion-layer capacitance, as shown in Fig. 1. According to the physically meaningful depletion-layer model, $C_{\rm pg}$, $C_{\rm pd}$, C_b, and C_c are solved simultaneously using the linear regression technique. The extraction results of Table I show that C_c is smaller than C_b because the drain-to-source depletion-layer extension is larger than the gate-to-source and gate-to-drain depletion-layer extensions. Physically meaningful C_b and C_c determine reasonable $C_{\rm pg}$ and $C_{\rm pd}$. The extraction results with physical significance are attributed to the novel extraction method and the correct equivalent circuit for the pinched-off cold FETs.

C. Small-Signal Equivalent Circuit

The new extraction method for $C_{\rm pg}$ and $C_{\rm pd}$ can be applied to obtain the small-signal equivalent-circuit model of the FET in the active region, as shown in Fig. 8 [14]. In addition to extrinsic parameters L_g, L_d, L_s, $C_{\rm pg}$, $C_{\rm pd}$, R_g, R_d, and R_s, the equivalent-circuit model of the FET has the intrinsic parameters including the gate-to-source capacitance ($C_{\rm gs}$), gate-to-drain capacitance ($C_{\rm gd}$), drain-to-source capacitance ($C_{\rm ds}$), intrinsic resistance (R_i), drain-to-source resistance ($R_{\rm ds}$), transconductance (g_m), and transit time (τ).

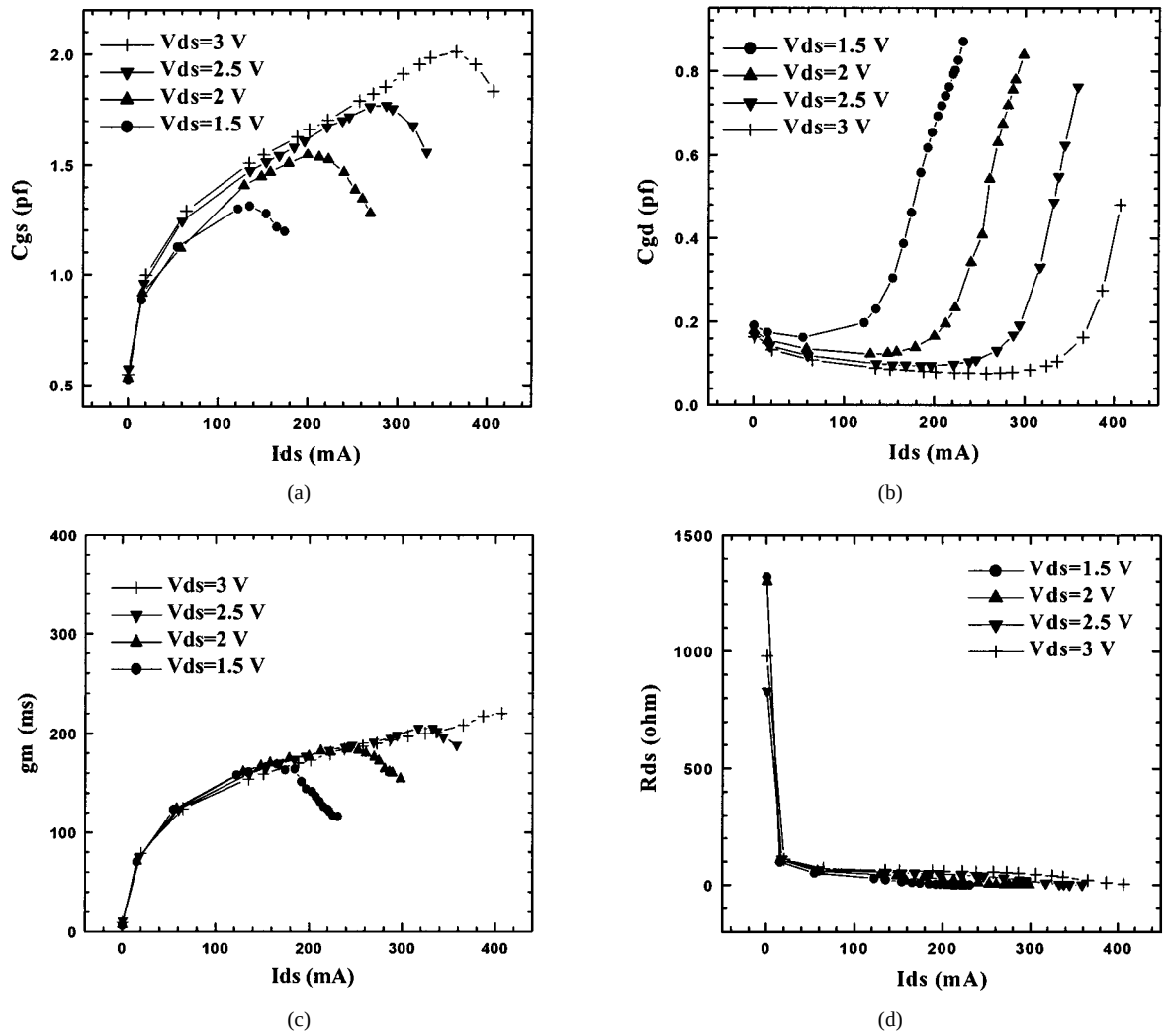

Fig. 10. Intrinsic element characteristics of the small-signal equivalent circuit for the FET as a function of drain-to-source current ($I_{\rm ds}$) and drain-to-source voltage ($V_{\rm ds}$). (a) $C_{\rm gs}$ characteristics. (b) $C_{\rm gd}$ characteristics. (c) g_m characteristics. (d) $R_{\rm ds}$ characteristics.

For the device with extrinsic parameters $L_g = 86.698$ pH, $L_d = 95.195$ pH, $L_s = 1.879$ pH, $C_{\rm pg} = 0.059$ pF, and $C_{\rm pd} = 0.065$ pF, the extrinsic resistances were extracted by the forward-gate-biased cold-FET method [14]. We obtained $R_g = 0.36\ \Omega$, $R_d = 0.50\ \Omega$, and $R_s = 0.48\ \Omega$.

The intrinsic elements of the small-signal equivalent-circuit model for a 0.7 μm $\times$ 1.5 mm GaAs MESFET biased at a drain-to-source voltage ($V_{\rm ds}$) of 2 V, a gate-to-source voltage ($V_{\rm gs}$) of -1.3 V and a drain-to-source current ($I_{\rm ds}$) of 158 mA were extracted by the intrinsic Y-parameter expressions [14], [18], [34], [35]. The saturation drain-to-source current ($I_{\rm dss}$) of the MESFET is 407 mA. The MESFET was biased at the class-AB condition. The intrinsic elements obtained are $C_{\rm gs} = 1.459$ pF, $C_{\rm gd} = 0.128$ pF, $C_{\rm ds} = 0.167$ pF, $R_i = 0.864\ \Omega$, $R_{\rm ds} = 39.625\ \Omega$, $g_m = 170$ mS, and $\tau = 1.951$ ps. As shown in the S-parameter data of Fig. 9, the simulated S-parameters based on the extracted parameters of the small-signal equivalent circuit exhibit great agreement with the measured S-parameters from 0.5 to 20 GHz. The new analytical method demonstrates accurate results for the small-signal equivalent-circuit modeling of the FETs.

On the basis of the equivalent-circuit method developed, we investigated the intrinsic element characteristics of the small-signal equivalent circuit for the FETs operating at different active biases. The S-parameters of the directly-ion-implanted MESFET [2] with a gate length of 0.7 μm, a gatewidth of 1.5 mm, and an $I_{\rm dss}$ of 407 mA at different active biases were measured. Fig. 10 shows the $C_{\rm gs}$, $C_{\rm gd}$, g_m, and $R_{\rm ds}$ characteristics of the MESFET as a function of $I_{\rm ds}$ and $V_{\rm ds}$ according to the equivalent-circuit simulation in conjunction with the measured S-parameters of the MESFET. $I_{\rm ds}$ corresponds with $V_{\rm gs}$. Fig. 10(a) illustrates the $C_{\rm gs}$ characteristics of the MESFETs. $C_{\rm gs}$ is very low, as the FET is in the pinched-off region. The $C_{\rm gs}$ increases after the FET is turned on. The $C_{\rm gs}$ characteristics as a function of $V_{\rm gs}$ can be explained by the depletion-layer distribution between the gate and source. The $C_{\rm gd}$ values as a function of $V_{\rm ds}$ and $I_{\rm ds}$ are shown in Fig. 10(b). The increase in $V_{\rm ds}$ increases the reverse bias between the gate and drain. This leads to the increase in the depletion-layer extension between the gate and drain and the decrease in the $C_{\rm gd}$. Fig. 10(c) shows the g_m characteristics of the MESFETs. The broadness and flatness of the g_m characteristics reflect the

linearity of the devices. The $R_{\rm ds}$ characteristics as a function of $V_{\rm ds}$ and $I_{\rm ds}$ are shown in Fig. 10(d). The devices in the pinched-off region have large $R_{\rm ds}$ values. The $R_{\rm ds}$ values are substantially reduced after the devices are turned on. The $R_{\rm ds}$ characteristics are similar for different $V_{\rm ds}$ biases.

The developed extraction method for the FET parasitic parameters provides the correct equivalent-circuit model for the evaluation of the microwave performance of the FETs and the design of the MMICs.

V. Conclusion

A novel analytical method has been presented in this paper to extract the parasitic capacitances $C_{\rm pg}$ and $C_{\rm pd}$ according to the Y-parameter frequency responses of the FETs and the linear regression technique. The Y-parameter frequency response equations are derived on the basis of the depletion-layer distribution with the physical meanings. The intercept-point and slope data of the regression lines associated with the measured Y-parameters of the FETs are used for the extraction of $C_{\rm pg}$ and $C_{\rm pd}$. The method improves the conventional methods and provides an accurate technique for the small-signal equivalent-circuit modeling of FETs.

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