A Charge Sheet Capacitance Model of Short Channel MOSFET's for SPICE

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***Abstract*—An analytic charge sheet capacitance model for short channel MOSFET's has been derived and implemented in SPICE.**

It is based on a surface potential formulation which computes the approximate surface potential without iterations. The dc current, charges, and their first and second derivatives are continuous under all operating regions. Equations for node charges have been derived to guarantee charge conservation. Short channel effects such as velocity saturation, channel length modulation, and channel-side-fringing-field capacitances have been included in the model equations.

This model shows good agreements with the measured gate capacitance for long and short channel MOSFET's. The SPICE simulation of a ring oscillator using this model shows the significant variation of circuit performance due to the short channel effects on capacitances.

NOTATIONS

x	Vertical dimension (Fig. 2).
y	Lateral dimension which is 0 at source and L at drain.
W	Effective channel width.
L	Effective channel length.
$\Psi(x, y)$	Electrostatic potential of silicon at (x, y).
$\Psi_S(y)$	Surface potential of a channel at y, referenced to the bulk.
Ψ_{SO}	Surface potential at source end of channel.
Ψ_{SL}	Surface potential at drain end of channel.
Φ_{MS}	Work function difference between gate material and silicon.
Q_{SS}	Surface state density.
V_{FB}	Flat band voltage.
V_{GB}	Applied voltage between gate and bulk (substrate).
V_{CB}	Voltage between channel and bulk.
V_{OX}	Voltage between gate and channel.
V_{GS}	Applied voltage between gate and source.
V_{DS}	Applied voltage between drain and source.
V_{BS}	Applied voltage between bulk and source.
V_{DB}	Applied voltage between drain and bulk.
V_{SB}	Applied voltage between source and bulk.
V_{DSSAT}	Drain saturation voltage (18).
V_{GST}	Equivalent to $(V_{GS} - V_{TH})$, but is non-negative (13.b).
V_{TH}	Threshold voltage in conventional notation.
VDS	Effective drain to source voltage (10).
I_D	DC drain current.
I'_D	Normalized dc drain current (21.c).
q	An electronic charge.
ϵ_s	Permittivity of silicon.
ϵ_{ox}	Permittivity of silicon dioxide.
$N_A(x, y)$	Bulk (substrate) doping concentration at (x, y).
N_{SUB}	Bulk (substrate) doping concentration, the same as $N_A(x, y)$ but the uniform substrate doping concentration is assumed.
$p(x, y)$	Hole concentration density at (x, y).
$n(x, y)$	Electron concentration density at (x, y).
n_i	Intrinsic carrier concentration of silicon.
ϕ_t	Thermal voltage, kT/q.
Φ_F	$\phi_t \cdot \log_e (N_{SUB}/n_i)$.
F_B	Correction factor for the bulk (substrate) charge effect (13.c).
$Q'_n(y)$	Inversion charge density, normalized by WC_{OX}.
$Q'_b(y)$	Bulk charge density, normalized by WC_{OX}.
Q_G	Total gate charge.
Q_D	Total drain charge.
Q_S	Total source charge.
Q_B	Total bulk charge.
C_{GG}	Gate capacitance, $\partial Q_G/\partial V_G$.
C_{GD}	Gate capacitance, $\partial Q_G/\partial V_D$.
C_{GB}	Gate capacitance, $\partial Q_G/\partial V_B$.
C_{GS}	Gate capacitance, $\partial Q_G/\partial V_S$.
$\mu_n(y)$	Mobility of carriers at a channel point y (15).
μ_{no}	Long channel mobility (no velocity saturation).
v_{SAT}	Maximum drift velocity of channel carriers.
E_{EFF}	Effective vertical electric field at the surface of silicon (source end).
E_{CRIT}	Critical electric field for the V_{GS} dependence of mobility.
$v_{DRIFT}(y)$	Drift velocity of carriers at a channel point y.
λ_{DG}	Coupling factor between drain junction and gate for channel length modulation (16.e).
λ_{GP}	Coupling factor between gate and pinchoff point for channel length modulation (16.e).
E_L	Lateral electric field in the pinchoff region (16.e).
T_{OX}	Gate oxide thickness.
C_{OX}	Gate oxide capacitance per unit area.
γ	Bulk effect coefficient, $\sqrt{2\epsilon_s q N_{SUB}}/C_{OX}$.
$E_x(x, y)$	Vertical electric field of silicon at (x, y).
$E_S(y)$	Vertical electric field at the surface of silicon $(E_x(0, y))$.
SF( )	Cubic spline function for the saturation function $S(z)$ (9).
CSF ( )	Cubic spline function for Ψ_S as a function of $(V_{GB} - V_{FB})$ at $V_{CB} = 0$.

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A	Model parameter to determine the smoothness of the transition between the linear and saturation regions (9).
V_O	Equation (21.b).
V_L	Equation (22.b).
$C1$	Channel-side-outer-fringing-field capacitance (Fig. 5).
$C2$	Direct overlap capacitance between gate and source or drain (Fig. 5).
$C3$	Channel-side-inner-fringing-field capacitance ($C3S$ and $C3D$ in Fig. 5).
T_{GATE}	Thickness of gate electrode (Fig. 5).
LD	Lateral diffusion of source, drain junction (Fig. 5).
X_J	Junction depth of source, drain junction (Fig. 5).
α	Slanting angle of gate electrode (Fig. 5) in radians.
δ	Equation (30.c).
C_F	Maximum value of $C3$ (31).
$Q_{D.F}$	Change of drain charge due to $C3$.
$Q_{S.F}$	Change of source charge due to $C3$.

I. Introduction

AN ACCURATE capacitance model is essential for accurate simulation of high-speed digital and analog circuits. Many studies have been done on MOSFET dc models [1]–[19], but considerably fewer studies have been done on MOSFET capacitance models [20]–[32], [9], [12]. One reason for this is the fact that the measurement of MOSFET capacitances has been difficult especially for small geometry MOSFET's. Only recently have sensitive MOSFET measurement systems been developed [33]–[39], [31]. Another reason for this is the fact that capacitance models can be fully evaluated only if they are implemented in circuit simulation programs. Implementation of capacitance models in a circuit simulation program requires in-depth understanding of the program and is much more difficult than the implementation of dc models. Hence, only a few capacitance models have been successfully implemented.

All the MOSFET models available in SPICE are piecewise-sectional models in which different sets of model equations are used for different operating regions. Usually, current and charges are continuous at boundaries between operating regions, but derivatives of current and charges (conductances and capacitances) are discontinuous. Specifically, many capacitance components are discontinuous at the threshold voltage. These discontinuities cause convergence problems in transient circuit simulations.

The opposite approaches to the above mentioned piecewise-sectional models are the double integration model by Pao and Sah [2], similar approaches reported in [13] and [14], and the charge sheet model by Brews [7] and [8]. In these models, current, charges, and their derivatives with respect to bias are continuous under all operating regions, since only one equation is used for all operating regions. This continuity property is highly beneficial for the convergence property of circuit simulation programs which use the Newton-Raphson method to solve circuit equations [40], [41]. The double integration model [2] is an accurate model for long channel MOSFET's, but too much computation time is required. The charge sheet model [7] is a simplified form of the double integration model. It assumes that the channel carriers form an infinitely thin layer of conducting sheet at the interface between silicon and oxide. Hence, the computation time of the charge sheet model is less than that of the double integration model. Compared to the conventional piecewise multisection models [3], [4], [9], [21], [22], [28] available in circuit simulation programs, the charge sheet model [7], [8], [27] still takes much longer computation time, since many time consuming iterations are required to find surface potentials at source and drain. Hence, in spite of all the advantages of the charge sheet model, it is not widely used in real circuit simulation programs.

In this paper, an approximation is made to find surface potentials without iterations or losing accuracy. Adopting a linear approximation of the square root term for the bulk charge [5], [6], analytic expressions for current and charges including the drift velocity saturation effect and the diffusion current component, have been derived. Also, the channel length modulation effect and the channel-side-fringing-field capacitance components are included in the model equations as semi-empirical terms. This model has been implemented in SPICE3 and simulation results are shown. Earlier versions of this work were reported in [31] and [42] but many enhancements have been done in this paper.

Recently, a similar work was reported by Yu *et al.* [32]. However, in [32], a two-dimensional array is stored to compute the surface potentials and numerical integrations are used to compute current and charges. In this work, analytic equations are derived for current and charge equations and only two values of surface potential (one at the source end and the other at the drain end of the channel) are required and they are computed using cubic spline functions.

The geometry dependence of threshold voltage and the drain-induced barrier lowering effect are not included in this work.

II. Formulation of Surface Potential

2.1. Noniterative Solution of Surface Potential

Fig. 1 shows an energy band diagram of a MOS system. Ψ_S is the surface potential referenced to the bulk (substrate). We want to find the surface potential as a function of $(V_{GB} - V_{FB})$ and V_{CB}. V_{GB} is the voltage applied between gate and bulk. V_{FB} is the flat band voltage. V_{CB} is the voltage between channel and bulk. Expressions for charge densities can be derived as functions of Ψ_S and $(V_{GB} - V_{FB})$. Fig. 2 shows a cross section of NMOSFET. Inside the silicon, we have the two-dimensional Poisson equation:

$$\frac{\partial^2\Psi(x, y)}{\partial x^2} + \frac{\partial^2\Psi(x, y)}{\partial y^2} = \frac{q}{\epsilon_s}\left(N_A(x, y) - p(x, y) + n(x, y)\right) \tag{1}$$

where $\Psi(x, y)$ is the electrostatic potential at a point (x, y), $N_A(x, y)$ is the effective ionized acceptor concentration, and $p(x, y)$ and $n(x, y)$ are hole and electron concentrations, respectively. $N_A(x, y)$, $p(x, y)$ and $n(x, y)$ can be represented in terms of n_i, $\Psi(x, y)$, and $V_{CB}(y)$, where n_i is the intrinsic carrier concentration:

$$N_A(x, y) = n_i \cdot e^{\Phi_F/\phi_t} \tag{2.a}$$

$$n(x, y) = n_i \cdot \exp\left(\Psi(x, y) - \Phi_F - V_{CB}(y)\right)/\phi_t \tag{2.b}$$

$$p(x, y) = n_i \cdot \exp\left(-\Psi(x, y) + \Phi_F\right)/\phi_t \tag{2.c}$$

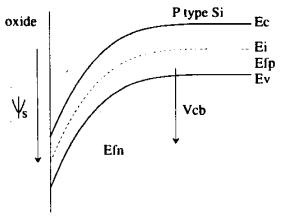


Fig. 1. Cross section of a NMOS system. Gate is not shown for clarity. *Efn* and *Efp* are quasi-Fermi levels of electrons and holes, respectively. *Ec* and *Ev* represent the edges of the conduction band and the valence band, respectively.

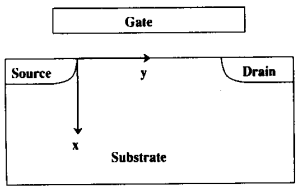


Fig. 2. Cross section of a NMOSFET in the channel length direction. y is the lateral dimension from source ($y = 0$) toward drain ($y = L$). x is the vertical dimension from the surface ($x = 0$) toward the bulk substrate.

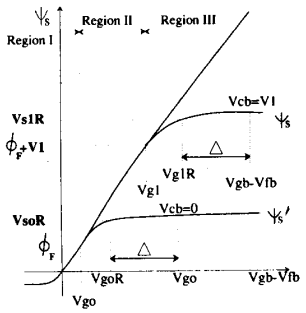


Fig. 3. Surface potential Ψ_S versus ($V_{GB} - V_{FB}$) with V_{CB} as parameters. For $V_{CB} = V1$, Region I corresponds to the region of ($V_{GB} - V_{FB}$) < Vgo, Region II corresponds to the region of $Vgo \le (V_{GB} - V_{FB}) < Vg1$, Region III corresponds to the region of ($V_{GB} - V_{FB}$) $\ge Vg1$.

where

$$\Phi_F = \phi_t \cdot \log_e (N_{SUB}/n_i). \tag{2.d}$$

Uniform bulk (substrate) doping concentration is assumed ($N_A(x, y) = N_{SUB}$ for all x, y) and ϕ_t is the thermal voltage kT/q. $V_{CB}(y)$ is the difference between quasi-Fermi levels, Efn in the channel and Efp in the bulk as shown in Fig. 1.

If we assume the gradual channel approximation, that is, assuming

$$\left|\frac{\partial^2 \Psi(x, y)}{\partial x^2}\right| \gg \left|\frac{\partial^2 \Psi(x, y)}{\partial y^2}\right| \tag{3}$$

we can neglect the y dependence of $\Psi(x, y)$ in (1).

We now integrate both sides of (1) with respect to Ψ from the neutral bulk to the surface of silicon using (2.a)–(2.d) and also the following relation (4) [18]:

$$\int_0^{\Psi_S(y)} \frac{\partial^2 \Psi(x, y)}{\partial x^2}\, d\Psi = \int_0^{E_S(y)} \frac{\partial E_x(x, y)}{\partial x} \cdot E_x(x, y)\, dx = \frac{1}{2} \cdot (E_S(y))^2 \tag{4}$$

where $E_x(x, y)$ is the x component of the electric field at (x, y); and $E_S(y)$ and $\Psi_S(y)$ are the x components of the electric field and the surface potential at the surface of silicon, respectively. The vertical (x component) electric field $E_S(y)$ can be represented in terms of V_{OX}, the voltage across gate oxide and the surface state density Q_{SS}, as

$$E_S(y) = \frac{C_{OX}}{\epsilon_s} \cdot \left(V_{OX}(y) + \frac{Q_{SS}}{C_{OX}}\right) = \frac{C_{OX}}{\epsilon_s} \cdot (V_{GB} - V_{FB} - \Psi_S(y)) \tag{5.a}$$

where

$$V_{FB} = \Phi_{MS} - \frac{Q_{SS}}{C_{OX}} \tag{5.b}$$

where C_{OX} is the gate oxide capacitance per unit area, Φ_{MS} is the work function difference between the gate material and silicon, and V_{FB} is the flat band voltage. Using (2)–(4) and (5.a), the integration of (1) yields

$$V_{GB} - V_{FB} - \Psi_S(y) = \pm\gamma\sqrt{\Psi_S(y) - \phi_t + \phi_t \cdot \exp\left(\Psi_S(y) - 2\Phi_F - V_{CB}(y)\right)/\phi_t + \phi_t \cdot e^{-\Psi_S(y)/\phi_t}} \tag{6.a}$$

where

$$\gamma = \frac{\sqrt{2\epsilon_s q N_{SUB}}}{C_{OX}}. \tag{6.b}$$

In the derivation of (6.a), we have one more term ($-\phi_t \cdot e^{(-2\Phi_F - V_{CB}(y))/\phi_t}$) inside the square root. However, this term is neglected since ($2\Phi_F \gg \phi_t$) and ($V_{CB}(y) \ge 0$). This is equivalent to assuming that the electron concentration in the neutral bulk (p-type substrate) is zero.

The + sign before the square root term in (6.a) is used for ($V_{GB} - V_{FB}$) ≥ 0 and the − sign is used for ($V_{GB} - V_{FB}$) < 0 (accumulation region). The Ψ_S term inside the square root in (6.a) originates from the fixed bulk charge and the ($-\phi_t$) term is due to the hole concentration in the neutral bulk. The first exponential term in (6.a) is due to the channel inversion charge (electron) and the second exponential term is due to the accumulation charge (hole) at the surface of silicon, respectively.

Some researchers calculated the surface potential from this exact equation ((6.a)) but many time consuming iterations are required. This time consuming iteration is often prohibitive in circuit simulation programs because, in some circuits, the surface potential needs to be evaluated millions of times in one simulation.

We will, instead, make an approximation to find the surface potential without iterations. Fig. 3 shows the surface potential versus ($V_{GB} - V_{FB}$) for $V_{CB} = 0$ and $V_{CB} = V1$, where $V1$ is non-negative. Vgo is ($V_{GB} - V_{FB}$) where the surface potential is Φ_F. $Vg1$ is ($V_{GB} - V_{FB}$) where the surface potential is ($\Phi_F + V_1$). $VgoR$ and $Vg1R$ are reference gate voltages which will be used in the inversion region (operating region III). Vgo and

$Vg1$ can be found from (6.a) by neglecting the two exponential terms, that is, assuming the mobile carrier density at the surface of silicon to be zero. Hence, $Vgo = \Phi_F + \gamma\sqrt{\Phi_F - \phi_t}$ and $Vg1 = \Phi_F + V1 + \gamma\sqrt{\Phi_F + V1 - \phi_t}$.

The curve for $V_{CB} = 0$ can be found from (6.a) by calculating $(V_{GB} - V_{FB})$ for given Ψ_S by simple substitution. This curve is then stored in the form of a cubic spline function [31], [42].

The cubic spline function is a piecewise, cubic polynomial and it guarantees the continuity of surface potential and its first and second derivatives with respect to applied biases. In this work the curve for $V_{CB} = 0$ is divided into 150 pieces with $\Delta\Psi_S = 0.01$ V for the range of Ψ_S from -0.3 to 1.2 V and the linear (natural) end condition is used [43], [44]. The memory requirement for storing the cubic spline coefficients are 600 double precision numbers per model, which is not large in modern computers.

We now consider how to find the surface potential for $V_{CB} = V1$, where $V1$ is a non-negative constant. The curve for $V_{CB} = V1$ is divided into 3 operating regions which are shown in Fig. 3.

a) Operating Region I (Accumulation or Depletion Region):

$$\left(\Psi_S < \Phi_F, \text{ that is, } (V_{GB} - V_{FB}) < \left(\Phi_F + \gamma\sqrt{\Phi_F - \phi_t}\right)\right).$$

This operating region corresponds to either accumulation or part of depletion region where the surface of silicon is accumulated with holes or is depleted of mobile carriers. In this operating region Ψ_S is independent of V_{CB} because n (electron concentration) and Efn (quasi-Fermi level of electron) (see Fig. 1) are unimportant. Therefore, Ψ_S can be computed directly from the stored cubic spline function.

b) Operating Region II (Depletion Region):

$$\left(\Phi_F \le \Psi_S < (\Phi_F + V_{CB}), \text{ that is, } (\Phi_F + \gamma\sqrt{\Phi_F - \phi_t})\right.$$
$$\left. \le (V_{GB} - V_{FB}) < \left(\Phi_F + V_{CB} + \gamma\sqrt{\Phi_F + V_{CB} - \phi_t}\right)\right).$$

This operating region corresponds to the depletion region where the surface of silicon is depleted of mobile carriers. Neglecting the two exponential terms in (6.a) which are related to inversion or accumulation carriers, we can find that (6.a) is reduced to a quadratic equation in Ψ_S. Hence, an analytic equation for Ψ_S can be derived as

$$\Psi_S = V_{GB} - V_{FB} + 0.5\gamma^2 - \gamma\sqrt{V_{GB} - V_{FB} + 0.25\gamma^2 - \phi_t}. \quad (7.a)$$

c) Operating Region III (Inversion Region):

$$\left(\Psi_S \ge (\Phi_F + V_{CB}), \text{ that is, } (V_{GB} - V_{FB})\right.$$
$$\left. \ge (\Phi_F + V_{CB} + \gamma\sqrt{\Phi_F + V_{CB} - \phi_t})\right).$$

This operating region corresponds to the inversion region where the surface of silicon is inverted with electrons. In this operating region, Ψ_S can be computed from (7.b) if the normalized inversion charge density Q_n' is known:

$$Q_n' = V_{GB} - V_{FB} - \Psi_S - \gamma\sqrt{\Psi_S - \phi_t}. \quad (7.b)$$

For $V_{CB} = 0$, Q_n' can be computed from the stored cubic spline function. For nonzero V_{CB}, Q_n' can be found if the same Q_n' is assumed for the same Δ for each V_{CB} curve, where Δ is the displacement in gate voltage from the reference point $Vg1R$ for each V_{CB} curve, as shown in Fig. 3, i.e.:

$$\Delta = V_{GB} - V_{FB} - Vg1R. \quad (7.c)$$

The reference point $Vg1R$ for each V_{CB} curve can be found by substituting $\Psi_S = Vs1R$ in (6.a) and neglecting the surface accumulation charge term. Hence:

$$Vg1R = Vs1R + \gamma\sqrt{Vs1R - \phi_t + \phi_t \cdot \exp\left(Vs1R - 2\Phi_F - V_{CB}\right)/\phi_t} \quad (7.d)$$

where

$$Vs1R = 2\Phi_F \cdot \left(1.025 + \frac{5.524 \cdot 10^{-2}}{\gamma + 0.520}\right) + V_{CB}. \quad (7.e)$$

In the earlier versions of this paper [31], [42], $Vs1R$ is set to $(2\Phi_F + V_{CB})$ and the exponential term in (7.d) is not used. This caused $(\partial\Psi_S/\partial V_{CB})$ to be slightly larger than 1 in the strong inversion region for $V_{CB} = 0$ [42]. The new formulation shown in (7.d) and (7.e) guarantees that $0 \le (\partial\Psi_S/\partial V_{CB}) \le 1$ for $\gamma \ge 0.15$.

Once Δ is found from (7.c) for some $(V_{CB} = V1)$ curve, Q_n' can be computed for the same Δ in the $(V_{CB} = 0)$ curve using the cubic spline function. Then Ψ_S can be computed from the computed Q_n' using (7.b) as

$$\Psi_S = V_{GB} - V_{FB} - Q_n' + 0.5\gamma^2 - \gamma\sqrt{V_{GB} - V_{FB} - Q_n' + 0.25\gamma^2 - \phi_t}. \quad (7.f)$$

The program for computing Ψ_S is shown in [42]. The above algorithm can, of course, be applied to the subthreshold region [42].

2.2. Surface Potential at Source and Drain

The surface potential at the source end, Ψ_{SO}, is computed using the previous algorithm for $V_{CB} = V_{SB}$. The surface potential at the drain end, Ψ_{SL}, is computed from V_{DS} and V_{DSSAT}, where V_{DS} is the applied drain-to-source voltage and V_{DSSAT} is the drain saturation voltage. Hence Ψ_{SL} can be written as

$$\Psi_{SL} = \Psi_{SO} + \text{VDS} \quad (8)$$

where VDS is the effective drain to source voltage. Conceptually VDS $= V_{DS}$ is the linear region and VDS $= V_{DSSAT}$ is the saturation region. To make the smooth transition for VDS between linear and saturation regions, a smooth function which we call "saturation function," S, is derived as

$$S(z) = 1 - \frac{\log_e\left(1 + e^{A(1-z)}\right)}{\log_e\left(1 + e^{A}\right)} \quad (9)$$

where z is V_{DS}/V_{DSSAT}. Fig. 4 shows the saturation function with different values of A. Large A gives a steep transition between the linear and saturation regions and small A gives a smooth transition. This parameter A is set to be a model parameter in the implementation. However, the computation of (9) is costly in computer time because it includes time consuming exponential and logarithmic functions. For the computational efficiency, another cubic spline function (SF) ( ) is derived from (9). The saturation function (9) is computed only once in the

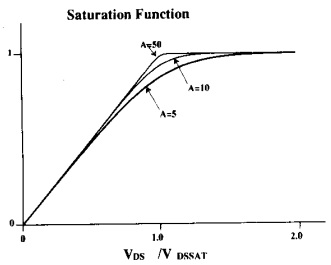


Fig. 4. The saturation function $S(z)$ in (9) for different values of A.

SPICE setup stage to compute the cubic spline coefficients of SF ( ), and SF ( ) is repeatedly used for the model computation.

Hence, the effective drain to source voltage VDS is computed from

$$\text{VDS} = \text{SF}\left(\frac{V_{\text{DS}}}{V_{\text{DSSAT}}}\right) \cdot (V_{\text{DSSAT}} - V_{\text{DSSAT.0}}) \tag{10}$$

where $V_{\text{DSSAT.0}}$ is V_{DSSAT} at $V_{\text{GST}} = 0$. In the previous versions of this work [31], [42], only V_{DSSAT} is used instead of ($V_{\text{DSSAT}} - V_{\text{DSSAT.0}}$) in (10), and that scheme did not give the correct exponential variation of the dc drain current in the subthreshold region. The new scheme in (10) fixed this problem.

III. Derivation of Current and Charge Equations

3.1. Bulk Charge Approximation

In the inversion and depletion regions where $\Psi_S > \Phi_F$, the normalized bulk charge density $Q_b'(y)$ can be represented in terms of surface potential Ψ_S as

$$Q_b'(y) = \gamma\sqrt{\Psi_S(y) - \phi_t}. \tag{11}$$

To find simple analytic charge equations which include the velocity saturation effect, we need a linear relationship between $Q_b'(y)$ and $\Psi_S(y)$ [5], [6]. For this purpose, the square root term in (11) is approximated as

$$\begin{aligned}\sqrt{\Psi_S(y) - \phi_t} &= \sqrt{(\Psi_{\text{SO}} - \phi_t) + (\Psi_S(y) - \Psi_{\text{SO}})} \\ &\approx \sqrt{\Psi_{\text{SO}} - \phi_t} + \frac{g}{2\sqrt{\Psi_{\text{SO}} - \phi_t}} \cdot (\Psi_S(y) - \Psi_{\text{SO}})\end{aligned} \tag{12.a}$$

where

$$g = 1 - \frac{1}{1.744 + 0.8364 \cdot (\Psi_{\text{SO}} - \phi_t)}. \tag{12.b}$$

This approximation was introduced by Poon *et al.* [6] and was used also in BSIM [15]. Using the approximation (12.a), the normalized inversion charge density $Q_n'(y)$ for ($\Psi_{\text{SO}} > \Phi_F$) can be represented as

$$\begin{aligned}Q_n'(y) &= V_{\text{GB}} - V_{\text{FB}} - \Psi_S(y) - \gamma\sqrt{\Psi_S(y) - \phi_t} \\ &= V_{\text{GST}} - F_B \cdot (\Psi_S(y) - \Psi_{\text{SO}})\end{aligned} \tag{13.a}$$

where

$$V_{\text{GST}} = V_{\text{GB}} - V_{\text{FB}} - \Psi_{\text{SO}} - \gamma\sqrt{\Psi_{\text{SO}} - \phi_t} \tag{13.b}$$

$$F_B = 1 + \frac{g\gamma}{2\sqrt{\Psi_{\text{SO}} - \phi_t}}. \tag{13.c}$$

V_{GST} in (13.b) is equivalent to ($V_{\text{GS}} - V_{\text{TH}}$) in the conventional notation, but V_{GST} always has a non-negative value. F_B has a value slightly larger than 1.0 and is usually between 1.1 and 1.3. In (12.a), the two terms ($\Psi_{\text{SO}} - \phi_t$) and ($\Psi_S(y) - \Psi_{\text{SO}}$) are symmetric before the approximation but they are no longer symmetric after the approximation. This causes an asymmetry problem between source and drain capacitances when V_{DS} becomes 0, but the overall effect of this asymmetry on circuit simulation results is small.

3.2. Current Equations

The dc drain current I_D can be written as the sum of drift and diffusion components, following the charge sheet formulation [7]:

$$I_D = WC_{\text{OX}} \cdot \mu_n(y) \cdot \left(Q_n'(y) \cdot \frac{d\Psi_S(y)}{dy} - \phi_t \cdot \frac{dQ_n'(y)}{dy}\right). \tag{14}$$

The Einstein relation ($D = \mu \cdot \phi_t$) is used in this derivation. The velocity saturation effect on the mobility is modeled as

$$\mu_n(y) = \frac{\mu_{no}}{1 + \mu_{no} \cdot \dfrac{d\Psi_S(y)/dy}{v_{\text{SAT}}}} \tag{15}$$

where μ_{no} is the mobility at a given gate voltage and v_{SAT} is the carrier saturation velocity. Substituting (15) into (14) and integrating both sides of the resulting equation from source to drain, we can derive an analytic equation for the dc drain current I_D. Including the effect of the channel length modulation ΔL, we can obtain the final equation for I_D as

$$\begin{aligned}I_D = \mu_{no} C_{\text{OX}} \frac{W}{L} &\cdot \frac{1}{1 + \dfrac{\mu_{no}(\Psi_{\text{SL}} - \Psi_{\text{SO}})}{v_{\text{SAT}} L}} \cdot \frac{1}{1 - \dfrac{\Delta L}{L}} \\ &\cdot (V_{\text{GST}} + F_B \cdot \phi_t - 0.5 \cdot F_B \cdot (\Psi_{\text{SL}} - \Psi_{\text{SO}})) \\ &\cdot (\Psi_{\text{SL}} - \Psi_{\text{SO}})\end{aligned} \tag{16.a}$$

where

$$\mu_{no} = \frac{\mu_o}{1 + \dfrac{E_{\text{EFF}}}{E_{\text{CRIT}}}} \tag{16.b}$$

$$\begin{aligned}E_{\text{EFF}} &= \frac{C_{\text{OX}}}{\epsilon_s} \cdot (0.5 \cdot Q_n'(0) + Q_b'(0)) \\ &= \frac{C_{\text{OX}}}{\epsilon_s} \cdot (0.5 \cdot V_{\text{GST}} + \gamma\sqrt{\Psi_{\text{SO}} - \phi_t})\end{aligned} \tag{16.c}$$

$$\Delta L = \frac{V_{\text{DS}} - \text{VDS}}{E_L} \tag{16.d}$$

$$\begin{aligned}E_L = \sqrt{\frac{qN_{\text{SUB}}(V_{\text{DS}} - \text{VDS})}{2\epsilon_s}} + \frac{C_{\text{OX}}}{\epsilon_s} &\cdot (\lambda_{\text{DG}} \cdot (V_{\text{DS}} - V_{\text{GS}} + V_{\text{FB}}) \\ &+ \lambda_{\text{GP}} \cdot (V_{\text{GS}} - V_{\text{FB}} - \text{VDS}))\end{aligned} \tag{16.e}$$

μ_o is the zero field mobility. E_{EFF} is the effective vertical electric field at the surface of silicon and it is computed following the schemes in [45]. For the channel length modulation ΔL in (16.d), we followed the equation in [46] by replacing V_{DSSAT} in [46] by VDS. E_L in (16.e) is the lateral electric field in the pinch-off region including the two coupling terms. E_{CRIT}, v_{SAT}, λ_{DG}, and λ_{GP} are model parameters.

3.3. Drain Saturation Voltage V_{DSSAT}

From (13.a) and (14) and using $v_{DRIFT}(y) = \mu_n(y) \cdot (d\Psi_S(y)/dy)$, we can derive (17) at $y = L$:

$$I_D = WC_{OX} \cdot v_{DRIFT}(L) \cdot (V_{GST} + F_B\phi_t - F_B \cdot (\Psi_{SL} - \Psi_{SO})) \quad (17)$$

where L is the effective channel length.

The drain saturation voltage V_{DSSAT} is defined as the effective drain to source voltage VDS, i.e., $(\Psi_{SL} - \Psi_{SO})$, at which the drift velocity at the drain end of the channel reaches the saturation velocity, i.e., $v_{DRIFT}(L) = v_{SAT}$.

From (16.a) and (17) we can find V_{DSSAT} as

$$V_{DSSAT} = -\frac{v_{SAT}L}{\mu_{no}} + \sqrt{\left(\frac{v_{SAT}L}{\mu_{no}}\right)^2 + 2 \cdot \frac{v_{SAT}L}{\mu_{no}} \cdot \frac{(V_{GST} + F_B\phi_t)}{F_B}}. \quad (18)$$

In this derivation, the channel length modulation effect is not included. For the very long channel MOSFET's, V_{DSSAT} in (18) is reduced to $(V_{GST}/F_B + \phi_t)$. This agrees with the SPICE level-3 model [9] except the thermal voltage term which is due to the diffusion component.

3.4. Charge Equations

In circuit simulations for MOSFET, we need charge and capacitance equations associated to each node in order to compute the transient or small-signal node currents. Capacitance equations can be derived analytically from charge equations by applying derivatives with respect to node voltages. For this purpose, the operating regions are divided into two regions: a) where $\Psi_{SO} \geq \Phi_F$, and b) where $\Psi_{SO} < \Phi_F$. Region a) corresponds to either the inversion or depletion region and Region b) corresponds to the accumulation or depletion region.

3.4.1. Charge Equations for $\Psi_{SO} \geq \Phi_F$: In this region, expressions for node charges can be derived from the following equations:

$$Q_G = WC_{OX} \cdot \int_0^L V_{OX}(y)\,dy = WC_{OX} \cdot \int_0^L \left(V_{GB} - V_{FB} - \frac{Q_{SS}}{C_{OX}} - \Psi_S(y)\right) dy \quad (19.a)$$

$$Q_B = -WC_{OX} \cdot \int_0^L \gamma\sqrt{\Psi_S(y) - \phi_t}\,dy \quad (19.b)$$

$$Q_D = -WC_{OX} \cdot \int_0^L Q_n'(y) \cdot \frac{y}{L}\,dy \quad (19.c)$$

$$Q_S = -(Q_G + Q_B + Q_D + WLQ_{SS}) \quad (19.d)$$

where Q_G, Q_B, Q_D, and Q_S are gate, bulk, drain, and source charges, respectively. In (19.a), V_{OX} is the voltage across the gate and all the oxide charges and the interface states are approximated as the term (Q_{SS}) which is located at the interface between oxide and silicon. Q_{SS} is assumed to be constant all along the channel ($0 \leq y \leq L$). This Q_{SS} adjustment results in a bias independent offset term in the Q_G expression and it does not affect capacitance values. To get Q_D in (19.c), we followed the Oh, Ward, and Dutton's channel charge partitioning scheme [23] which can be derived analytically from the current continuity equation. The derivation of (19.c) is shown in [23] and is repeated in [47] and [42].

To derive analytic equations for node charges, we represent Ψ_S in terms of y. For this purpose, (14) is converted to

$$I_D\,dy = WC_{OX} \cdot \mu_n(y) \cdot \left(Q_n'(y) - \phi_t \cdot \frac{dQ_n'(y)}{d\Psi_S}\right) \cdot d\Psi_S. \quad (20)$$

Substituting (13.a) and (15) into (20) and integrating the resulting equation from source to some channel point y, we can find

$$\Psi_S(y) - \Psi_{SO} = \frac{1}{F_B} \cdot \left(V_O - \sqrt{V_O^2 - 2F_BI_D' \cdot \frac{y}{L}}\right) \quad (21.a)$$

where

$$V_O = V_{GST} + F_B\phi_t - \frac{\mu_{no}I_D'}{v_{SAT}L} \quad (21.b)$$

$$I_D' = \frac{I_D \cdot \left(1 - \frac{\Delta L}{L}\right)}{\mu_{no} \cdot \frac{W}{L} C_{OX}} \quad (21.c)$$

where I_D' is the normalized drain current which does not include the channel length modulation effect. I_D' has a unit of $[V^2]$.

Substituting (21.a) into (19.a), we can find the gate charge Q_G as

$$Q_G = WLC_{OX} \cdot \left\{V_{GB} - V_{FB} - \frac{Q_{SS}}{C_{OX}} - \Psi_{SO} - \frac{V_O}{F_B} + \frac{V_O^3 - V_L^3}{3F_B^2I_D'}\right\} \quad (22.a)$$

where

$$V_L = \sqrt{V_O^2 - 2F_BI_D'}. \quad (22.b)$$

Using the linear approximation of the square root term as shown in (12.a), the bulk charge Q_B in (19.b) can be rewritten as

$$Q_B = -WC_{OX} \cdot \int_0^L \gamma\sqrt{\Psi_{SO} - \phi_t} + (F_B - 1) \cdot (\Psi_S(y) - \Psi_{SO}) \cdot dy. \quad (23.a)$$

Substituting (21.a) into (23.a), we can find

$$Q_B = -WLC_{OX} \cdot \left\{\gamma\sqrt{\Psi_{SO} - \phi_t} + \left(1 - \frac{1}{F_B}\right) \cdot \left(V_O - \frac{V_O^3 - V_L^3}{3F_BI_D'}\right)\right\}. \quad (23.b)$$

The drain charge Q_D can be derived by substituting (13.a) and (21.a) into (19.c), as

$$Q_D = -WLC_{OX} \cdot \left\{ \frac{\mu_{no} I'_D}{2 v_{SAT} L} - \frac{F_B \phi_t}{2} + \frac{\frac{2}{3} V_O^2 \cdot (V_O^3 - V_L^3) - \frac{2}{5}(V_O^5 - V_L^5)}{(2F_B I'_D)^2} \right\}. \quad (24)$$

The source charge Q_S can be computed from the other three components as shown in (19.d).

In the charge equations (22.a), (23.b), and (24), when the normalized drain current I'_D goes to 0, both nominator and denominator go to zero in some terms. Hence, for very small I'_D where $(\Psi_{SL} - \Psi_{SO}) \approx 0$, the charge equations are approximated into their asymptotic forms as

$$Q_G = WLC_{OX} \left\{ V_{GB} - V_{FB} - \frac{Q_{SS}}{C_{OX}} - 0.5 \cdot (\Psi_{SL} + \Psi_{SO}) \right\} \quad (25.a)$$

$$Q_B = -WLC_{OX} \left\{ \gamma \sqrt{\Psi_{SO} - \phi_t} + 0.5 \cdot (F_B - 1) \cdot (\Psi_{SL} - \Psi_{SO}) \right\} \quad (25.b)$$

$$Q_D = -WLC_{OX} \left\{ 0.5 \cdot V_{GST} - \frac{F_B \cdot (\Psi_{SL} - \Psi_{SO})}{3} \right\} \quad (25.c)$$

$$Q_S = -(Q_G + Q_B + Q_D + WLQ_{SS}). \quad (25.d)$$

3.4.2. Charge Equations for $\Psi_{SO} < \Phi_F$: In this operating region, (13.a) for the normalized inversion charge density Q'_n is not valid and so the previously derived (22.a), (23.b), and (24) cannot be used. In this region, $\Psi_S(y) = \Psi_{SO}$ and $Q'_n(y) = 0$ for all y $(0 \le y \le L)$. Hence:

$$Q_G = WLC_{OX} \cdot \left(V_{GB} - V_{FB} - \frac{Q_{SS}}{C_{OX}} - \Psi_{SO} \right) \quad (26.a)$$

$$Q_B = -(Q_G + WLQ_{SS}) \quad (26.b)$$

$$Q_D = 0 \quad (26.c)$$

$$Q_S = 0. \quad (26.d)$$

3.5. Channel Length Modulation for Charge Components

For short channel MOSFET's, the total inversion charge changes appreciably as the effective channel length varies [42]. By substituting (21.a) into (13.a), we can find the channel charge density profile $Q'_n(y)$ as

$$Q'_n(y) = \frac{\mu_{no} I'_D}{v_{SAT} L} - F_B \phi_t + \sqrt{V_O^2 - 2F_B I'_D \cdot \frac{y}{L}}. \quad (27)$$

When the effective channel length L is changed to $(L - \Delta L)$, the profile of the difference can be approximated as

$$\Delta Q'_n(y) = Q'_n(y)\big|_{(L-\Delta L)} - Q'_n(y)\big|_L = -\frac{\partial Q'_n(y)}{\partial L} \cdot \Delta L. \quad (28.a)$$

From (27), we can derive

$$\frac{\partial Q'_n(y)}{\partial L} = -\frac{1}{1 + \frac{\mu_{no}(\Psi_{SL} - \Psi_{SO})}{v_{SAT} L}} \cdot \left(\frac{\mu_{no} I'_D}{v_{SAT} L^2} + \frac{\partial Q'_n(y)}{\partial y} \cdot \left(\frac{y}{L} + \frac{\mu_{no} V_O}{F_B v_{SAT} L} \right) \right). \quad (28.b)$$

Using (28.a) and (28.b), we can derive the change of each node charge due to channel length modulation as

$$\Delta Q_D = -WC_{OX} \cdot \int_0^L \Delta Q'_n(y) \cdot \frac{y}{L} dy = -\frac{1}{1 + \frac{\mu_{no}(\Psi_{SL} - \Psi_{SO})}{v_{SAT} L}} \cdot \frac{\Delta L}{L} \cdot \left(2 \cdot Q_D + \frac{\mu_{no} V_O}{F_B v_{SAT} L}(Q_D + Q_S) + WC_{OX} \frac{\mu_{no}}{v_{SAT}} \left(1.5 I'_D + \frac{V_O}{F_B}(V_{GST} - V_O + V_L) \right) + WLC_{OX}(V_L - F_B \phi_t) \right) \quad (29.a)$$

$$\Delta Q_S = -WC_{OX} \cdot \int_0^L \Delta Q'_n(y) \cdot \left(1 - \frac{y}{L}\right) dy = \frac{1}{1 + \frac{\mu_{no}(\Psi_{SL} - \Psi_{SO})}{v_{SAT} L}} \cdot \frac{\Delta L}{L} \cdot \left(Q_D - Q_S + \frac{\mu_{no} V_O}{F_B v_{SAT} L} \cdot (Q_D + Q_S) + WC_{OX} \cdot \frac{\mu_{no}}{v_{SAT}} \cdot \left(-0.5 I'_D + \frac{V_O V_{GST}}{F_B} \right) \right). \quad (29.b)$$

Assuming $\Delta Q_B = 0$ for simplicity, then we have

$$\Delta Q_G = -(\Delta Q_D + \Delta Q_S) = WC_{OX} \cdot \int_0^L \Delta Q'_n(y)\, dy = \frac{1}{1 + \frac{\mu_{no}(\Psi_{SL} - \Psi_{SO})}{v_{SAT} L}} \cdot \frac{\Delta L}{L} \cdot \left(Q_D + Q_S + WC_{OX} \frac{\mu_{no}}{v_{SAT}} \cdot \left(2 I'_D - \frac{V_O(V_O - V_L)}{F_B} \right) + WLC_{OX}(V_L - F_B \phi_t) \right). \quad (29.c)$$

The same ΔL in (16.d) is used for the channel length modulation for charges as well as for the dc drain current.

3.6. Channel-Side-Fringing-Field Capacitance

For short channel MOSFET's, the channel side stray capacitances have made significant contribution to the total gate capacitance [48]. Channel side stray capacitances have three

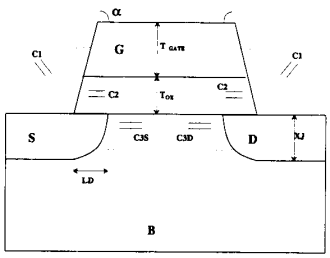


Fig. 5. Cross section of a NMOSFET to show the three components of the channel side stray capacitances, $C1$, $C2$, and $C3$ [48].

components $C1$, $C2$, and $C3$ as shown in Fig. 5. $C1$ is the outer-fringing-field capacitance between gate and source or drain electrode. $C2$ is the direct overlap capacitance between gate and source or drain junction. $C3$ is the inner-fringing-field capacitance between gate and the side wall of the source or drain junction. $C3$ becomes nonzero when the channel is depleted of mobile carriers and so some electric fields originating from the gate are terminated at the side wall of source or drain junction.

For $C1$, $C2$, and $C3$, we followed the equations in [48]:

$$C1 = W \cdot \frac{\epsilon_{ox}}{\alpha} \cdot \log_e\left(1 + \frac{T_{GATE}}{T_{OX}}\right) \tag{30.a}$$

$$C2 = W \cdot \frac{\epsilon_{ox}}{T_{OX}}\left(LD + 0.5 \cdot T_{OX} \cdot \left(\frac{1 - \cos\alpha}{\sin\alpha} + \frac{1 - \cos\delta}{\sin\delta}\right)\right) \tag{30.b}$$

where

$$\delta = 0.5 \cdot \pi \cdot \frac{\epsilon_{ox}}{\epsilon_s} \tag{30.c}$$

where α is the slanting angle of gate electrode in radians, T_{GATE} is the thickness of the gate electrode, W is the channel width, and LD is the metallurgical lateral diffusion of source, drain junction as shown in Fig. 5. ϵ_{ox} and ϵ_s are the dielectric constants of oxide and silicon, respectively. C_F is the maximum value of the inner-fringing capacitance component $C3$:

$$C_F = W \cdot \frac{\epsilon_{ox}}{\delta} \cdot \log_e\left(1 + \frac{X_J \cdot \sin\alpha}{T_{OX}}\right) \tag{31}$$

where X_J is the depth of the source, drain junctions. The capacitance components $C1$ and $C2$ are bias-independent and they are added to gate–drain or gate–source overlap capacitances, C_{GDO} and C_{GSO} [9]. The capacitance component $C3$ is bias-dependent and it is modeled as a charge based form. Hence:

$$Q_{D.F} = -C_F \cdot \frac{V_{DS} - VDS}{1 + \exp\left(-\frac{V_{GB} - V_{FB}}{30\phi_t}\right)} \tag{32.a}$$

$$Q_{S.F} = -C_F \cdot \frac{V_{GST} - V_{GS} + V_{FB} + 2\Phi_F + \gamma\sqrt{2\Phi_F - V_{BS}}}{1 + \exp\left(-\frac{V_{GB} - V_{FB}}{30\phi_t}\right)}. \tag{32.b}$$

$Q_{D.F}$ is added to the drain charge Q_D, $Q_{S.F}$ is added to the source charge Q_S and $-(Q_{D.F} + Q_{S.F})$ is added to Q_G. The exponential term in (32.a) and (32.b) is added to guarantee that the channel-side-fringing-field capacitance is 0 in the accumulation region. Conceptually, the nominator in (32.a) is 0 in the linear region and it is linearly dependent on $(V_{DS} - V_{DSSAT})$ in the saturation region. Similarly, the nominator in (32.b) is 0 when $V_{GS} > V_{TH}$ and it is proportional to $(-V_{GS} + V_{TH})$ when $V_{GS} < V_{TH}$. The constant 30 in (32.a) and (32.b) is a heuristic factor to determine the slope of the transition.

IV. Capacitance Measurement System

To extract model parameters, an automatic direct-on-wafer off-chip gate capacitance measurement system has been developed. This system is similar to the system reported earlier [34]. However, it has been fully automated now by using the switching matrix scanner and the resolution has been enhanced by an order of magnitude to about 14 aF. This off-chip capacitance measurement technique [31], [34], [37] has advantages over the on-chip technique [33], [35], [36], [39] in the flexibility, and over the off-the-shelf technique [38] in the resolution, respectively. The details of this measurement system used in this work are shown in [31] and [42].

V. Comparison of the Model with the Measured Data

5.1. Surface Potential and Its Derivatives

To check the validity of the surface potential formulation scheme shown in Section II-2.1, the calculated values using this scheme are compared with the measured data. The surface potential and its derivatives with respect to bias can be extracted from the MOSFET gate capacitance measurement. When drain and source nodes are tied together, the surface potential $\Psi_S(y)$ is constant all along the channel ($0 \le y \le L$) and Ψ_S can be computed as (see [18, eq. (7.40)]):

$$\Psi_S = \int_{V_{FB}}^{V_{GB}} \left(1 - \frac{C_{GG}}{WLC_{OX}}\right) dV_G \tag{33}$$

where we used the fact that Ψ_S is 0 at $V_{GB} = V_{FB}$ (flat band voltage). V_{FB} can be extracted from the capacitance measurement [19] or the threshold voltage measurement. In this work V_{FB} can be adjusted to fit the calculated data.

Fig. 6 shows the comparison between calculated values and the measured data for a PMOSFET with $W/L = 100\ \mu m/100\ \mu m$ and the uniform substrate doping concentration.

In Fig. 6, slight discrepancies can be observed between measured and calculated surface potentials at around the flat band voltage ($-V_{GB} = -V_{FB} = -0.11$ V). This is probably due to the slight decrease of the substrate doping concentration at the very surface of silicon due to the threshold-adjustment-implantation.

An algorithm for finding the surface potential Ψ_S for MOSFET's with nonuniform substrate doping concentrations and its comparison with measurements are shown in [42].

5.2. Gate Capacitances of Long Channel MOSFET's

Fig. 7(a)–(c) shows the comparison of the measured and the calculated gate capacitances for a long channel NMOSFET with

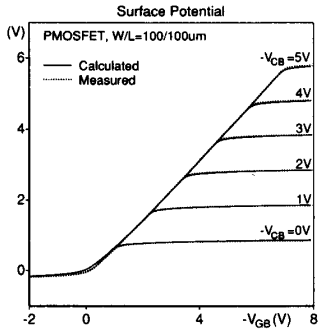


Fig. 6. Comparison of the measured and the calculated surface potential curves for the long channel PMOSFET. The measured data have been extracted from the measured C_{GG} using (33). The model parameters used for the calculated curve are $V_{FB} = 0.11$ V, $N_{SUB} = 3.5 \cdot 10^{15}$ cm^{-3}, $T_{OX} = 58.6$ nm, and $\gamma = 0.58\sqrt{V}$.

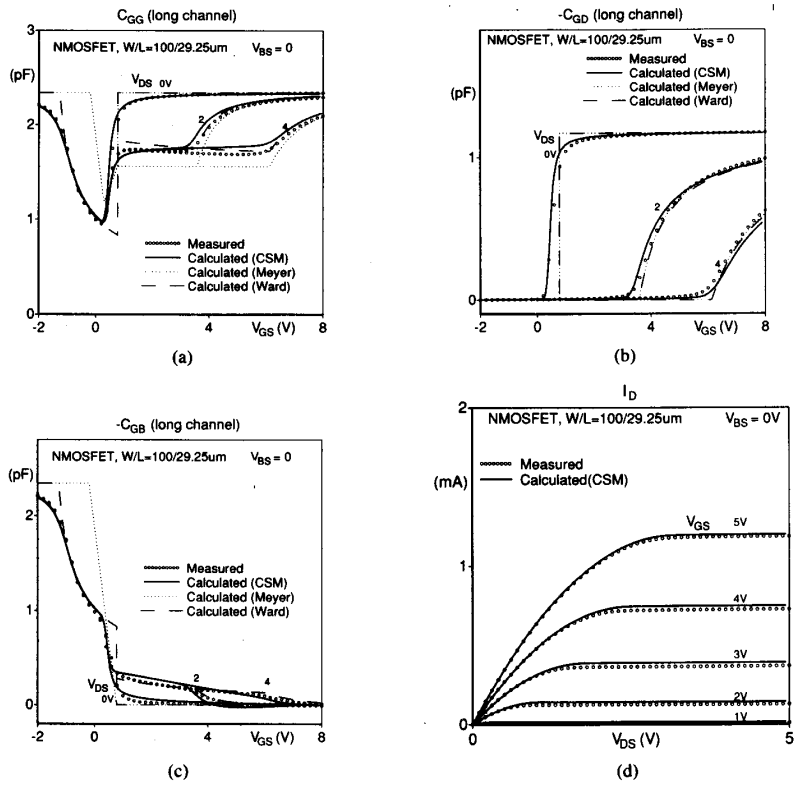


Fig. 7. Comparison of the measured and the calculated gate capacitances and dc drain current for a long channel NMOSFET with $W/L = 100$ μm/29.25 μm (effective dimension). This work (CSM), the Meyer, and the Ward–Dutton models in SPICE2 are used to get the calculated values. Model parameters used for the calculation are $T_{OX} = 43$ nm, $V_{FB} = -1.26$ V, $N_{SUB} = 2.3 \cdot 10^{16}$ cm^{-3}, $\mu_0 = 800$ cm^2/(V · s), $E_{CRIT} = 10^6$ V/cm, $v_{SAT} = 2.0 \cdot 10^7$ cm/s, $\lambda_{DG} = 0.5$, $\lambda_{GP} = 1.0$, *satfactor* (A in (9)) = 20, $X_J = 0.17$ μm, $T_{GATE} = 0.7$ μm, and $\alpha = 90$ deg. (a) C_{GG}. (b) C_{GD}. (c) C_{GB}. (d) I_D versus V_{DS}.

$W/L = 100$ μm/29.25 μm (effective dimension). Calculated values using the Meyer model [21] and the Ward–Dutton model [22] in SPICE2, are also shown for comparison. Fig. 7(d) shows the dc drain current versus V_{DS}, as a reference.

5.2.1. C_{GG}: In the C_{GG} curve shown in Fig. 7(a), the Meyer model gives large errors from the measured data in the cutoff and saturation regions, since the bulk charge effect is neglected in the Meyer model. The Ward–Dutton model gives

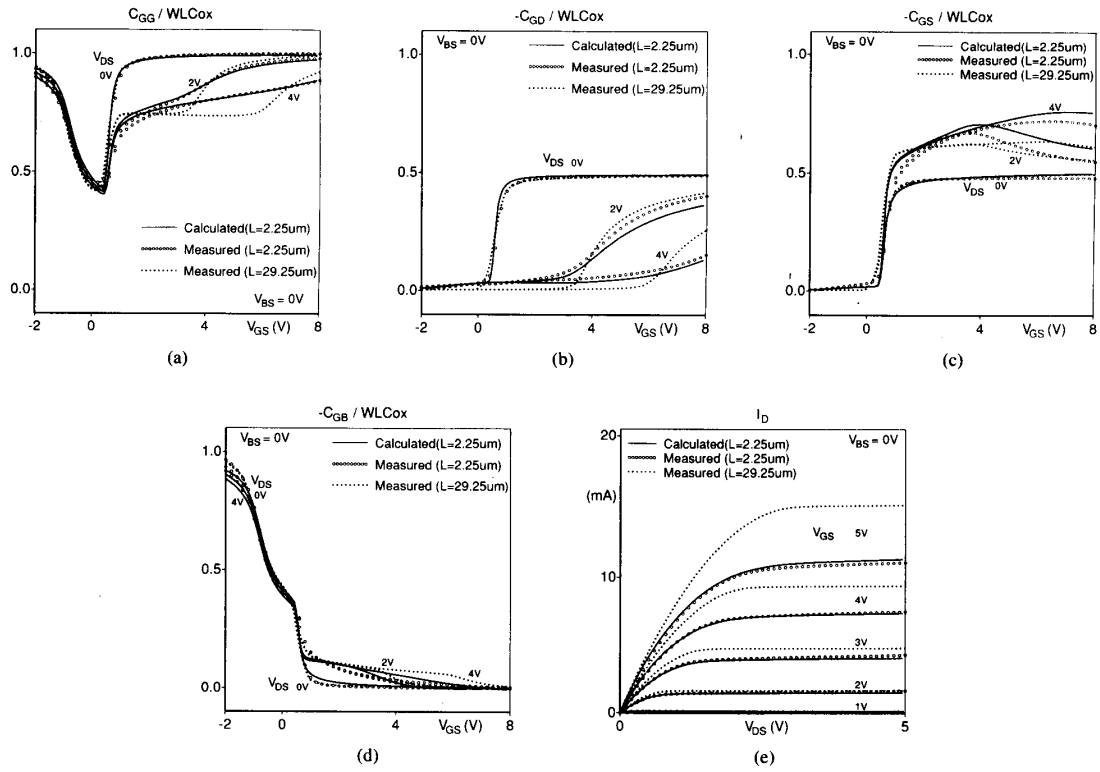


Fig. 8. Comparison of measured and calculated gate capacitances and dc drain current for a short channel NMOSFET with $W/L = 100\ \mu m/2.25\ \mu m$ (effective dimension). The measured data of a long channel NMOSFET are also shown for comparison. The same model parameter values as in Fig. 7 are used for the calculation except $V_{FB} = -1.06$ V, $N_{SUB} = 2 \cdot 10^{16}$ cm^{-3}, *satfactor* (A in (9)) = 5. (a) C_{GG}. (b) C_{GD}. (c) C_{GS}. (d) C_{GB}. (e) I_D versus V_{DS}.

large errors in the subthreshold region and has discontinuities at the threshold voltage ($V_{GS} = V_{TH}$). The charge sheet model (CSM) presented in this paper shows good agreement with the measured data. The continuity of the capacitance and its slope is especially excellent.

5.2.2. C_{GD}: In the C_{GD} curve shown in Fig. 7(b), all the models show fair agreements with the measured data except the discontinuities of the Meyer and Ward–Dutton models at $V_{GS} = V_{TH}$ for $V_{DS} = 0$. Also, the charge sheet MOSFET (CSM) model and the measured data show smooth transitions between the linear and saturation regions, but the Meyer and the Ward–Dutton models show abrupt transitions in slope between the two regions. This smooth transition is due to the diffusion current which is included in this work but is not included in the Meyer or the Ward–Dutton model. Also, a slight channel length modulation effect can be observed in the saturation region both in the measured data and this work (CSM).

5.2.3. C_{GB}: In the C_{GB} curve shown in Fig. 7(c), the Meyer model gives large errors from the measured data in the cutoff region and it predicts that $C_{GB} = 0$ for $V_{GS} \geq V_{TH}$ independently of V_{DS}. This is due to the neglect of the bulk charge effect in the Meyer model. The Ward–Dutton model gives good agreement with the measured data in the strong inversion region ($V_{GS} > V_{TH}$) but it gives a discontinuity at $V_{GS} = V_{TH}$. This work gives good agreement with the measured data except slight mismatches in the saturation region.

5.2.4. I_D: Fig. 7(d) shows the dc drain current I_D versus V_{DS} using the same model parameter set which is used in the capacitance calculation shown in Fig. 7(a)–(c). Excellent agreements can be observed between measured and calculated data.

In this work, all the model parameters were extracted using a curve fitting.

5.3. Gate Capacitances of Short Channel MOSFET's

Fig. 8(a)–(d) shows the comparisons of the measured and calculated gate capacitances for a short channel NMOSFET with $W/L = 100\ \mu m/2.25\ \mu m$ (effective dimension). The measured data of a long channel NMOSFET are also shown for comparison. The capacitance components are normalized by the total gate oxide capacitance WLC_{OX}. The velocity saturation effect, the channel length modulation effect on charges, and the fringing-field capacitances which are described in Section III, are also included in the calculation. The measured data and the calculated data using this work show pronounced short channel effects and they give good agreements with other data measured using different techniques [33], [35], [36], [38], [39], and also with the two-dimensional device simulation results [49], [50]. Bias-independent stray capacitances, such as $C1$ and $C2$ in Fig. 5, are not included in the figures for clarity.

Fig. 8(e) shows the dc drain current versus V_{DS}, as a reference.

5.3.1. C_{GG}: In the C_{GG} curve shown in Fig. 8(a), the CSM shows good agreement with the measured data. In the saturation region, appreciable differences can be observed between long and short channel C_{GG}. C_{GG} decreases as V_{DS} increases, in the cutoff and saturation regions. This is due to the fringing-field capacitances which are shown in $C3S$ and $C3D$ in Fig. 5. As V_{DS} increases, the depletion region of the drain junction becomes wider and the less bulk charge is under control of the gate-to-bulk electric field (the charge sharing effect).

5.3.2. C_{GD}: In the C_{GD} curve shown in Fig. 8(b), appreciable short channel effects can be observed. The calculated and the measured short channel C_{GD} show good agreement between each other. However, the measured long channel C_{GD} shows appreciable differences from this work or the measured short channel C_{GD}. The C_{GD} component is the most important one among four gate capacitance components, because its effect is multiplied by the voltage gain between drain and gate nodes due to the Miller effect.

In the cutoff region (where $V_{GS} < V_{TH}$), the calculation and the measurement for the short channel MOSFET show that C_{GD} increases with V_{GS}, while the long channel C_{GD} is constant at 0. This is due to the fringing-field capacitance component $C3D$ shown in Fig. 5 and the increase of the depletion layer depth with increasing V_{GS}.

With $V_{GS} > V_{TH}$, in the saturation region, the short channel C_{GD} is nonzero and increases with V_{GS}, but the long channel C_{GD} is constant at 0. This nonzero C_{GD} in the saturation region is due to the combination of two effects. One effect is again due to the fringing-field capacitance component $C3D$ shown in Fig. 5 which gives a constant capacitance C_F shown in (31) independently of V_{GS}. The other effect is due to the channel length modulation on channel charges, which is described in Section III-3.5. From (16.d) and (29.c), C_{GD}, due to the channel length modulation effect, can be approximated as $(Q_D + Q_S)/(E_L' L)$ if the velocity saturation effect is neglected. E_L' is the average lateral electric field in the pinch-off region. Since the magnitudes of Q_D and Q_S increase with V_{GS}, C_{GD}, due to channel length modulation, increases in magnitude with V_{GS} in the saturation region.

With $V_{GS} > V_{TH}$, in the linear region, C_{GD} of short channel MOSFET's is smaller than that of long channel MOSFET's especially for the ($V_{DS} = 4$ V) curve. This is due to the velocity saturation effect which causes the total channel charge of short channel MOSFET's to be less sensitive to the drain voltage than that of long channel MOSFET's in the linear region [31]–[39], [49].

5.3.3. C_{GS}: In the cutoff region (where $V_{GS} < V_{TH}$), the short channel C_{GS} (Fig. 8(c)) is nonzero and increases with V_{GS} due to the channel-side-fringing-field capacitance $C3S$ shown in Fig. 5. This $C3S$ component becomes 0 in the strong inversion region ($V_{GS} > V_{TH}$), as shown in (32.b). In the saturation region, the short channel C_{GS} decreases with the increase of V_{DS}, while the long channel C_{GS} is constantly independent of V_{DS}. This is due to the channel length modulation effect, as can be verified in (29.c) [42].

At large V_{GS}, in the linear region, the short channel C_{GS} can be much larger than the long channel C_{GS} especially for the ($V_{DS} = 4$ V) curve. This is due to the velocity saturation effect which causes the channel charge density near the drain to be proportional to I_D, and hence, modulating V_S has an additional effect on the channel charge through the change in I_D.

5.3.4. C_{GB}: In the C_{GB} curve shown in Fig. 8(d), the splitting of C_{GB} for different V_{DS} can be observed in the cutoff region ($V_{GS} < 0.5$ V) due to the fringing-field capacitance components ($C3D$ and $C3S$ in Fig. 5). Larger V_{DS} results in smaller C_{GB} in the cutoff region. As V_{DS} increases, more bulk charge becomes associated with the electric field lines originating from the drain junction, therefore, less bulk charge is available to modulate the gate charge (the charge sharing effect). In the strong inversion region, the short channel C_{GB} is much smaller than the long channel C_{GB} for the same reason.

5.3.5. I_D: Fig. 8(e) shows the measured and calculated short channel I_D along with the measured long channel I_D. The long channel I_D is multiplied by the ratio of the effective channel length (29.25/2.25). The same model parameter set as in the capacitance calculation (from Fig. 8(a)–(d)) is used for the short channel I_D calculation. The square law dependence of the saturation current on ($V_{GS} - V_{TH}$) can be observed for the long channel I_D, but almost a linear dependence can be observed for the short channel I_D, especially for high V_{GS}. This clearly demonstrates the velocity saturation effect.

VI. Simulation Results and Performance Comparison

6.1. Transient Gate Current of a NMOSFET

Fig. 9(a) and (b) shows the simulation results for the turn-on and the turn-off transients of a NMOSFET using this CSM model and the SPICE level 2 charge based model ($XQC = 0.4$) [9], [22]. Since there is a discontinuity of the gate capacitance C_{GG} at the threshold voltage in the SPICE level 2 charge based model [9], as shown in Fig. 7(a), its simulated current oscillates whenever the gate voltage crosses the threshold voltage (V_{TH}) as shown in Fig. 9(a) and (b). The period of oscillation corresponds to the internal time step used in SPICE. On the contrary, the CSM model generates a stable gate current waveform because of the continuity of the gate capacitance C_{GG} all over the operating regions, as shown in Fig. 7(a). The trapezoidal integration is used and the same convergence criterion is used for the two simulations.

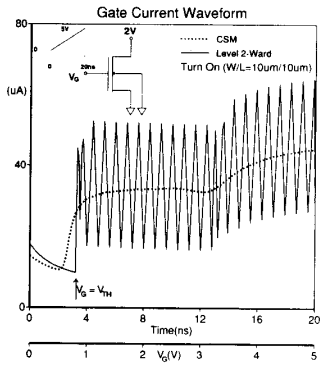
6.2. Output Voltage Waveform of a Ring Oscillator

Fig. 10 shows the simulated output voltage waveforms of an 11-stage E-D NMOS ring oscillator. The effective channel length of all MOSFETs is 2.25 μm.

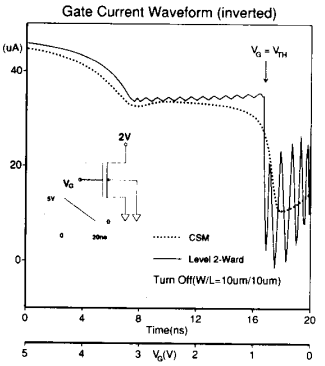
The curve (1) includes all the short channel effects discussed in this paper. The curve (2) does not include the channel-side-fringing-field capacitances $C1$ and $C3$ shown in Fig. 5 by setting $X_J = 0$ and $T_{GATE} = 0$. The curve (3) does not include the channel-side-fringing field capacitances as in the curve (2), and furthermore it does not include the channel length modulation effect for charge (29). However, both the velocity saturation effect and the overlap capacitance $C2$ are included in all the three simulation curves (1)–(3).

Table I shows the unit delay time of an inverter stage which has been calculated from Fig. 10. The significant contribution of the short channel effects on capacitances to the circuit performance can be observed. The fringing-field capacitances have larger influences on the delay time (5.3%) than the channel length modulation for charge (2.5%).

Table II shows the values of each capacitance component for an enhancement driver ($W/L = 10\ \mu m/2.25\ \mu m$) used in the



(a)



(b)

Fig. 9. Comparison of the gate current waveforms during the turn-on and turn-off transients of a NMOSFET, simulated using this work (CSM) and the SPICE level 2 charge based model (Level 2-Ward). (a) Turn-on transient. (b) Turn-off transient.

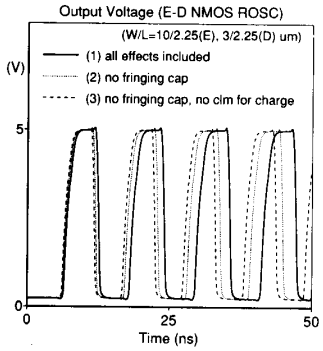


Fig. 10. The output voltage waveforms of an 11-stage E-D NMOS ring oscillator simulated using this work. The same model parameters in Fig. 8 and the lateral diffusion $LD = 0.375\ \mu m$, the unit area junction capacitance $C_J = 4.07 \cdot 10^{-4}\ F/M^2$ are used for the SPICE simulation.

ring oscillator of Fig. 10. The sum of fringing capacitances $C1$ and CF is 9.4% of the intrinsic gate capacitance WLC_{OX}. Although the junction capacitance at the output node $C_J \cdot A_J$ is still dominant in values, these fringing capacitances contribute to the Miller capacitance between gate and drain along with the overlap capacitance $C2$ and the effective values become much larger due to the multiplication by the voltage gain.

TABLE I
THE DELAY TIME OF AN INVERTER STAGE OF THE RING OSCILLATOR IN FIG. 10. THE NUMBERS INSIDE PARENTHESES REPRESENT THE PERCENT VARIATIONS

Simulation Curves	Curve (1)	Curve (2)	Curve (3)
Unit delay time	526 ps (0%)	498 ps (−5.3%)	485 ps (−7.8%)

6.3. *Performance Comparison between Models in SPICE3*

Comparisons of run statistics have been made for some circuits using the CSM model (this work), the level-2 Meyer model and BSIM 40/60 ($x$part = 0) and BSIM 0/100 ($x$part = 1) models [15], [28] available in SPICE3. The ratios 40/60 and 0/100 models refer to the ratios of drain and source charges in saturation region, respectively. Table III shows the comparison of the CPU time per model computation. This work takes about twice as much longer than the conventional MOSFET models in SPICE3.

Table IV shows the comparison of run statistics of the transient analysis of an NMOS op amp in the unity gain configuration, and this work (CSM model) results in a reduction in required iterations and it demonstrates the better convergence property of the CSM model than other models. This is due to its continuity property of current, charges, and their derivatives with respect to biases.

Table V shows the run statistics of the ac analysis of an NMOS op amp in the open loop configuration. Simulation using this work requires fewer dc operational iterations than other models in dc operating point computation (dc op).

VII. CONCLUSION

An analytic charge sheet capacitance model of short channel MOSFET's has been derived and implemented in SPICE3. No iterations are needed to find the surface potential. The model equations are charge-based and include the drift velocity saturation effect, the diffusion current, and the effect of the bulk charge in analytic derivation steps. Also, the channel length modulation effect on charges, and the channel-side-fringing-field capacitances are included in the model as semi-empirical terms. The dc drain current, node charges, and their first and second derivatives are continuous under all operating regions. This continuity property improves the convergence property in circuit simulations.

An automatic gate capacitance measurement system has been used to extract model parameters. Comparison of this model with the measured gate capacitances of short channel MOSFET's shows good agreement.

The SPICE simulation of an E-D NMOS ring oscillator using this model shows the significant variation of the circuit performance due to the short channel effects on capacitances.

Comparison of the circuit simulation run statistics using this model implemented in SPICE3 and other models in SPICE3 shows that using this model requires much fewer iterations, due to the continuity property of this model.

TABLE II
THE VALUES OF CAPACITANCE COMPONENT OF AN ENHANCEMENT DRIVER OF THE RING OSCILLATOR IN FIG. 10. THE VALUES INSIDE PARENTHESES REPRESENT THE PERCENT RATIOS WITH RESPECT TO THE INTRINSIC GATE CAPACITANCE WLC_{OX}

Components	$C1$	$C2$	CF	WLC_{OX}	$C_J \cdot A_J$
Values (fF)	0.63 (3.5%)	3.23 (17.9%)	1.06 (5.9%)	18.07 (100%)	12.21 (67.6%)

TABLE III
COMPARISON OF CPU TIME PER MODEL COMPUTATION USING THE VAX 8800 RUNNING ULTRIX V.2.2. "CSM" IS THE CHARGE SHEET MOSFET MODEL (THIS WORK) AND "MEYER" IS THE SPICE LEVEL 2 WITH THE MEYER CAPACITANCE MODEL. BSIM IS THE BERKELEY SHORT-CHANNEL IGFET MODEL [15], [28]

Model	CSM	Meyer	BSIM
CPU time per model	2.2 ms	0.7 ms	1.0 ms

TABLE IV
RUN STATISTICS OF THE TRANSIENT ANALYSIS OF AN NMOS OP AMP IN UNITY GAIN CONFIGURATION. BSIM0 AND BSIM1 REFER TO THE BSIM 40/60 ($x$part = 0) AND BSIM 0/100 ($x$part = 1) PARTITIONING MODELS, RESPECTIVELY [15], [28]

Model	CSM	Meyer	BSIM0	BSIM1
Total CPU Time(s)	32	16	18	18
Number of Iterations	435	532	491	493
Total Time Pts.	137	150	150	151
Reject. Time Pts.	16	14	18	20
Load Time(s)	28	11	14	14

TABLE V
THE RUN STATISTICS OF THE AC ANALYSIS OF AN NMOS OP AMP IN THE OPEN LOOP CONFIGURATION

Model	CSM	Meyer	BSIM0	BSIM1
Total CPU Time(s)	3.0	2.1	3.4	3.4
DC OP Iterations	24	25	97	97
Load Time (seconds)	1.3	0.4	1.3	1.3

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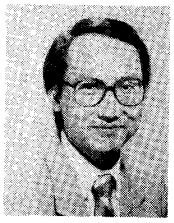

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