Pranav M

pranav0x0112 | Pranav M | https://prawns.dev/ | pranav.m1205@gmail.com |

About Me

Undergraduate ECE student interested indigital hardware, processor design, and embedded systems. Currently building open-source RISC-V cores and SoCs, while exploring verification methodologies, microarchitecture, and performance-driven design.

Education

2023 - 2027 Electronics and Communication Engineering at **PES University**
2022 Class 12th at **Vydehi School of Excellence**

Projects

Specula GitHub
Designed a lightweight out-of-order RV32I core in Bluespec Verilog with register renaming, reservation stations, and ROB-based commit.

Aetheron GitHub
Implemented a RISC-V SoC with TileLink-lite interconnect and peripherals including UART, GPIO, and timers using Bluespec.

Resona GitHub
Developed a RISC-V DSP simulator in Rust with cycle-accurate support for the 'P' extension (saturating arithmetic, dot products).

RTOSsseract GitHub
Ported a basic RTOS to Xilinx MicroBlaze on Arty A7-35T with task scheduling, timer interrupts, and UART-based I/O in C.

Chipocalypse GitHub
Built a CHIP-8 emulator in Verilog with a custom CPU core, opcode decoder, display module, and keyboard input handling.

RISCape GitHub
Implemented a 5-stage pipelined RISC-V CPU in SystemVerilog with full hazard detection, stalling, and forwarding logic.

Experience

Silicon Club, PES University — Club Head Aug 2025 – Present
Led hardware-focused club initiatives and guided peers on digital design projects. Organized hands-on workshops and supported student teams in competitions.

HSP, PES University — Mentor Jul 2025 – Aug 2025
Mentored students through building CHIP-8 emulators — a project I previously developed in Verilog. Guided architecture design, reviewed HDL, and helped debug CPU/display modules.

Skills

Languages	SystemVerilog, Verilog, Bluespec, Rust, C, Python, Assembly
Tools & Platforms	Vivado, GTKWave, Vitis IDE, Verilator, ModelSim, Git, VS Code, Neovim, Linux
Domains	Digital Design, Computer Architecture, Embedded Systems, SoC Design, RTL Simulation and Synthesis
Communication	LaTeX, Blogging, Documentation