

TOP 100 VLSI FRONT END INTERVIEW QUESTIONS

(Categorized by Beginner, Intermediate, and Advanced Levels)

Interview Questions

(Level-Wise | Powered by Chipshala)

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Beginner Level Questions

- 1. What is a sensitivity list? Why is (*) used?
- 2. What is the difference between casex, casez, and case?
- 3. What is the difference between combinational and sequential logic?
- 4. What is a metastability condition?
- 5. What are synthesizable and non-synthesizable constructs?
- 6. How do you infer a latch in Verilog?
- 7. What is FSM? Types of FSMs?
- 8. Difference between initial and always blocks?
- 9. How do you write a parameterized module in Verilog?
- 10. What are synthesizable loops in RTL design?
- 11. Explain how to implement a priority encoder.
- 12. Difference between always_comb, always_ff, and always_latch in SystemVerilog?
- 13. What is the difference between posedge clk and posedge clk or posedge reset?
- 14. What is the difference between blocking and non-blocking assignments in Verilog?
- 15. What are the different types of delays in Verilog?

- 16. What is a race condition?
- 17. What is the difference between wire and reg?
- 18. What is a setup and hold violation?
- 19. What is clock gating?
- 20. What is the role of a sensitivity list in simulation?

Intermediate Level Questions

- 1. What is the use of a test vector?
- 2. What are asynchronous and synchronous resets?
- 3. How do you detect if a signal is glitching?
- 4. How do you avoid race conditions in testbenches?
- 5. What is RTL simulation vs. synthesis?
- 6. What is the default state of a signal in simulation?
- 7. What is register packing and duplication?
- 8. What is inferred vs instantiated hardware?
- 9. Difference between assign and always blocks?
- 10. How do you optimize area in RTL design?
- 11. What are don't care conditions in synthesis?
- 12. What is meant by fan-out?
- 13. How do you avoid combinational loops in RTL?
- 14. How do you use generate blocks in Verilog/SystemVerilog?
- 15. What are the three blocks in FSM design?
- 16. What is a latch and how is it different from a flip-flop?
- 17. What is the role of generate block in Verilog?
- 18. What is event-driven simulation?
- 19. How is a counter implemented in Verilog?
- 20. How is FSM livelock diagnosed?

- 21. What is the issue with latch inference in RTL?
- 22. Explain one-hot encoding and when it's used.
- 23. What is zero-delay modeling?
- 24. How do you implement a pipeline in RTL design?
- 25. What is a glitch and how do you avoid it?
- 26. What is meant by over-constraining vs. under-constraining?
- 27. What are functional vs code coverage?
- 28. What is Moore vs Mealy FSM difference?
- 29. How do you handle assign vs force in simulation?
- 30. What is false path and multicycle path in timing?
- 31. What is combinational feedback and why is it bad?
- 32. What is reset deassertion glitch and how is it fixed?
- 33. Difference between posedge clk and @clk?
- 34. What is the default value of uninitialized signals in sim?
- 35. What is the difference between edge-sensitive and level-sensitive devices?
- 36. How do you write a priority encoder in Verilog?
- 37. What is an implicit vs explicit FSM?
- 38. What is the purpose of unique case in SystemVerilog?
- 39. What is a synthesis warning vs error?
- 40. How to detect and fix race conditions using <=?

Advanced Level Questions

- 1. What is CDC reconvergence and why is it dangerous?
- 2. What is datapath/control decoupling and why is it used?
- 3. What is toggle rate and how does it impact power?
- 4. What are power-aware verification techniques at RTL?
- 5. What is FSM state encoding corruption and how is it debugged?

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- 6. What causes FSM livelock and how to fix it?
- 7. How to handle async FIFO full/empty logic?
- 8. What is RTL clock gating and how is it implemented?
- 9. What is a sticky bit and where is it used?
- 10. What is scan FF and its role in design for test?
- 11. What is glitch-free muxing in clock domain switching?
- 12. What is clock-domain pessimism in STA?
- 13. How to design glitch-free combinational logic?
- 14. What is RTL code coverage?
- 15. How do you design a reconfigurable FSM?
- 16. What is the significance of setup/hold margins in CDC?
- 17. What are stuck-at faults in simulation?
- 18. How is a testbench structured for RTL simulation?
- 19. How to detect and fix redundant logic in RTL?
- 20. What is RTL power estimation and how is it done?
- 21. How do you transfer data between two async clock domains safely?
- 22. What is a retiming technique in synthesis?
- 23. What is multicycle path constraint and when is it used?
- 24. What is glitch power and how do you reduce it?
- 25. What is a coverage hole and how do you detect/fix it?
- 26. Why should inferred latches be avoided in synthesis?
- 27. What is the role of input/output buffering in RTL design?
- 28. What is ready/valid protocol in SoC buses?
- 29. What are the risks of metastability and how is it handled?
- 30. What is the purpose of cover assertions?
- 31. How to minimize logic duplication in RTL?
- 32. What is RTL-level area optimization technique?
- 33. What is functional reset coverage?

34. What is clock gating's impact on sim and synthesis? 35. How do you check clock skew issues in RTL code? 36. What is false path and how does it affect timing closure? 37. What is assertion-based verification and why is it better? 38. Difference between immediate vs concurrent assertions? 39. How do you handle race conditions in non-blocking assignments? 40. What is handshake-based pulse synchronization in CDC?

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