VLSI TO YOU YOUTUBE CHANNEL

INTERVIEW QUESTIONS IN SYSTEM VERILOG

1. What is the difference between an initial and final block of the **systemverilog**?
2. Explain the simulation phases of **SystemVerilog verification**?
3. What is the Difference between SystemVerilog packed and unpacked array?
4. What is “This ” keyword in the systemverilog?
5. randomized in the systemverilog test bench?
6. in SystemVerilog which array type is preferred for memory declaration and why?
7. How to avoid race round condition between DUT and test bench in SystemVerilog verification?
8. What are the advantages of the systemverilog program block?
9. What is the difference between logic and bit in SystemVerilog?
10. What is the difference between datatype logic and wire?
11. What is a virtual interface?
12. What is an abstract class?
13. What is the difference between $random and $urandom?
14. What is the expect statements in assertions?
15. What is the difference between == and === ?

16. What are the system tasks?
17. What is SystemVerilog assertion binding and advantages of it?
18. What are parameterized classes?
19. How to generate array without randomization?
20. Explain the difference between **deep copy** and **shallow copy**?
21. What is interface and advantages over the normal way?
22. What is modport and explain the usage of it?
23. What is a clocking block?
24. What is the difference between the clocking block and modport?
25. What are the basic testbench components?
26. What is the difference between a $rose and @ (posedge)?
27. What is the use of extern?
28. What is scope randomization?
29. What is the difference between blocking and non-blocking assignments?
30. What are automatic variables?
31. What is the scope of local and private variables?
32. How to check if any bit of the expression is X or Z?
33. What is the Difference between param and typedef?
34. What is `timescale?
35. Explain the difference between new( ) and new[ ] ?
36. What is the difference between task and function in class and Module?
37. Why always blocks are not allowed in the program block?

38. Why forever is used instead of always in program block?

39. What is SVA?

40. Explain the difference between fork-join, fork-join_none, and fork- join_any?

41. What is the difference between mailboxes and queues?

42. What is casting?

43. What is inheritance and polymorphism?

44. What is callback?

45. What is constraint solve-before?

46. What is coverage and what are different types?

47. What is the importance of coverage in SystemVerilog verification?

48. When you will say that verification is completed?

49. What are illegal bins? Is it good to use it and why?

50. What is “super “?

51. What is the input skew and output skew in the clocking block?

52. What is a static variable?

53. What is a package?

54. What is the difference between bit [7:0] and byte?

55. What is randomization

56. What are the constraints? Is all constraints are bidirectional?

57. What are in line constraints?

58. What is the difference between rand and randc?

59. Explain pass by value and pass by ref?

60. What are the advantages of cross-coverage?

61. What is the difference between associative and dynamic array?

62. What is the type of SystemVerilog assertions?

63. What is the difference between $display,$strobe,$ monitor?

64. Can we write SystemVerilog assertions in class?

65. What is an argument pass by value and pass by reference?