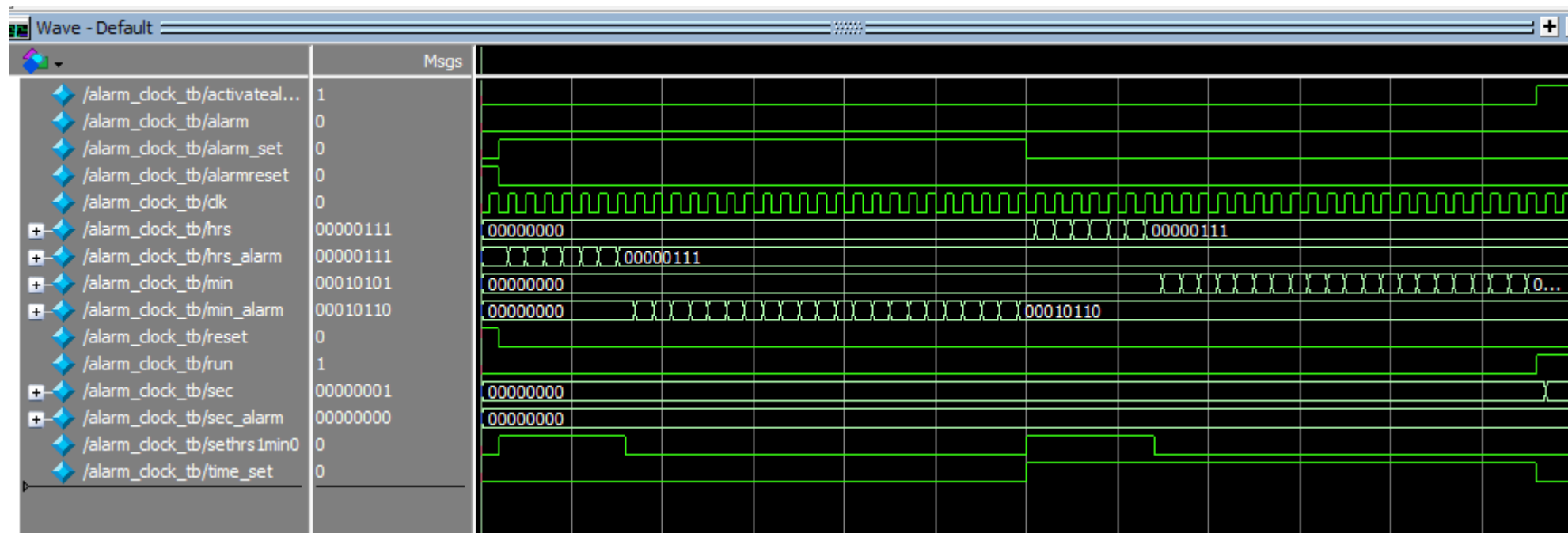


Lab 4

Pranav Nadimpalli

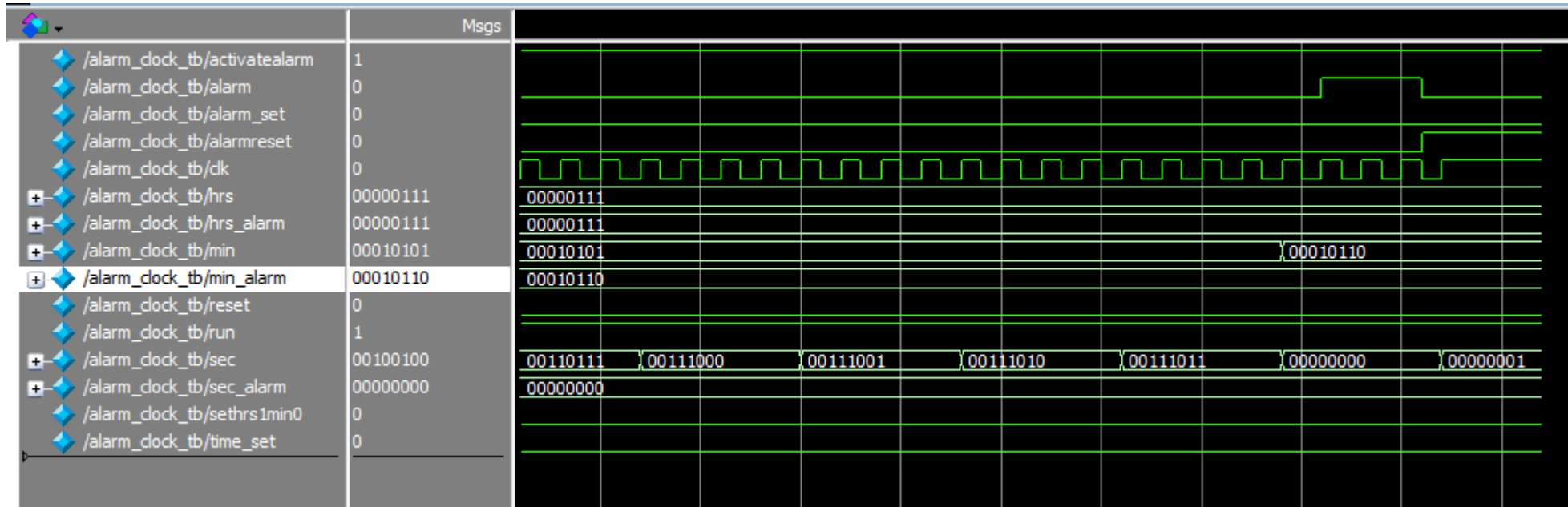
Simulated Alarm Clock pt. 1

- Setting the time. Hours and minutes for alarm set to 7:22:00 while clock is set to 7:21



Simulate Alarm Clock Pt. 2

- Running clock till alarm once times match the alarm is set then reset when reset is high. I am only showing the last portion for ease to read.



Flow Summary

Compilation Report - alarm_clock_pv

Table of Contents

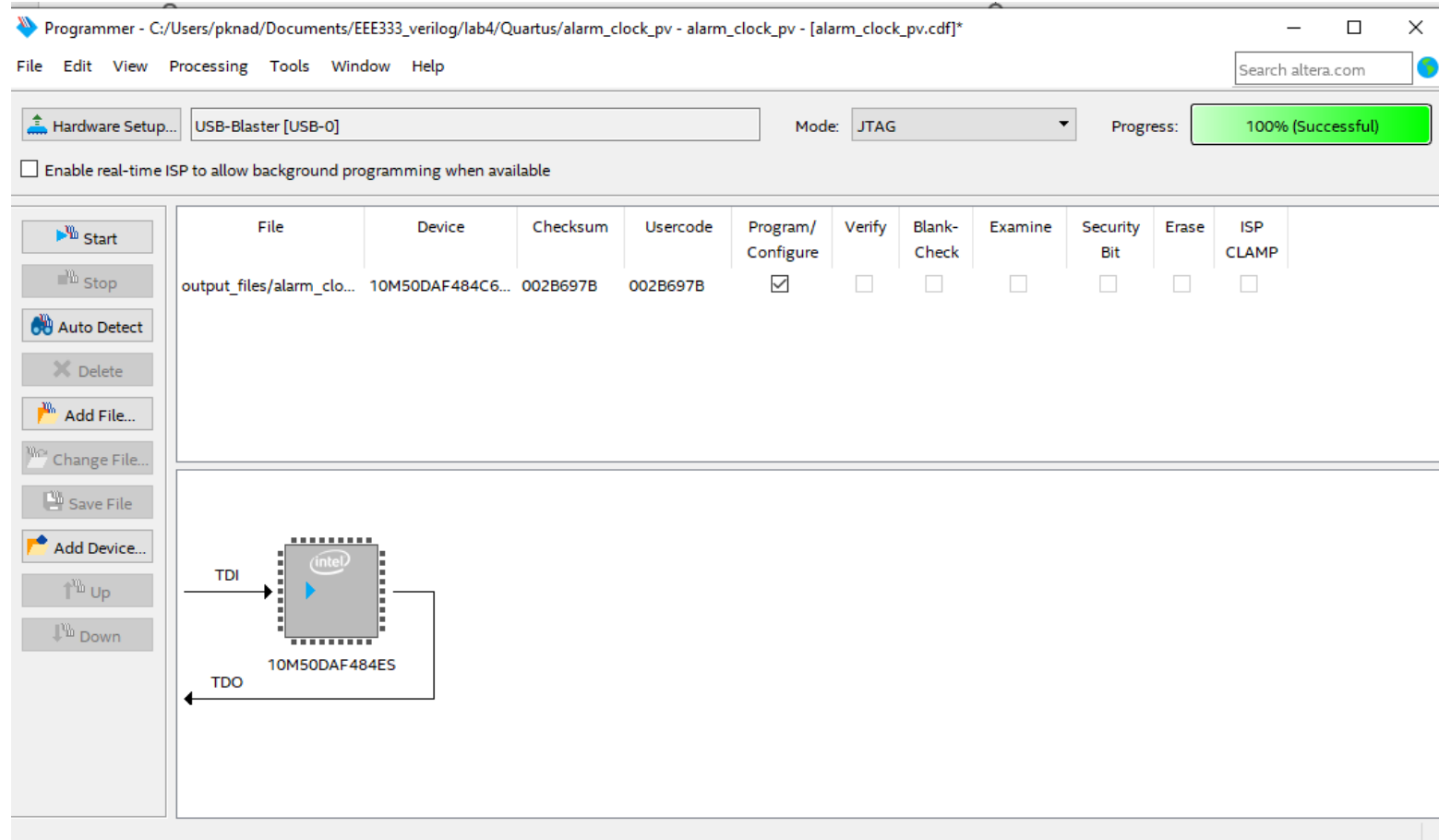
- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Flow Messages
- Flow Suppressed Messages
- Assembler
- Timing Analyzer

Flow Summary

<<Filter>>

Flow Status	Successful - Sun Mar 24 22:20:28 2024
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	alarm_clock_pv
Top-level Entity Name	alarm_clock_pv
Family	MAX 10
Device	10M50DAF484C6GES
Timing Models	Preliminary
Total logic elements	486 / 49,760 (< 1 %)
Total registers	80
Total pins	58 / 360 (16 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

Programmed



Pin assignment

Pin Planner - C:/Users/pknad/Documents/EEE333_verilog/lab4/Quartus/alarm_clock_pv - alarm_clock_pv

File Edit View Processing Tools Window Help

Report not available

Groups Report

Tasks

Early Pin Planning

Early Pin Planning...

Top View - Wire Bond
MAX 10 - 10M60DAF48C6GES

Pin Legend

Symbol Pin Type

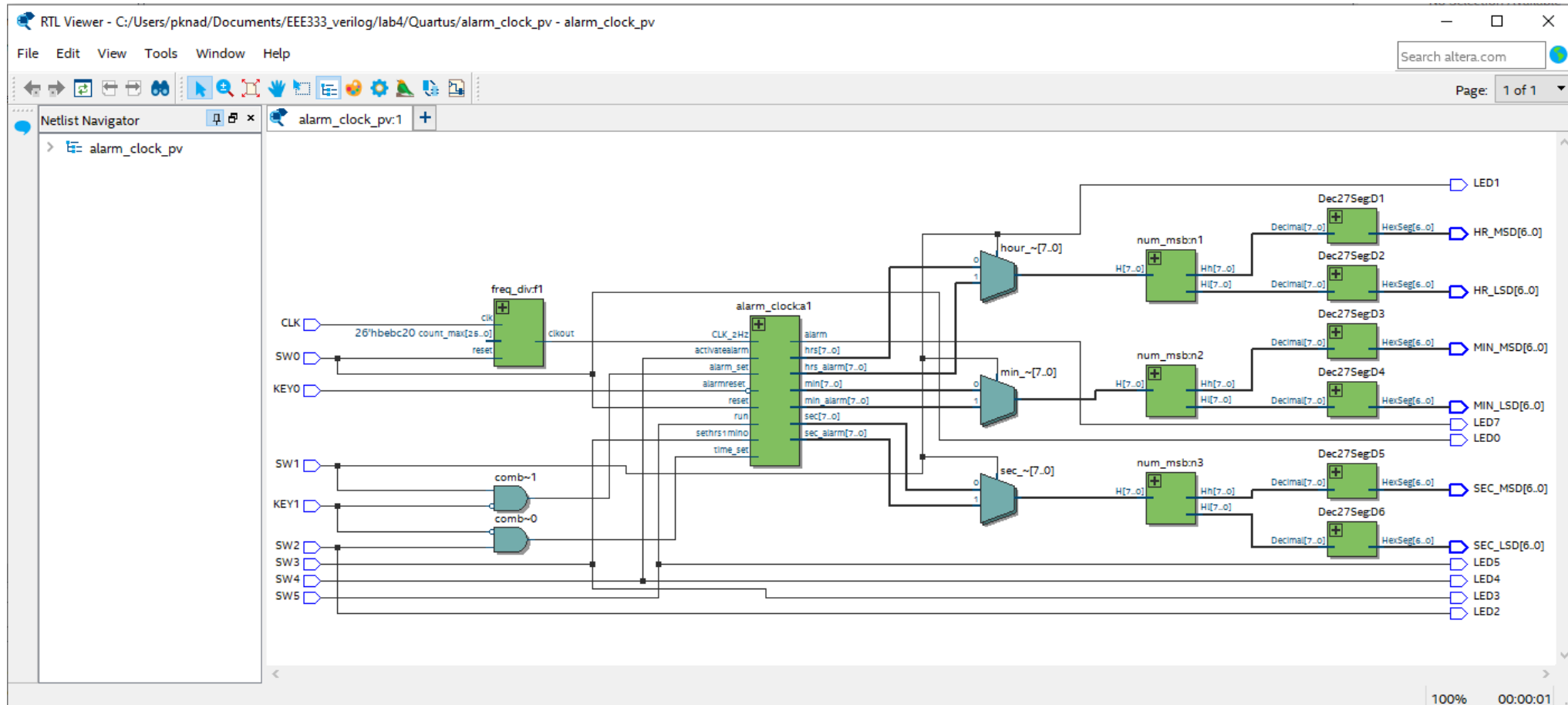
- User I/O
- User assigned I...
- Fitter assigned I...
- Unbonded pad
- Reserved pin
- Other configura...
- DEV_OE
- DEV_CLR

Filter: Pins: all

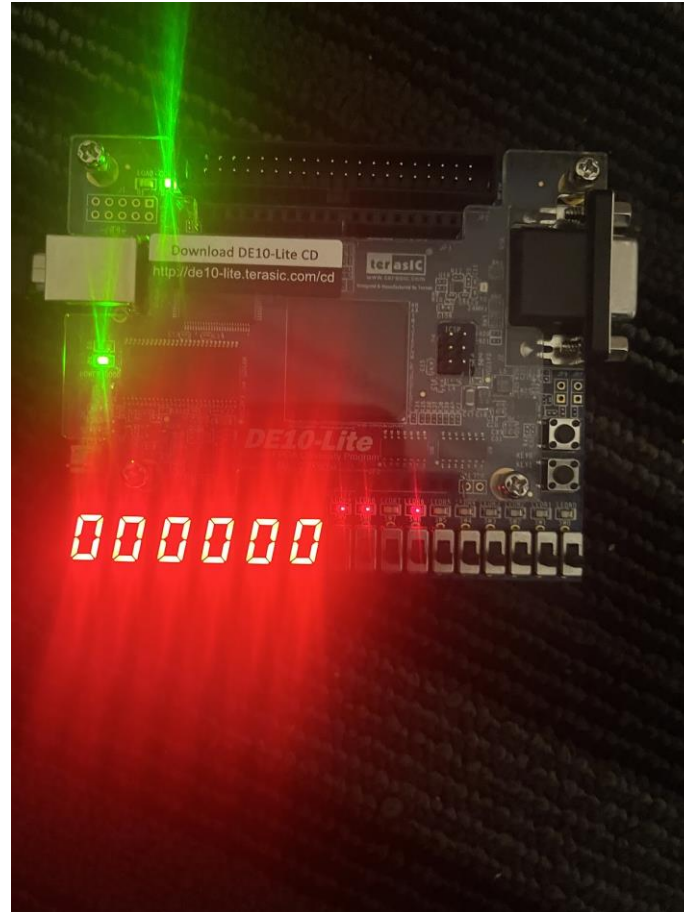
Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	Strict Preservation
CLK	Input	PIN_P11	3	B3_NO	PIN_P11	2.5 V		12mA (default)			
HR_LSD[6]	Output	PIN_F20	6	B6_NO	PIN_F20	2.5 V		12mA (default)	2 (default)		
HR_LSD[5]	Output	PIN_F19	6	B6_NO	PIN_F19	2.5 V		12mA (default)	2 (default)		
HR_LSD[4]	Output	PIN_H19	6	B6_NO	PIN_H19	2.5 V		12mA (default)	2 (default)		
HR_LSD[3]	Output	PIN_J18	6	B6_NO	PIN_J18	2.5 V		12mA (default)	2 (default)		
HR_LSD[2]	Output	PIN_E19	6	B6_NO	PIN_E19	2.5 V		12mA (default)	2 (default)		
HR_LSD[1]	Output	PIN_E20	6	B6_NO	PIN_E20	2.5 V		12mA (default)	2 (default)		
HR_LSD[0]	Output	PIN_F18	6	B6_NO	PIN_F18	2.5 V		12mA (default)	2 (default)		
HR_MSD[6]	Output	PIN_N20	6	B6_NO	PIN_N20	2.5 V		12mA (default)	2 (default)		
HR_MSD[5]	Output	PIN_N19	6	B6_NO	PIN_N19	2.5 V		12mA (default)	2 (default)		
HR_MSD[4]	Output	PIN_M20	6	B6_NO	PIN_M20	2.5 V		12mA (default)	2 (default)		
HR_MSD[3]	Output	PIN_N18	6	B6_NO	PIN_N18	2.5 V		12mA (default)	2 (default)		
HR_MSD[2]	Output	PIN_L18	6	B6_NO	PIN_L18	2.5 V		12mA (default)	2 (default)		
HR_MSD[1]	Output	PIN_K20	6	B6_NO	PIN_K20	2.5 V		12mA (default)	2 (default)		
HR_MSD[0]	Output	PIN_J20	6	B6_NO	PIN_J20	2.5 V		12mA (default)	2 (default)		
KEY0	Input	PIN_B8	7	B7_NO	PIN_B8	2.5 V		12mA (default)			
KEY1	Input	PIN_A7	7	B7_NO	PIN_A7	2.5 V		12mA (default)			
LED0	Output	PIN_A8	7	B7_NO	PIN_A8	2.5 V		12mA (default)	2 (default)		
LED1	Output	PIN_A9	7	B7_NO	PIN_A9	2.5 V		12mA (default)	2 (default)		
LED2	Output	PIN_A10	7	B7_NO	PIN_A10	2.5 V		12mA (default)	2 (default)		
LED3	Output	PIN_B10	7	B7_NO	PIN_B10	2.5 V		12mA (default)	2 (default)		
LED4	Output	PIN_D13	7	B7_NO	PIN_D13	2.5 V		12mA (default)	2 (default)		
LED5	Output	PIN_C13	7	B7_NO	PIN_C13	2.5 V		12mA (default)	2 (default)		
LED7	Output	PIN_D14	7	B7_NO	PIN_D14	2.5 V		12mA (default)	2 (default)		
MIN_LSD[6]	Output	PIN_B22	6	B6_NO	PIN_B22	2.5 V		12mA (default)	2 (default)		
MIN_LSD[5]	Output	PIN_C22	6	B6_NO	PIN_C22	2.5 V		12mA (default)	2 (default)		
MIN_LSD[4]	Output	PIN_B21	6	B6_NO	PIN_B21	2.5 V		12mA (default)	2 (default)		
MIN_LSD[3]	Output	PIN_A21	6	B6_NO	PIN_A21	2.5 V		12mA (default)	2 (default)		
MIN_LSD[2]	Output	PIN_B19	7	B7_NO	PIN_B19	2.5 V		12mA (default)	2 (default)		
MIN_LSD[1]	Output	PIN_A20	7	B7_NO	PIN_A20	2.5 V		12mA (default)	2 (default)		
MIN_LSD[0]	Output	PIN_B20	6	B6_NO	PIN_B20	2.5 V		12mA (default)	2 (default)		
MIN_MSD[6]	Output	PIN_E17	6	B6_NO	PIN_E17	2.5 V		12mA (default)	2 (default)		
MIN_MSD[5]	Output	PIN_D19	6	B6_NO	PIN_D19	2.5 V		12mA (default)	2 (default)		
MIN_MSD[4]	Output	PIN_C20	6	B6_NO	PIN_C20	2.5 V		12mA (default)	2 (default)		
MIN_MSD[3]	Output	PIN_C19	7	B7_NO	PIN_C19	2.5 V		12mA (default)	2 (default)		

0% 00:00:00

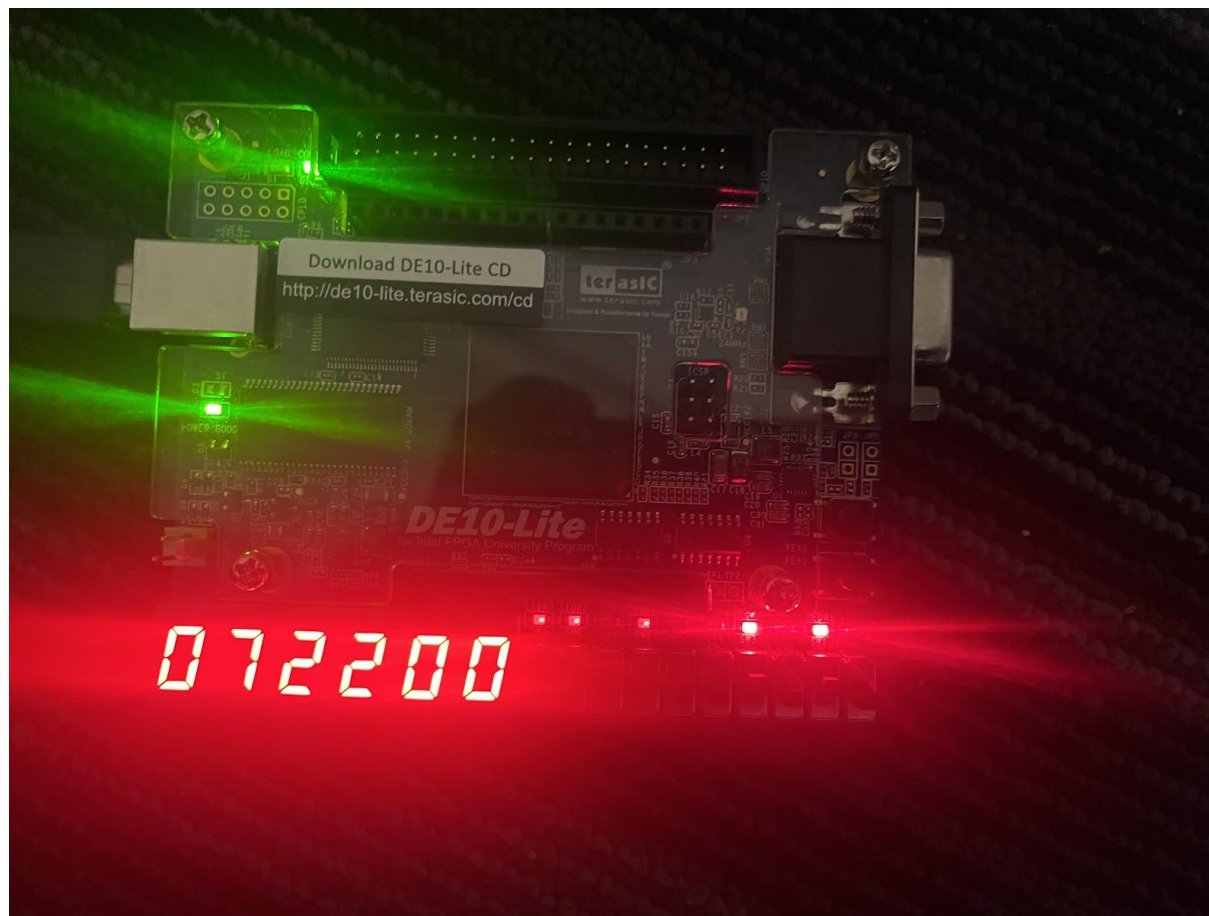
Net List viewer



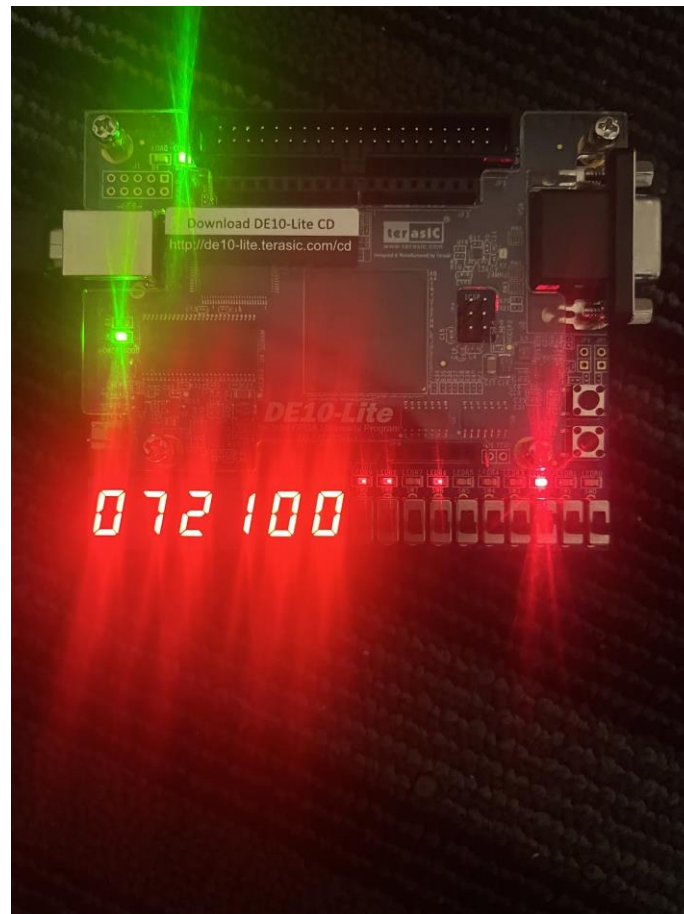
Clk & alarm reset



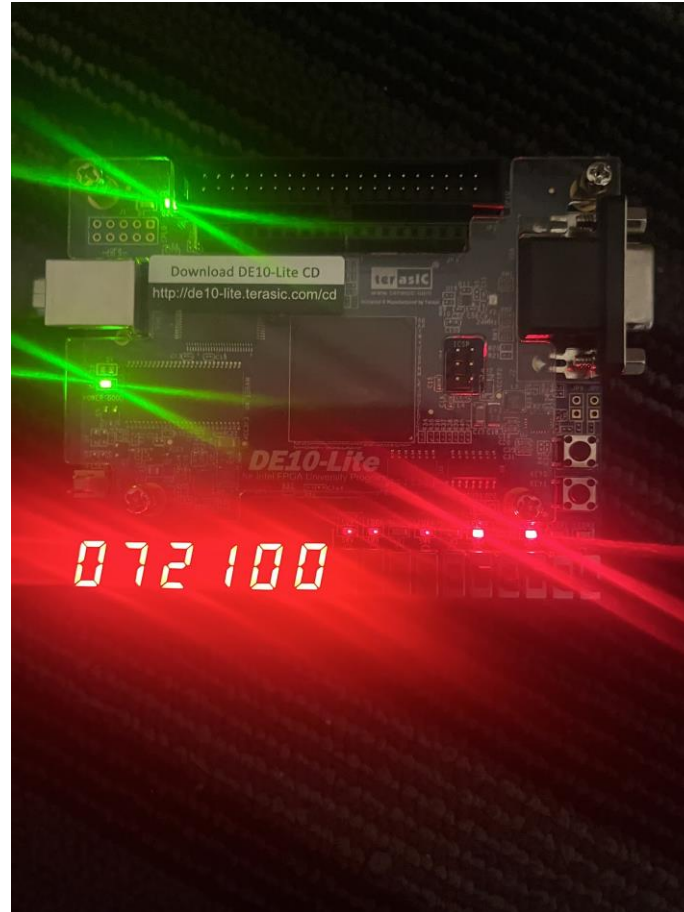
Set alarm to 7: 22



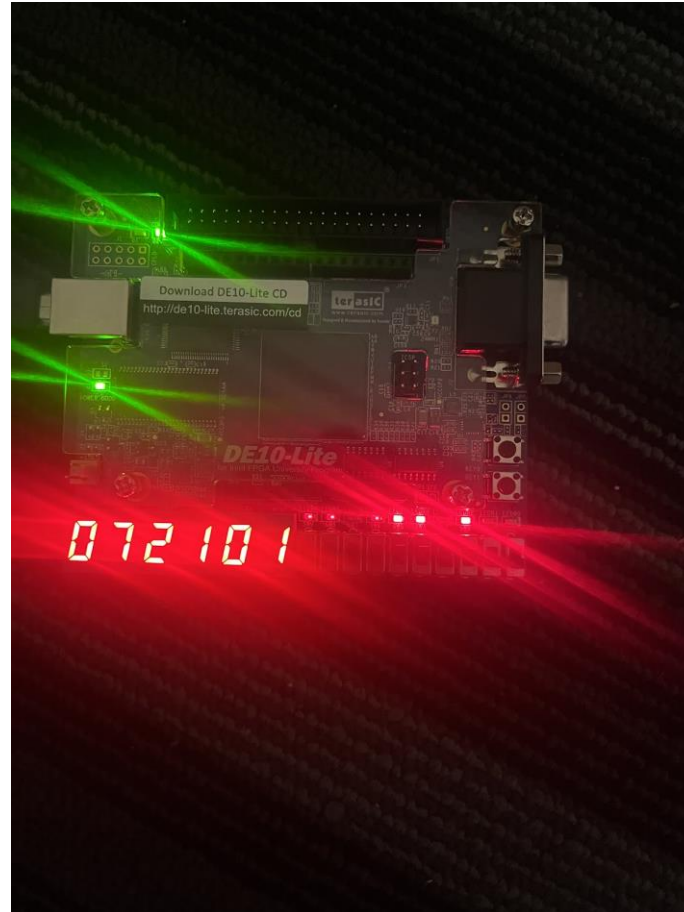
Set clock to 7:21



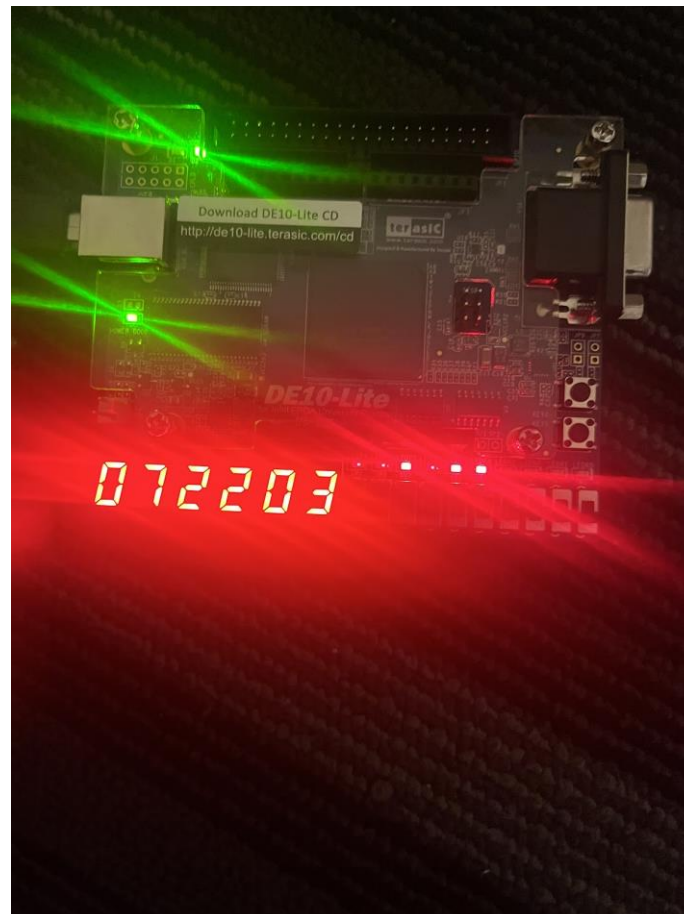
Active alarm



Run timer



Alarm went off



Alarm reset

