

Lab 2

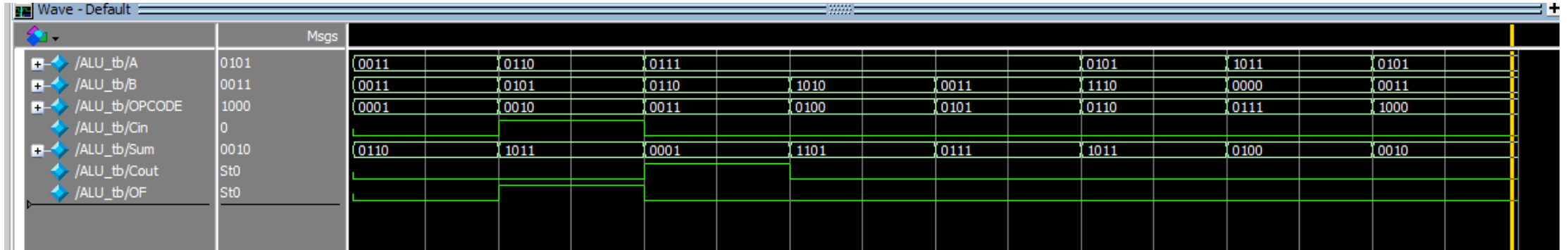
Pranav Nadimpalli

ALU Test Bench 1-8

Operation	Aluin_a	Aluin_b	Cin	Alu_out	Cout	OF
Add	0011	0011	0	0110	0	0
Add with Cin	0110	0101	1	1011	0	1
Sub b from a	0111	0110	0	0001	1	0
Bitwise NAND	0111	1010	0	1101	0	0
Bitwise OR	0111	0011	0	0111	0	0
Bitwise XOR	0101	1110	0	1011	0	0
Bitwise NOT	1011	0000	0	0100	0	0
Logical right shift	0101	0000	0	0010	0	0

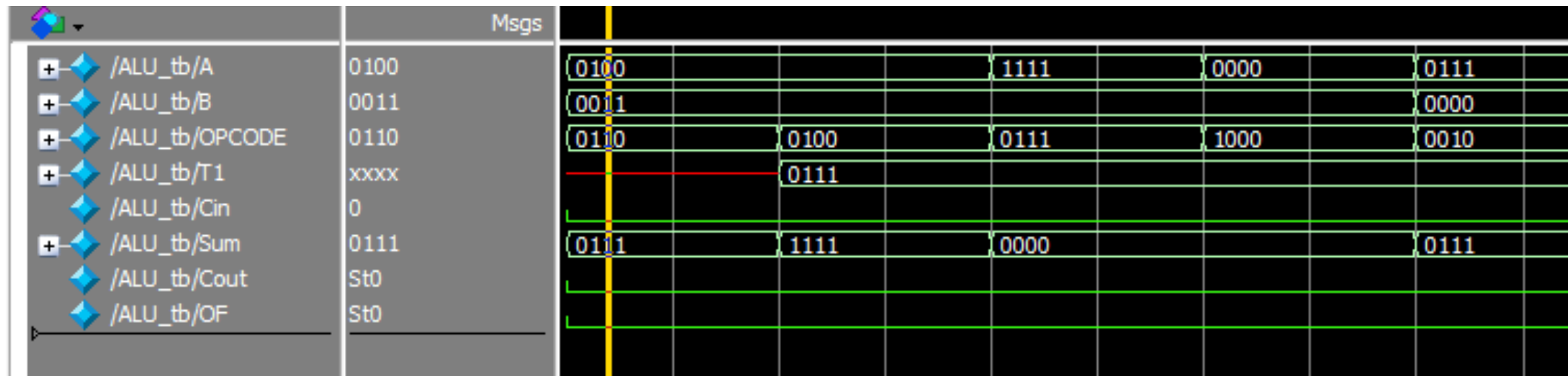
ALU Test Bench Waveforms (1-8)

- All Waves in Order of Table Operations



ALU Test Bench 9 + Waves (Series of operations to Get to Final Output)

Operation	Aluin_a	Aluin_b	Cin	Result	Carry Out	Overflow
(a^b) + ((a&b)>>1)	0100	0011	0	0111	0	0



Board Programming

Programmer - C:/Users/pknad/Documents/EEE333_verilog/lab2/quartus/al_u_pv/ALU_pv - ALU_pv - [ALU_pv.cdf]

File Edit View Processing Tools Window Help

Hardware Setup... USB-Blaster [USB-0] Mode: JTAG Progress: 100% (Successful)

☐ Enable real-time ISP to allow background programming when available

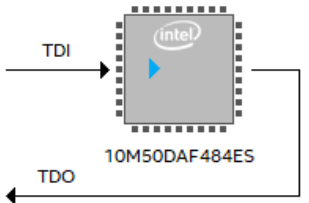
File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP
output_files/ALU_pv.sof	10M50DAF484C6...	00273DBE	00273DBE	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Start Stop Auto Detect Delete Add File... Change File... Save File Add Device... Up Down

TDI

10M50DAF484ES

TDO



Pin Assignment

Pin Planner - C:/Users/pknad/Documents/EEE333_verilog/lab2/quartus/alu_pv/ALU_pv - ALU_pv

File Edit View Processing Tools Window Help

Search altera.com

Report

Report not available

Groups Report

Tasks

- Early Pin Planning
 - Early Pin Planning...
 - Run I/O Assignment Analysis
 - Export Pin Assignments...

Top View - Wire Bond
MAX 10 - 10M50DAF484C6GES

Pin Legend

Symbol	Pin Type
○	User I/O
●	User assigned I...
●	Fitter assigned I...
○	Unbonded pad
○	Reserved pin
○	Other configura...
○	DEV_OE
○	DEV_CLR
○	DIFF_n
○	DIFF_p
○	DQ
○	DQS
○	DQS#

Named: * Edit: < >

Filter: Pins: all

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Cu
OF	Output	PIN_D14	7	B7_NO	PIN_D14	2.5 V	Reserved	12r
OPCODE[3]	Input	PIN_B14	7	B7_NO	PIN_B14	2.5 V		12r
OPCODE[2]	Input	PIN_A14	7	B7_NO	PIN_A14	2.5 V		12r
OPCODE[1]	Input	PIN_A13	7	B7_NO	PIN_A13	2.5 V		12r
OPCODE[0]	Input	PIN_B12	7	B7_NO	PIN_B12	2.5 V		12r
alu_out[3]	Output	PIN_B10	7	B7_NO	PIN_B10	2.5 V		12r
alu_out[2]	Output	PIN_A10	7	B7_NO	PIN_A10	2.5 V		12r
alu_out[1]	Output	PIN_A9	7	B7_NO	PIN_A9	2.5 V		12r
alu_out[0]	Output	PIN_A8	7	B7_NO	PIN_A8	2.5 V		12r
aluin_a[3]	Input	PIN_A12	7	B7_NO	PIN_A12	2.5 V		12r
aluin_a[2]	Input	PIN_C12	7	B7_NO	PIN_C12	2.5 V		12r
aluin_af11	Input	PIN_D12	7	B7_NO	PIN_D12	2.5 V		12r

0% 00:00:00

Flow Summary

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Flow Summary

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> Flow Suppressed Messages

> Assembler

> Timing Analyzer

Compilation Report - ALU_pv

Flow Summary

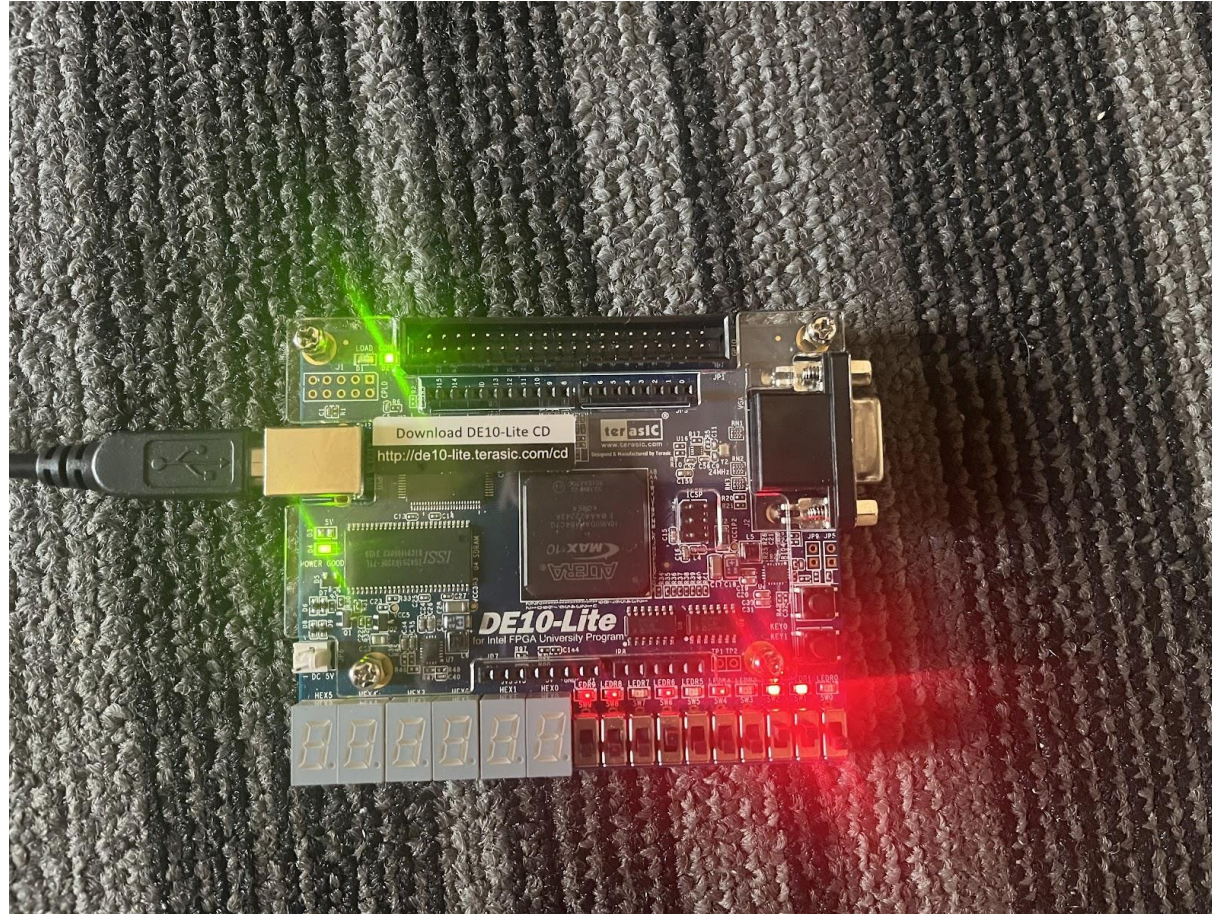
<<Filter>>

Flow Status	Successful - Sun Feb 11 16:47:14 2024
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	ALU_pv
Top-level Entity Name	ALU_pv
Family	MAX 10
Device	10M50DAF484C6GES
Timing Models	Preliminary
Total logic elements	32 / 49,760 (< 1 %)
Total registers	0
Total pins	15 / 360 (4 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

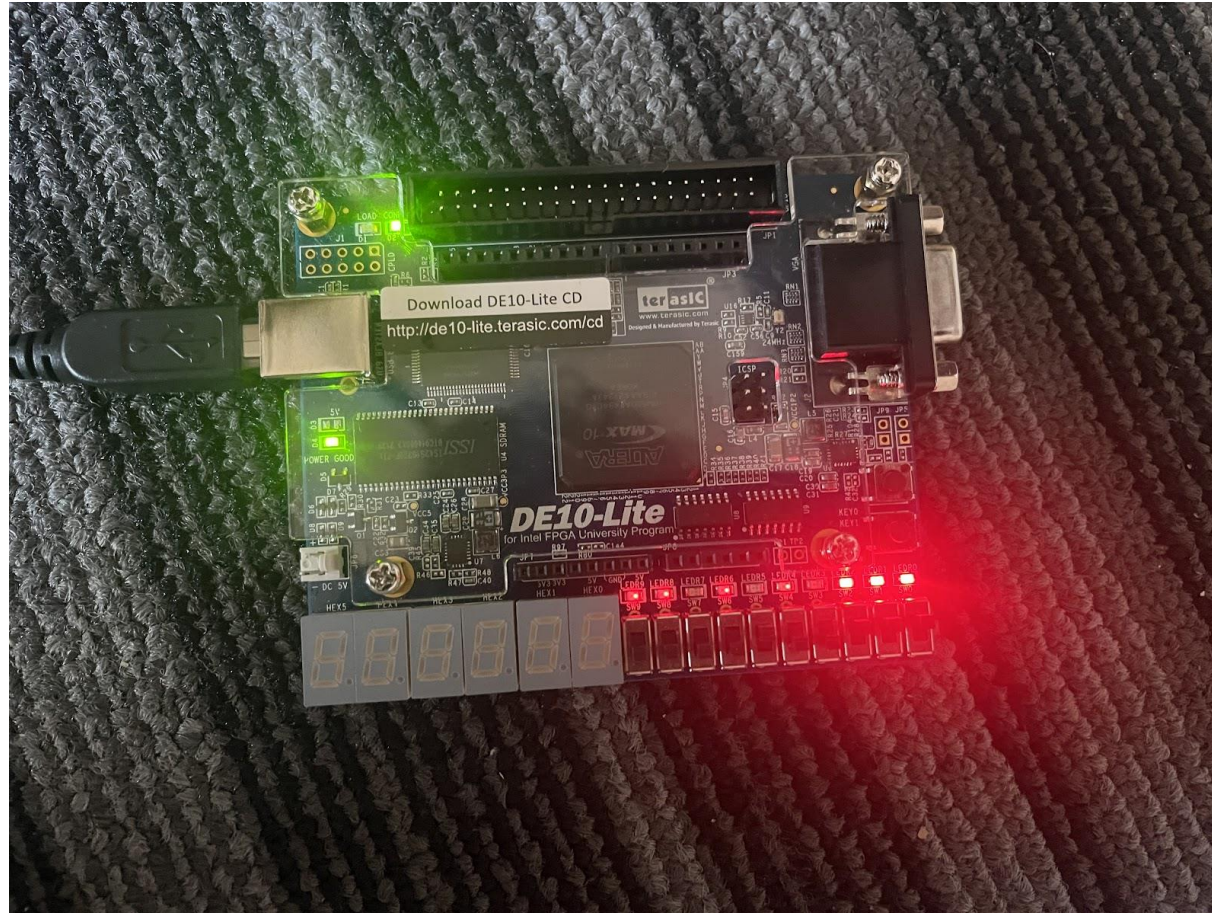
Physical Validation Table

Operation	A	B	Cin	Out	Cout	OF
Add	0011	0011	0	0110	0	0
Add with Cin	0011	0011	1	0111	0	0
Sub b from a	0111	0011	0	0100	1	0
NAND	0110	0011	0	1101	0	0
OR	0110	0011	0	0111	0	0
NOT	1111	0011	0	0000	0	0
Logical Shift Right	0101	0011	0	0010	0	0

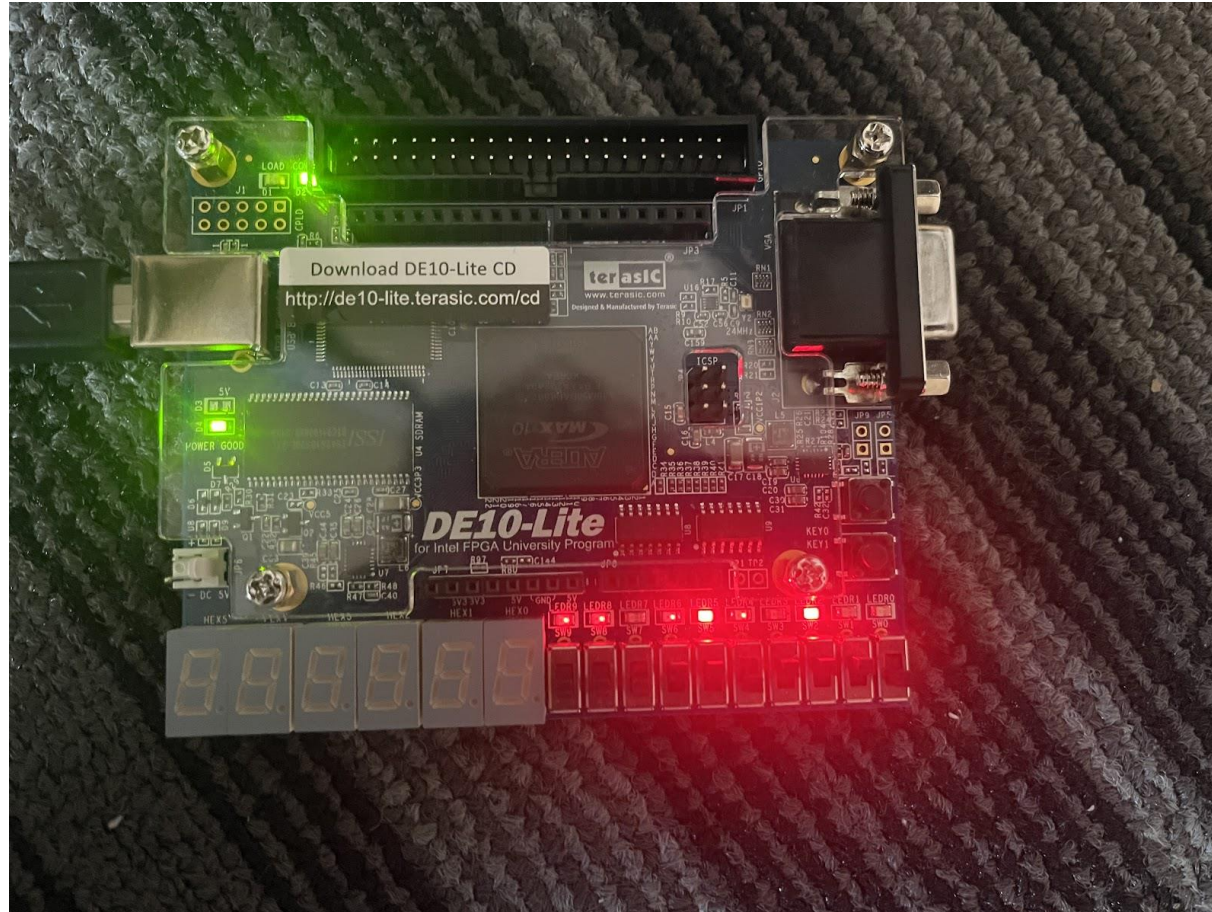
Add



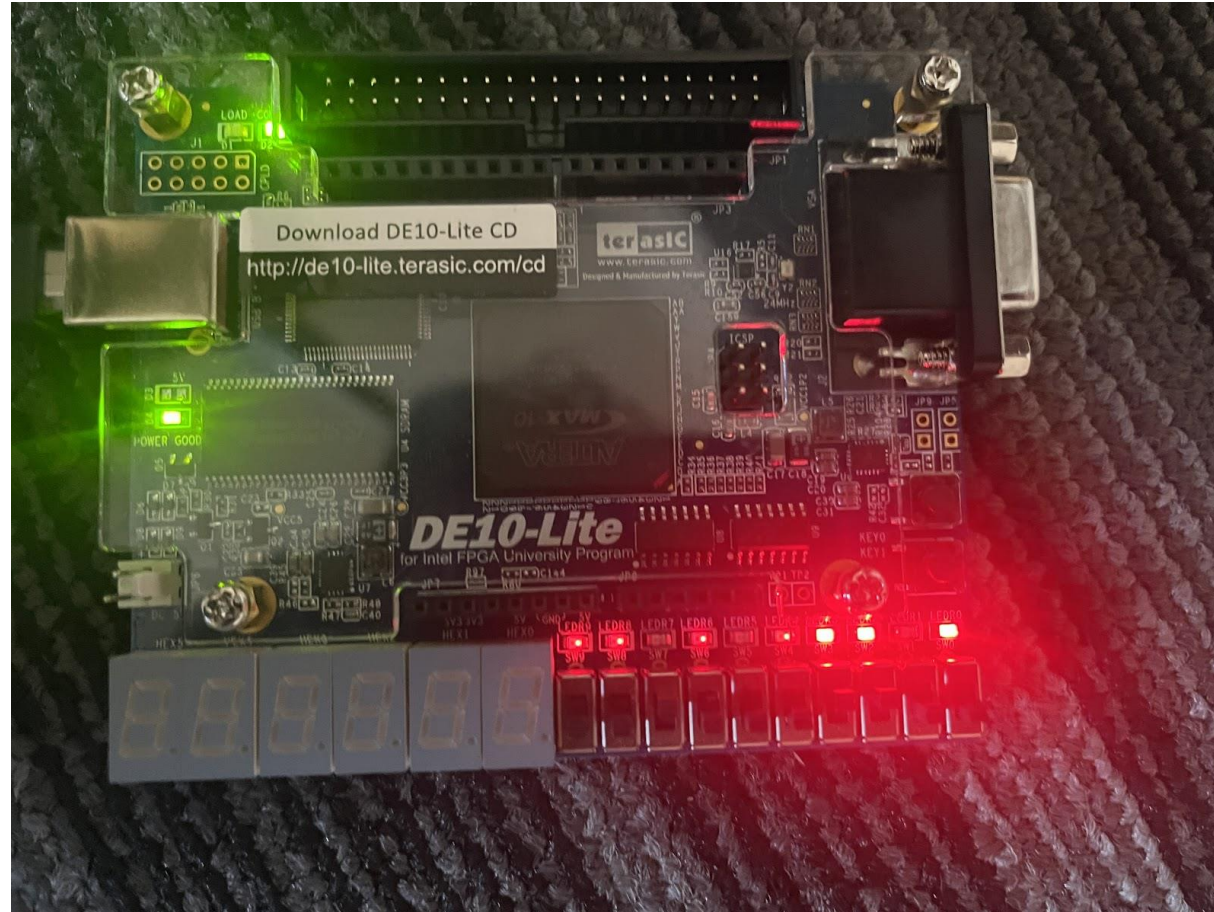
Add with Cin



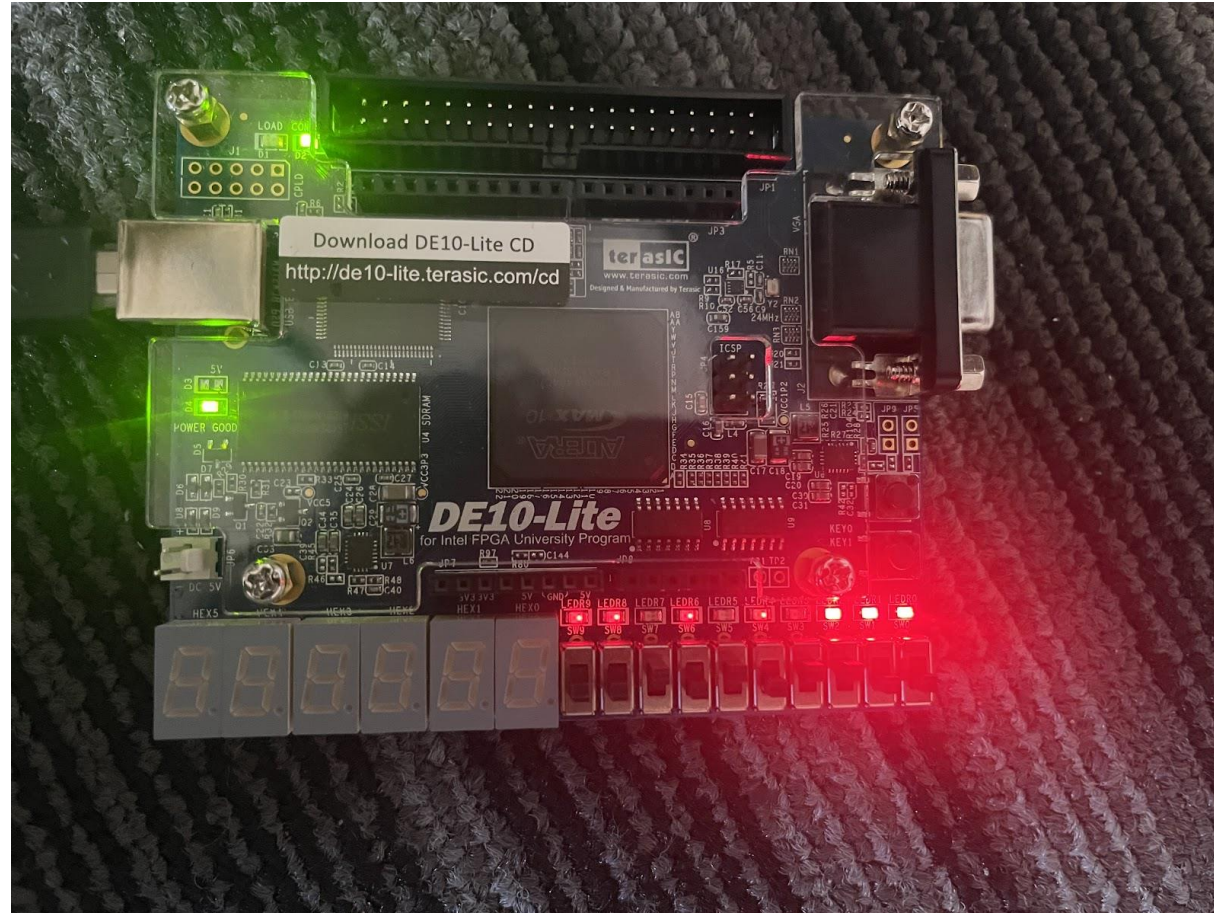
Sub B From A



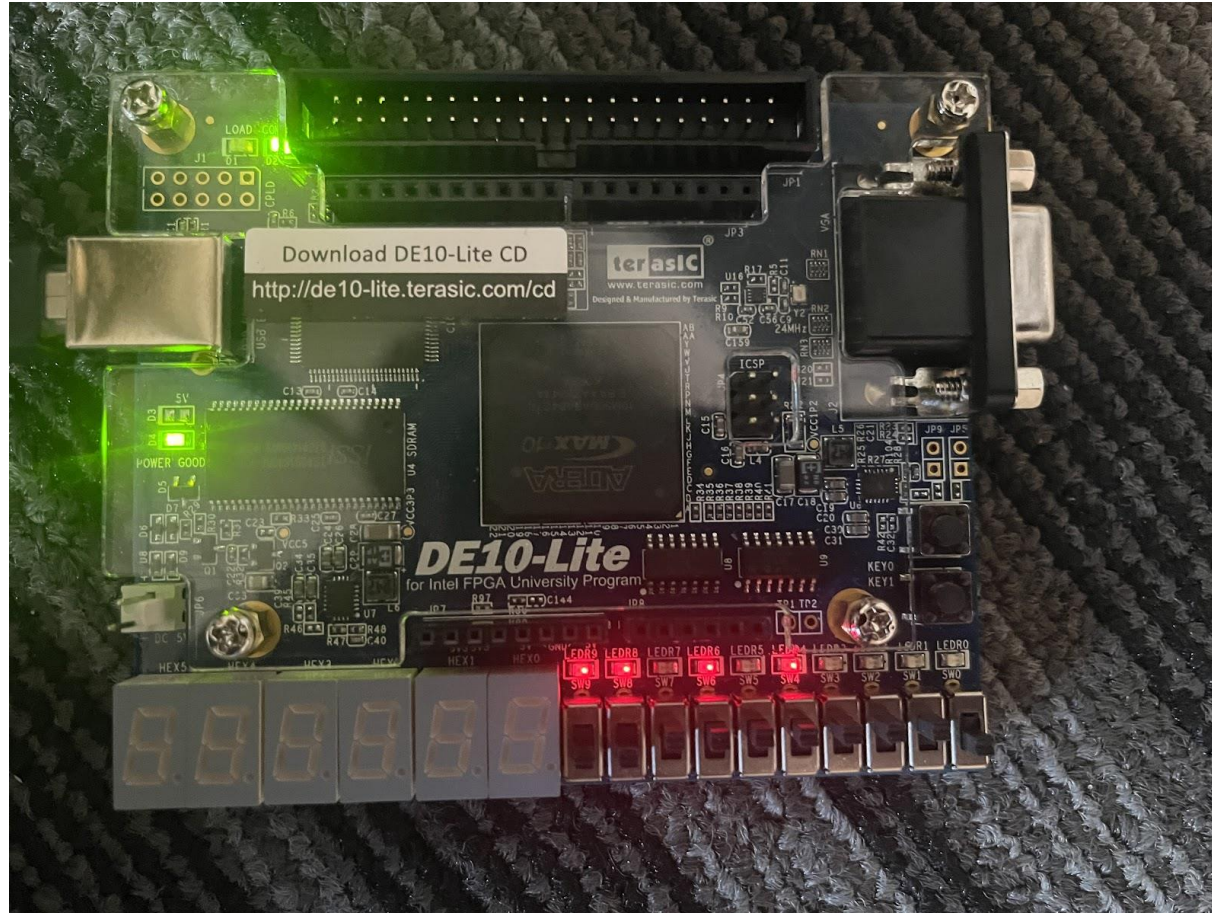
NAND



OR



NOT



Logical Shift Right

