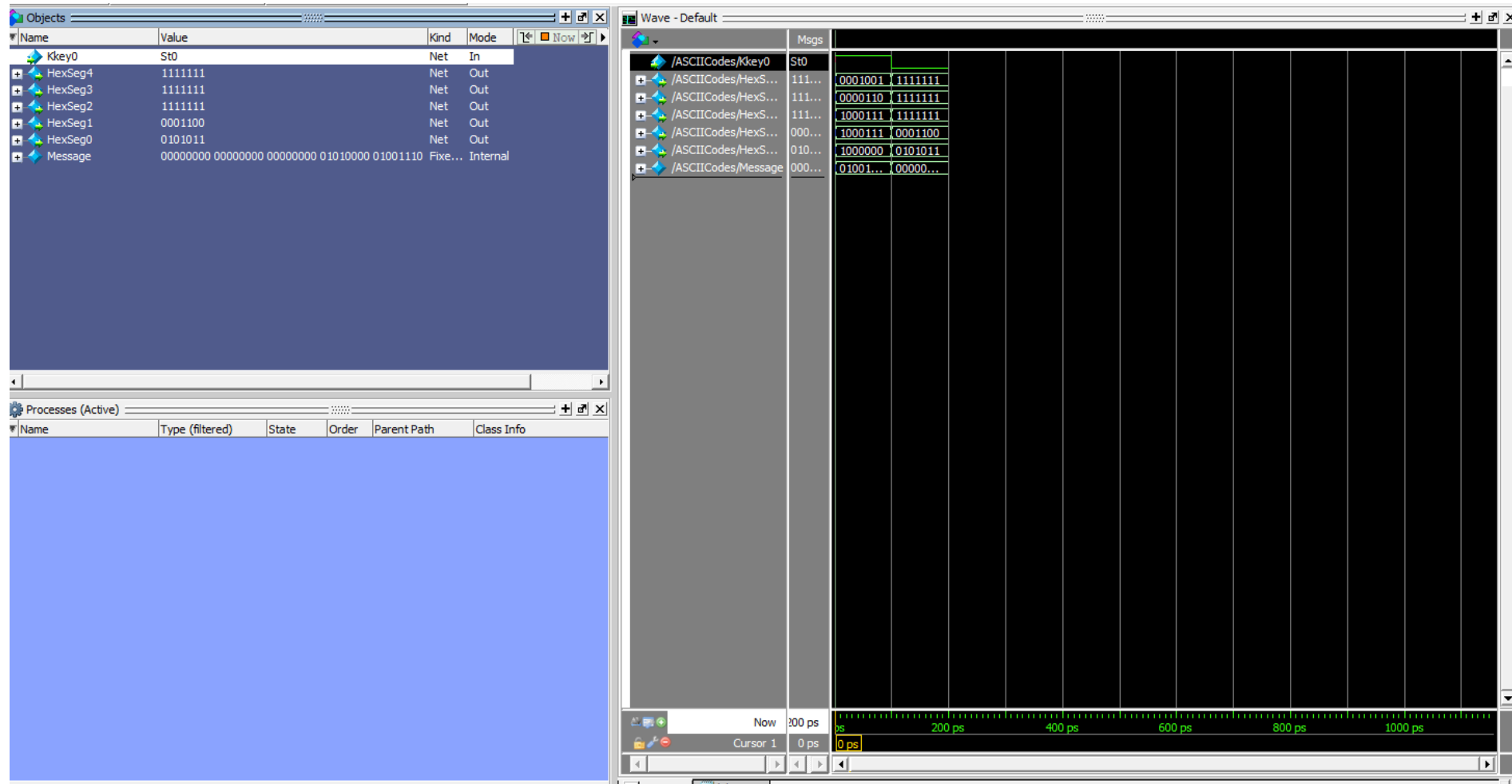


Lab 1 Supp Work

Pranav Nadimpalli

Problem 2 (Showing Kkey0 at High and Low)

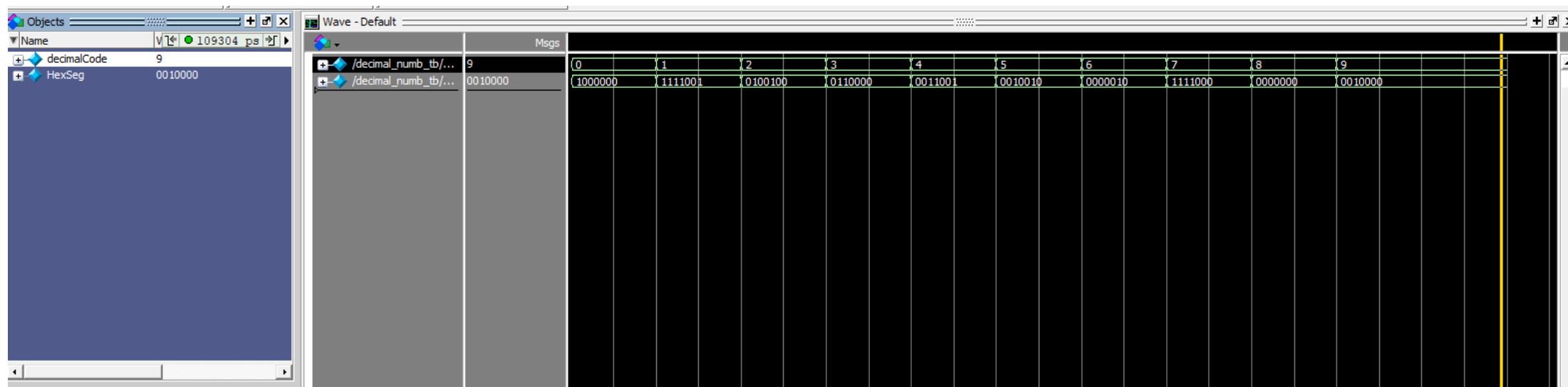


Problem 3 (Ascii27Seg Test 0-9)

The screenshot displays a logic analyzer interface with two main panels. The left panel, titled 'Objects', shows a list of variables: 'AsciiCode' with a value of 8, and 'HexSeg' with a value of 0000000. The right panel, titled 'Wave - Default', shows a waveform with two signals: '/ascii_numb_tb/Ascii...' and '/ascii_numb_tb/Hex...'. The 'Ascii...' signal has a value of 8, and the 'Hex...' signal has a value of 0000000. Below these, a table displays the binary values for the 'HexSeg' signal across 10 time slots (0 to 9). A vertical yellow line is positioned between the 8th and 9th time slots.

(0)	1	2	3	4	5	6	7	8	9
1000000	1111001	0100100	0110000	0011001	0010010	0000010	1111000	0000000	0010000

Problem 4 (Decimal27Seg TB)



Problem 5 (Pin assignment)

File Edit View Processing Tools Window Help

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Report

Report not available

Groups Report

Tasks

Early Pin Planning

Early Pin Planning...

Top View - Wire Bond
MAX 10 - 10M80DAF484C6GES

Pin Legend

- Symbol Pin Type
- User assigned I...
- Fitter assigned L...
- Unbonded pad
- Reserved pin
- Other configura...
- DEV_OE
- DEV_CLR
- DIFF_n
- DIFF_p

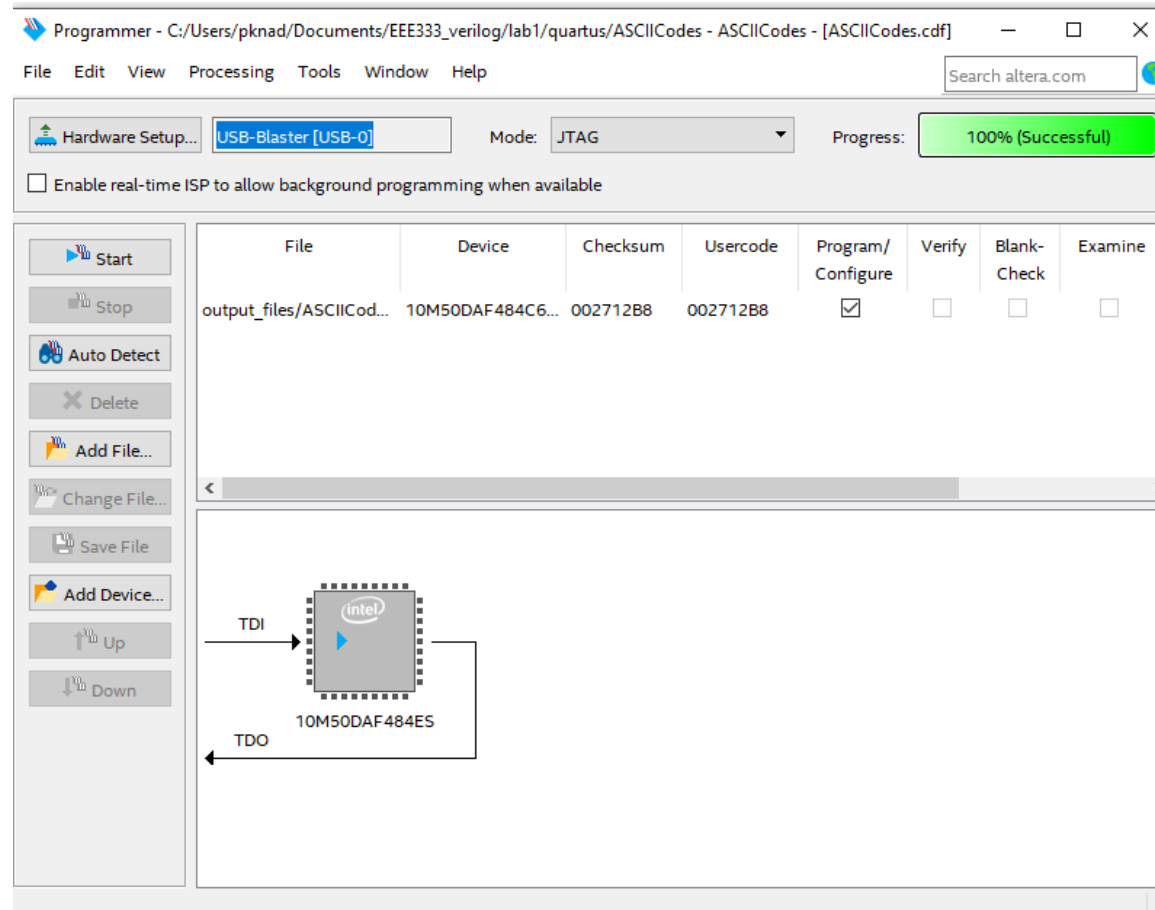
Filter: Pins: all

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	Strict Preservation
HexSeg0[3]	Output	PIN_C16	7	B7_NO	PIN_C16	2.5 V		12mA (default)	2 (default)		
HexSeg0[2]	Output	PIN_C15	7	B7_NO	PIN_C15	2.5 V		12mA (default)	2 (default)		
HexSeg0[1]	Output	PIN_E15	7	B7_NO	PIN_E15	2.5 V		12mA (default)	2 (default)		
HexSeg0[0]	Output	PIN_C14	7	B7_NO	PIN_C14	2.5 V		12mA (default)	2 (default)		
HexSeg1[6]	Output	PIN_B17	7	B7_NO	PIN_B17	2.5 V		12mA (default)	2 (default)		
HexSeg1[5]	Output	PIN_A18	7	B7_NO	PIN_A18	2.5 V		12mA (default)	2 (default)		
HexSeg1[4]	Output	PIN_A17	7	B7_NO	PIN_A17	2.5 V		12mA (default)	2 (default)		
HexSeg1[3]	Output	PIN_B16	7	B7_NO	PIN_B16	2.5 V		12mA (default)	2 (default)		
HexSeg1[2]	Output	PIN_E18	6	B6_NO	PIN_E18	2.5 V		12mA (default)	2 (default)		
HexSeg1[1]	Output	PIN_D18	6	B6_NO	PIN_D18	2.5 V		12mA (default)	2 (default)		
HexSeg1[0]	Output	PIN_C18	7	B7_NO	PIN_C18	2.5 V		12mA (default)	2 (default)		
HexSeg2[6]	Output	PIN_B22	6	B6_NO	PIN_B22	2.5 V		12mA (default)	2 (default)		
HexSeg2[5]	Output	PIN_C22	6	B6_NO	PIN_C22	2.5 V		12mA (default)	2 (default)		
HexSeg2[4]	Output	PIN_B21	6	B6_NO	PIN_B21	2.5 V		12mA (default)	2 (default)		
HexSeg2[3]	Output	PIN_A21	6	B6_NO	PIN_A21	2.5 V		12mA (default)	2 (default)		
HexSeg2[2]	Output	PIN_B19	7	B7_NO	PIN_B19	2.5 V		12mA (default)	2 (default)		
HexSeg2[1]	Output	PIN_A20	7	B7_NO	PIN_A20	2.5 V		12mA (default)	2 (default)		
HexSeg2[0]	Output	PIN_B20	6	B6_NO	PIN_B20	2.5 V		12mA (default)	2 (default)		
HexSeg3[6]	Output	PIN_E17	6	B6_NO	PIN_E17	2.5 V		12mA (default)	2 (default)		
HexSeg3[5]	Output	PIN_D19	6	B6_NO	PIN_D19	2.5 V		12mA (default)	2 (default)		
HexSeg3[4]	Output	PIN_C20	6	B6_NO	PIN_C20	2.5 V		12mA (default)	2 (default)		
HexSeg3[3]	Output	PIN_C19	7	B7_NO	PIN_C19	2.5 V		12mA (default)	2 (default)		
HexSeg3[2]	Output	PIN_E21	6	B6_NO	PIN_E21	2.5 V		12mA (default)	2 (default)		
HexSeg3[1]	Output	PIN_E22	6	B6_NO	PIN_E22	2.5 V		12mA (default)	2 (default)		
HexSeg3[0]	Output	PIN_F21	6	B6_NO	PIN_F21	2.5 V		12mA (default)	2 (default)		
HexSeg4[6]	Output	PIN_F20	6	B6_NO	PIN_F20	2.5 V		12mA (default)	2 (default)		
HexSeg4[5]	Output	PIN_F19	6	B6_NO	PIN_F19	2.5 V		12mA (default)	2 (default)		
HexSeg4[4]	Output	PIN_H19	6	B6_NO	PIN_H19	2.5 V		12mA (default)	2 (default)		
HexSeg4[3]	Output	PIN_J18	6	B6_NO	PIN_J18	2.5 V		12mA (default)	2 (default)		
HexSeg4[2]	Output	PIN_E19	6	B6_NO	PIN_E19	2.5 V		12mA (default)	2 (default)		
HexSeg4[1]	Output	PIN_E20	6	B6_NO	PIN_E20	2.5 V		12mA (default)	2 (default)		
HexSeg4[0]	Output	PIN_F18	6	B6_NO	PIN_F18	2.5 V		12mA (default)	2 (default)		
Kkey0	Input	PIN_B8	7	B7_NO	PIN_B8	2.5 V		12mA (default)			
<<new node>>											

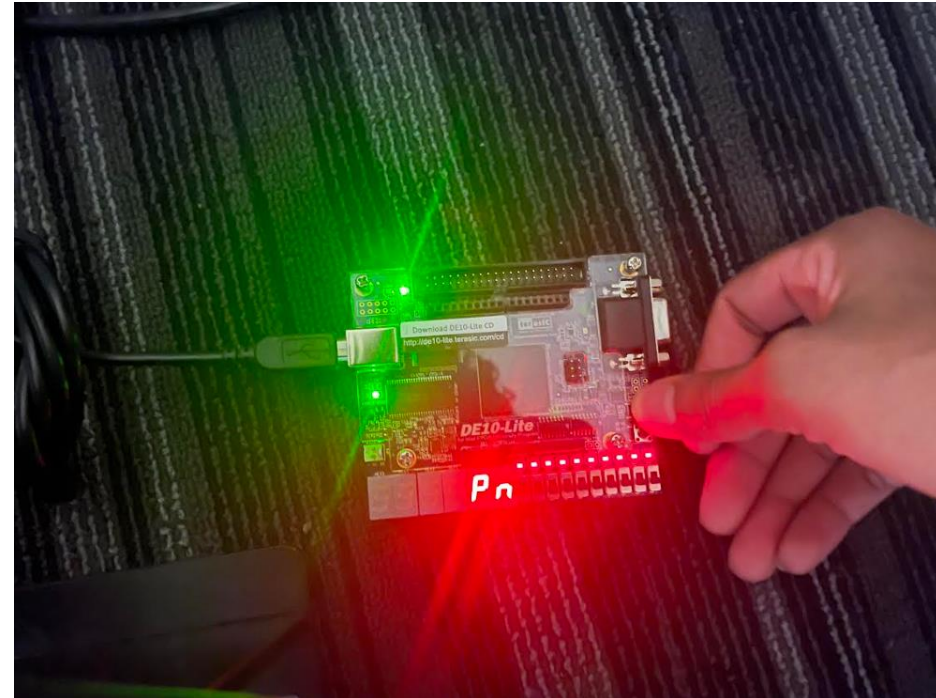
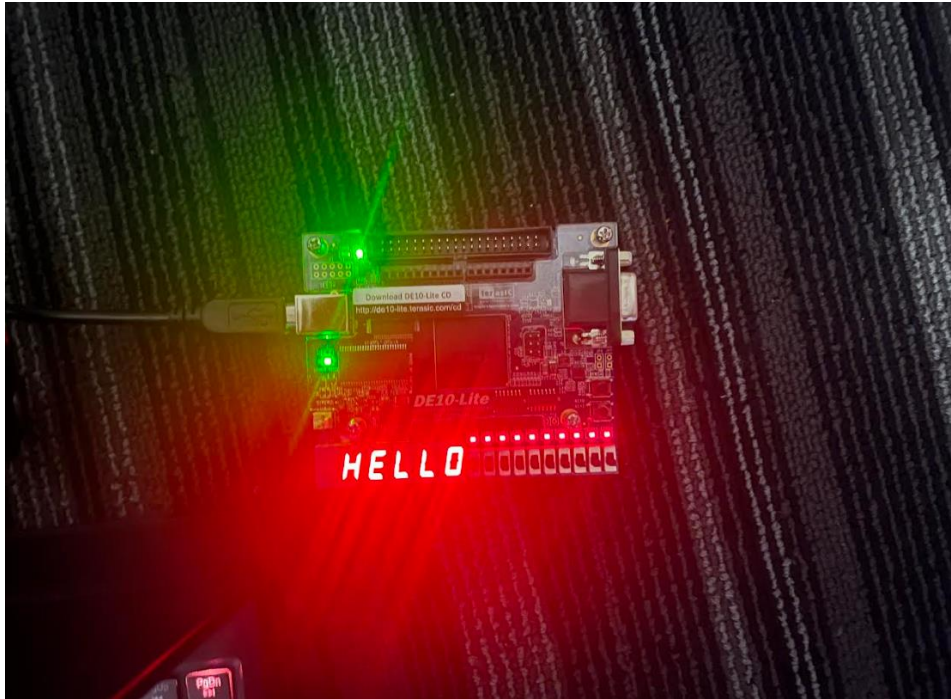
All Pins

0% 00:00:00

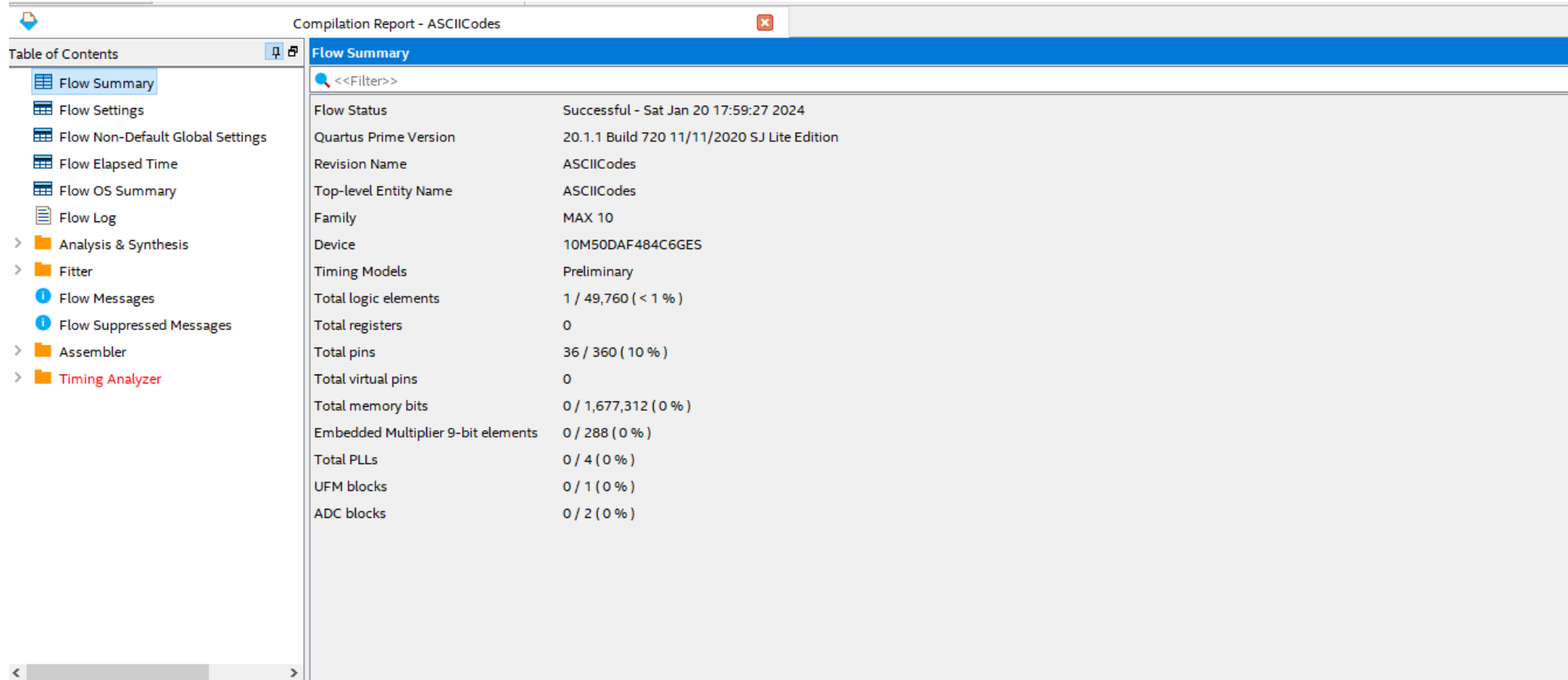
Problem 5 (Successful Programming)



Problem 5 (Final Product)



Problem 5 (Flow Summary)



Compilation Report - ASCII Codes

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- > Analysis & Synthesis
- > Fitter
- > Flow Messages
- > Flow Suppressed Messages
- > Assembler
- > Timing Analyzer

Flow Summary

<<Filter>>

Flow Status	Successful - Sat Jan 20 17:59:27 2024
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	ASCII Codes
Top-level Entity Name	ASCII Codes
Family	MAX 10
Device	10M50DAF484C6GES
Timing Models	Preliminary
Total logic elements	1 / 49,760 (< 1 %)
Total registers	0
Total pins	36 / 360 (10 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)