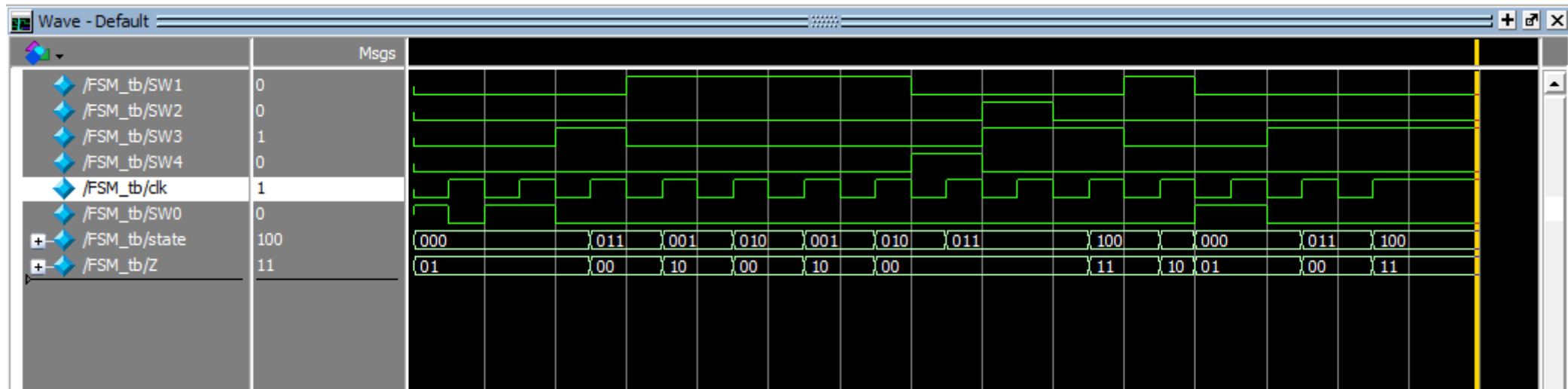


Lab 3

Pranav Nadimpalli

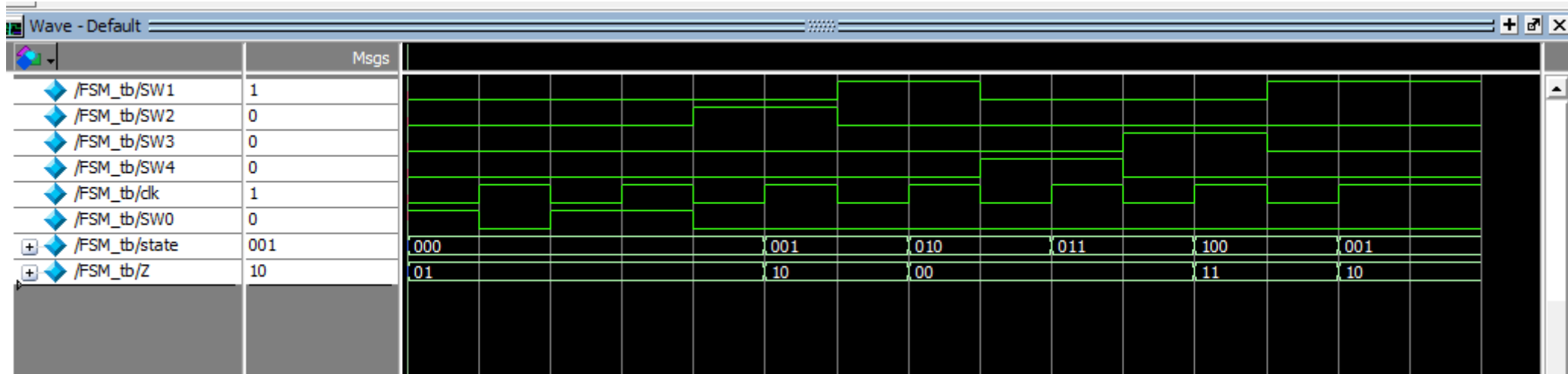
FSM Simulation Demo Part 1

First clock pulse is reset



FSM Simulation Demo Part 2

First clock pulse is reset



FPGA Progarammed

Programmer - C:/Users/pknad/Documents/EEE333_verilog/lab3/quartus/FSM_pv - FSM_pv - [FSM_pv.cdf]*

File Edit View Processing Tools Window Help

Hardware Setup... USB-Blaster [USB-0] Mode: JTAG Progress: 100% (Successful)

☐ Enable real-time ISP to allow background programming when available

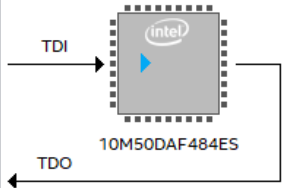
Start Stop Auto Detect Delete Add File... Change File... Save File Add Device... Up Down

File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP
output_files/FSM_pv.sof	10M50DAF484C6...	002746BA	002746BA	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

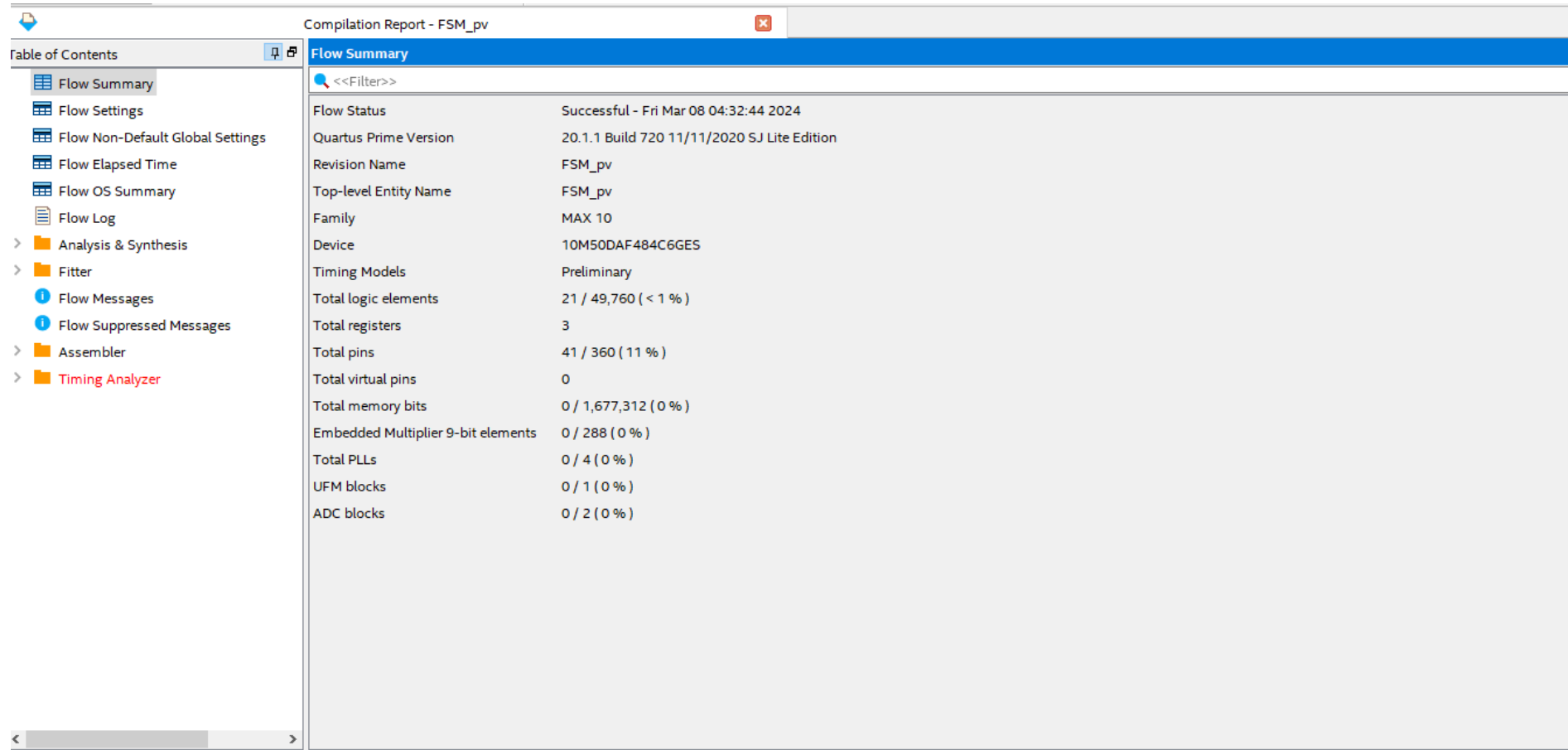
TDI

10M50DAF484ES

TDO



FPGA Flow Summary



The screenshot displays the 'Compilation Report - FSM_pv' window in Quartus Prime. The 'Flow Summary' tab is active, showing a table of compilation statistics. The left sidebar contains a 'Table of Contents' with various report sections, including 'Flow Summary', 'Flow Settings', 'Flow Non-Default Global Settings', 'Flow Elapsed Time', 'Flow OS Summary', 'Flow Log', 'Analysis & Synthesis', 'Fitter', 'Flow Messages', 'Flow Suppressed Messages', 'Assembler', and 'Timing Analyzer'.

Flow Summary	
Flow Status	Successful - Fri Mar 08 04:32:44 2024
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	FSM_pv
Top-level Entity Name	FSM_pv
Family	MAX 10
Device	10M50DAF484C6GES
Timing Models	Preliminary
Total logic elements	21 / 49,760 (< 1 %)
Total registers	3
Total pins	41 / 360 (11 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

FPGA Pin Assignment

Pin Planner - C:/Users/pknad/Documents/EEE333_verilog/lab3/quartus/FSM_pv - FSM_pv

File Edit View Processing Tools Window Help

Report not available

Groups Report

Tasks

Early Pin Planning

Early Pin Planning...

Top View - Wire Bond
MAX 10 - 10M60DAF48C6GES

Pin Legend

Symbol Pin Type

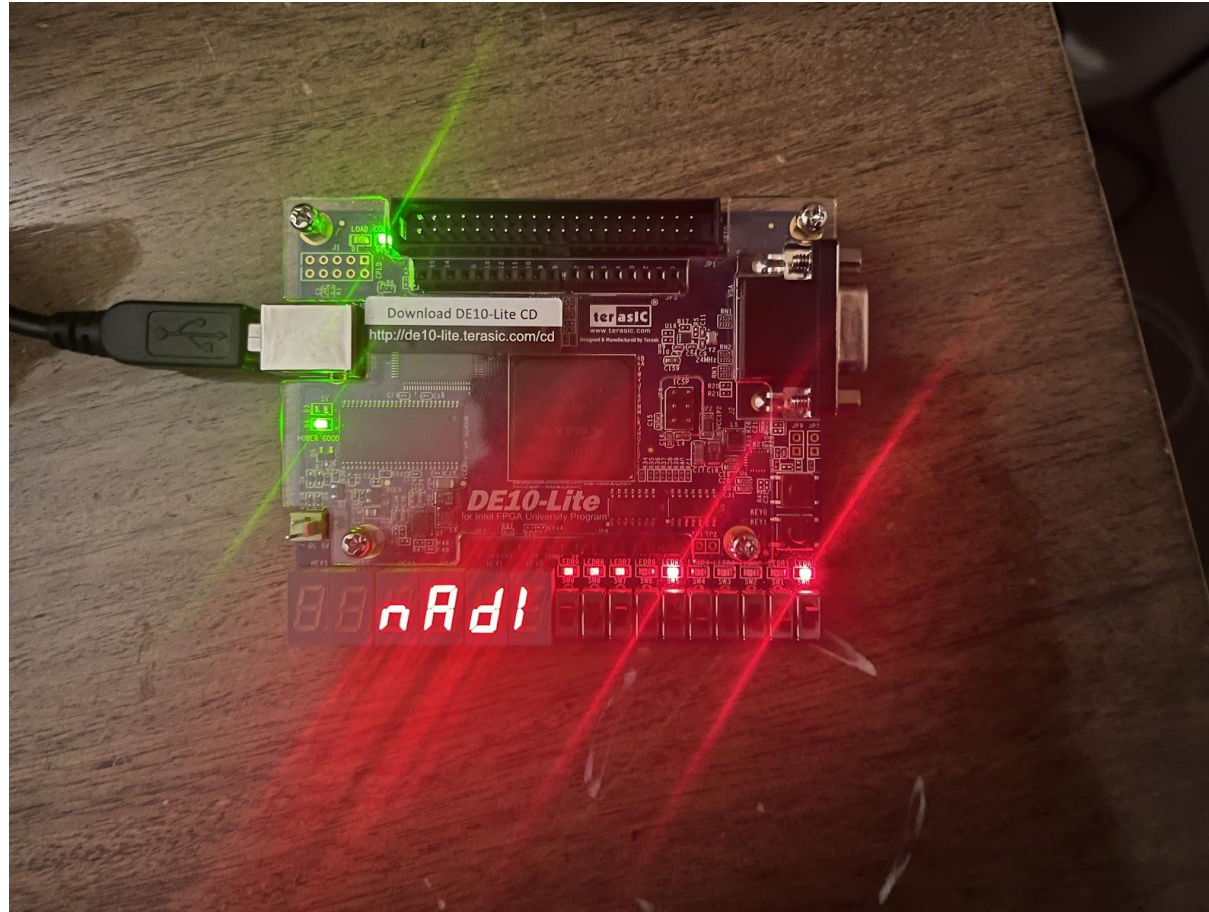
- User I/O
- User assigned I...
- Fitter assigned I...
- Unbonded pad
- Reserved pin
- Other configura...
- DEV_OE
- DEV_CLR

Filter: Pins: all

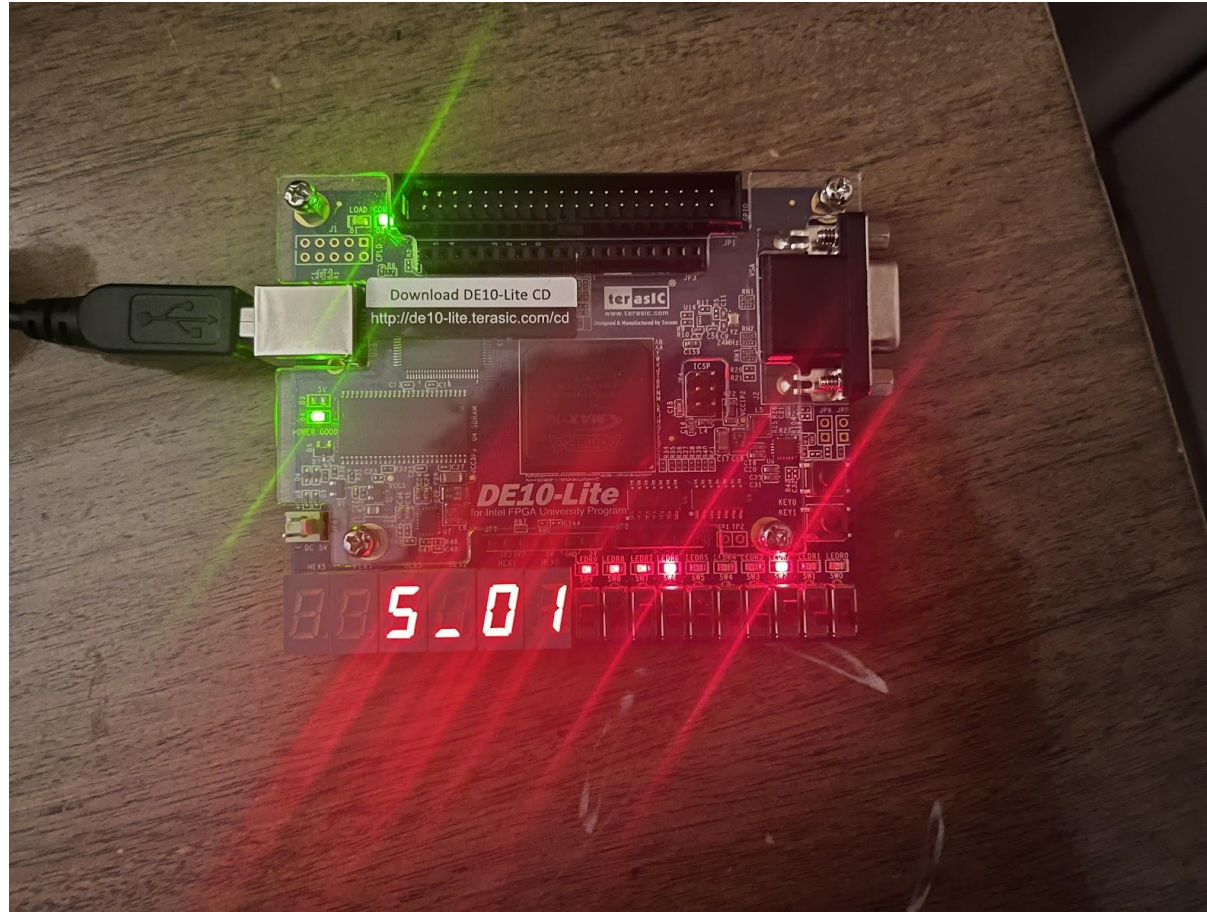
Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	Strict Preservation
Key0	Input	PIN_B8	7	B7_NO	PIN_B8	2.5 V		12mA (default)			
LED_SW[6]	Output	PIN_E14	7	B7_NO	PIN_E14	2.5 V		12mA (default)	2 (default)		
LED_SW[5]	Output	PIN_C13	7	B7_NO	PIN_C13	2.5 V		12mA (default)	2 (default)		
LED_SW[4]	Output	PIN_D13	7	B7_NO	PIN_D13	2.5 V		12mA (default)	2 (default)		
LED_SW[3]	Output	PIN_B10	7	B7_NO	PIN_B10	2.5 V		12mA (default)	2 (default)		
LED_SW[2]	Output	PIN_A10	7	B7_NO	PIN_A10	2.5 V		12mA (default)	2 (default)		
LED_SW[1]	Output	PIN_A9	7	B7_NO	PIN_A9	2.5 V		12mA (default)	2 (default)		
LED_SW[0]	Output	PIN_A8	7	B7_NO	PIN_A8	2.5 V		12mA (default)	2 (default)		
SEG0[6]	Output	PIN_C17	7	B7_NO	PIN_C17	2.5 V		12mA (default)	2 (default)		
SEG0[5]	Output	PIN_D17	7	B7_NO	PIN_D17	2.5 V		12mA (default)	2 (default)		
SEG0[4]	Output	PIN_E16	7	B7_NO	PIN_E16	2.5 V		12mA (default)	2 (default)		
SEG0[3]	Output	PIN_C16	7	B7_NO	PIN_C16	2.5 V		12mA (default)	2 (default)		
SEG0[2]	Output	PIN_C15	7	B7_NO	PIN_C15	2.5 V		12mA (default)	2 (default)		
SEG0[1]	Output	PIN_E15	7	B7_NO	PIN_E15	2.5 V		12mA (default)	2 (default)		
SEG0[0]	Output	PIN_C14	7	B7_NO	PIN_C14	2.5 V		12mA (default)	2 (default)		
SEG1[6]	Output	PIN_B17	7	B7_NO	PIN_B17	2.5 V		12mA (default)	2 (default)		
SEG1[5]	Output	PIN_A18	7	B7_NO	PIN_A18	2.5 V		12mA (default)	2 (default)		
SEG1[4]	Output	PIN_A17	7	B7_NO	PIN_A17	2.5 V		12mA (default)	2 (default)		
SEG1[3]	Output	PIN_B16	7	B7_NO	PIN_B16	2.5 V		12mA (default)	2 (default)		
SEG1[2]	Output	PIN_E18	6	B6_NO	PIN_E18	2.5 V		12mA (default)	2 (default)		
SEG1[1]	Output	PIN_D18	6	B6_NO	PIN_D18	2.5 V		12mA (default)	2 (default)		
SEG1[0]	Output	PIN_C18	7	B7_NO	PIN_C18	2.5 V		12mA (default)	2 (default)		
SEG2[6]	Output	PIN_B22	6	B6_NO	PIN_B22	2.5 V		12mA (default)	2 (default)		
SEG2[5]	Output	PIN_C22	6	B6_NO	PIN_C22	2.5 V		12mA (default)	2 (default)		
SEG2[4]	Output	PIN_B21	6	B6_NO	PIN_B21	2.5 V		12mA (default)	2 (default)		
SEG2[3]	Output	PIN_A21	6	B6_NO	PIN_A21	2.5 V		12mA (default)	2 (default)		
SEG2[2]	Output	PIN_B19	7	B7_NO	PIN_B19	2.5 V		12mA (default)	2 (default)		
SEG2[1]	Output	PIN_A20	7	B7_NO	PIN_A20	2.5 V		12mA (default)	2 (default)		
SEG2[0]	Output	PIN_B20	6	B6_NO	PIN_B20	2.5 V		12mA (default)	2 (default)		
SEG3[6]	Output	PIN_E17	6	B6_NO	PIN_E17	2.5 V		12mA (default)	2 (default)		
SEG3[5]	Output	PIN_D19	6	B6_NO	PIN_D19	2.5 V		12mA (default)	2 (default)		
SEG3[4]	Output	PIN_C20	6	B6_NO	PIN_C20	2.5 V		12mA (default)	2 (default)		
SEG3[3]	Output	PIN_C19	7	B7_NO	PIN_C19	2.5 V		12mA (default)	2 (default)		
SEG3[2]	Output	PIN_E21	6	B6_NO	PIN_E21	2.5 V		12mA (default)	2 (default)		
SEG3[1]	Output	PIN_E22	6	B6_NO	PIN_E22	2.5 V		12mA (default)	2 (default)		
SEG3[0]	Output	PIN_E23	6	B6_NO	PIN_E23	2.5 V		12mA (default)	2 (default)		

0% 00:00:00

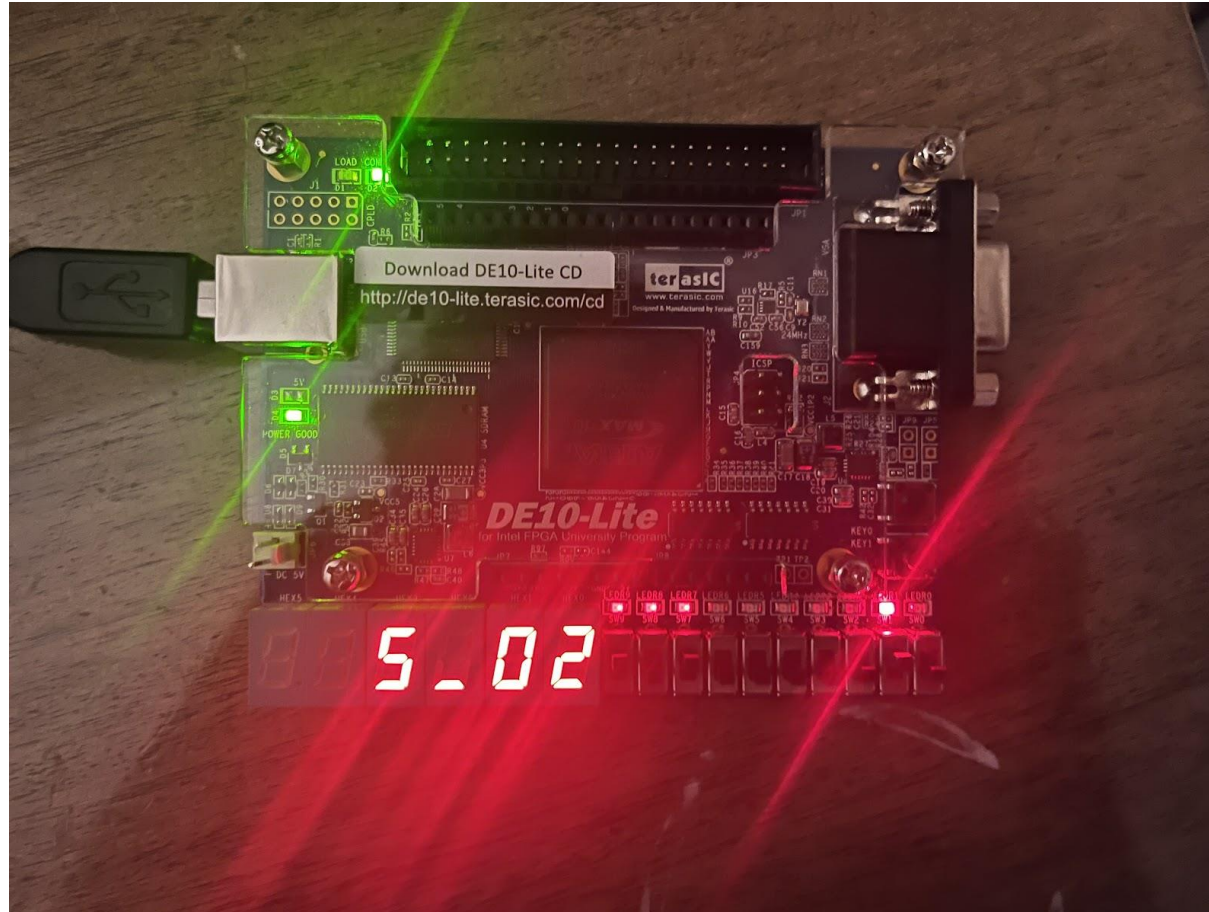
FPGA Test SW0=1; Z=01; Step 1



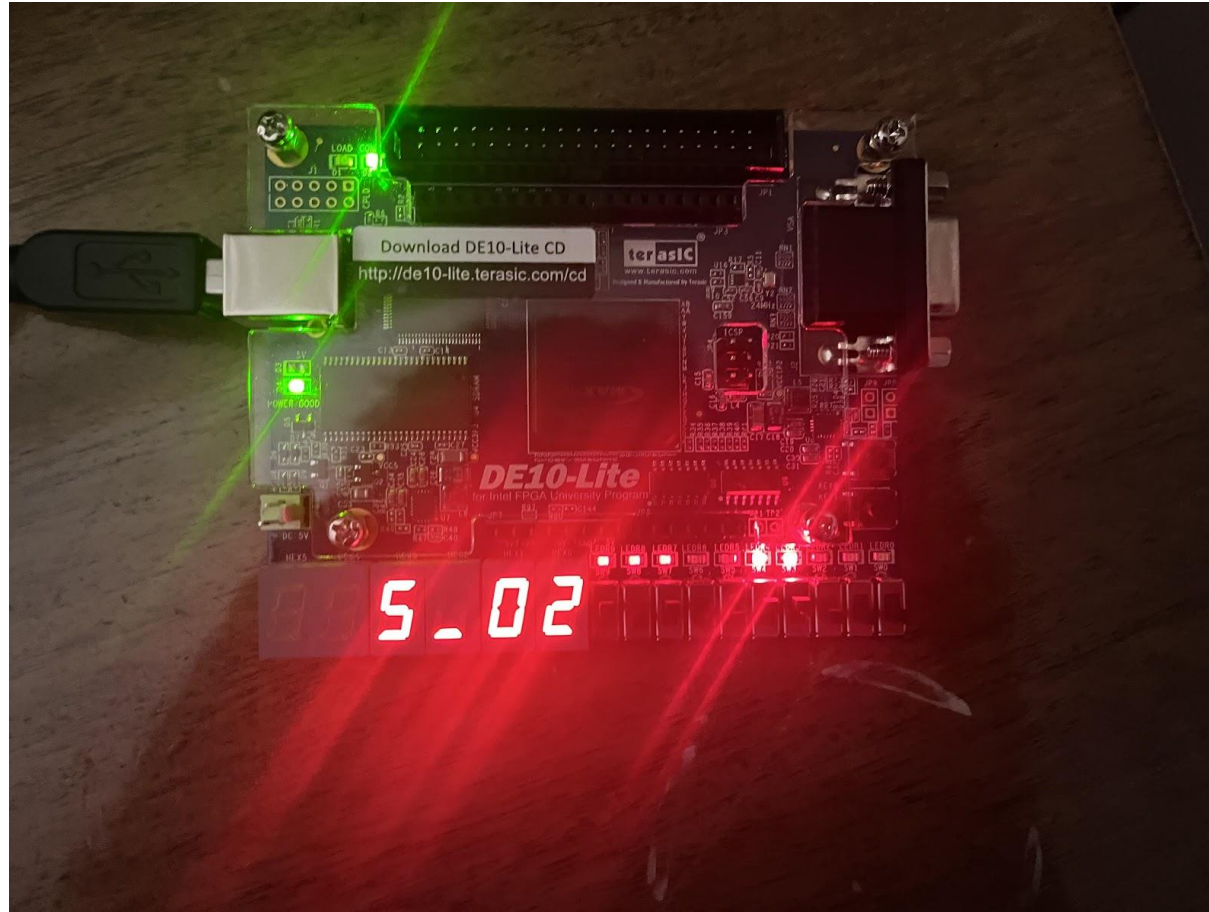
FPGA Test SW2=1; Z=10 Step 2



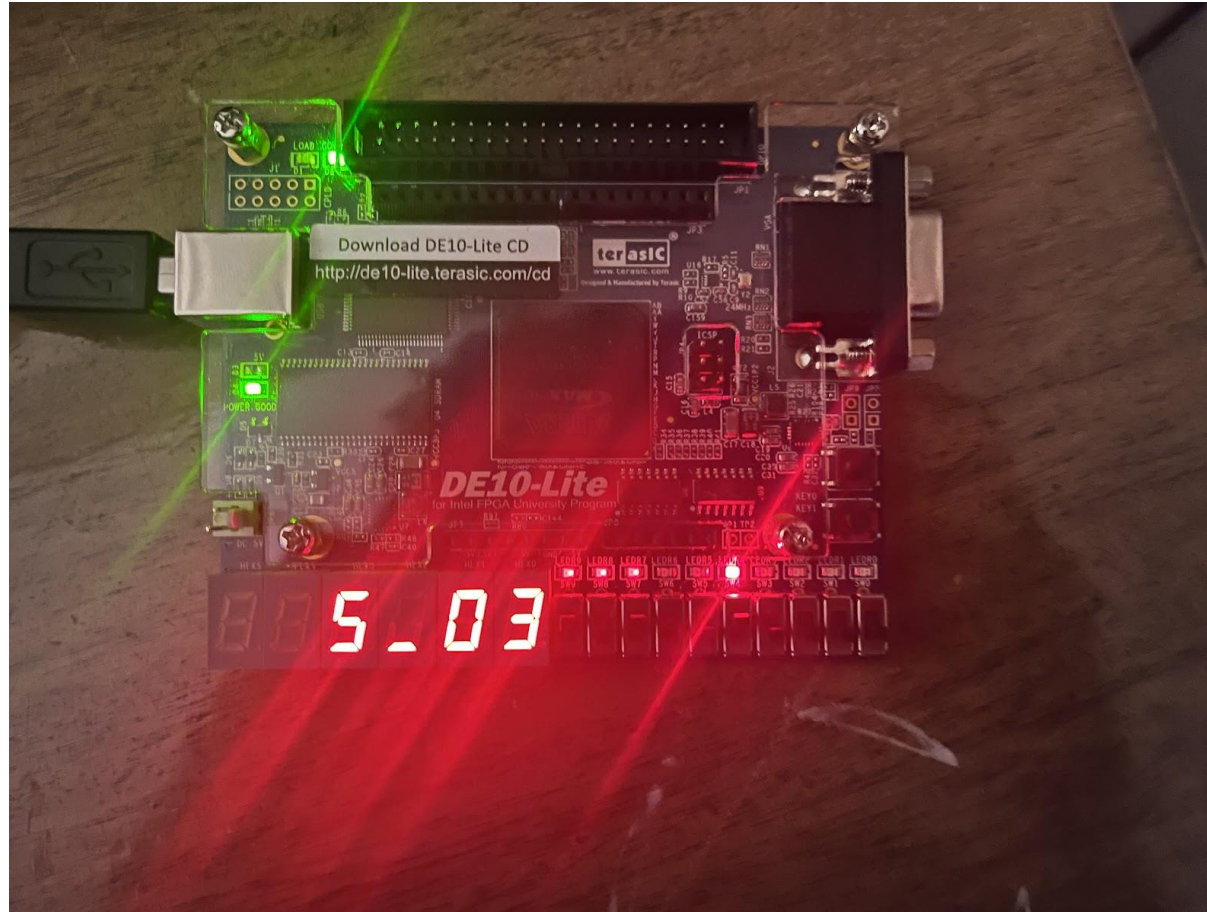
FPGA Test SW1=1; Z=00 Step 3



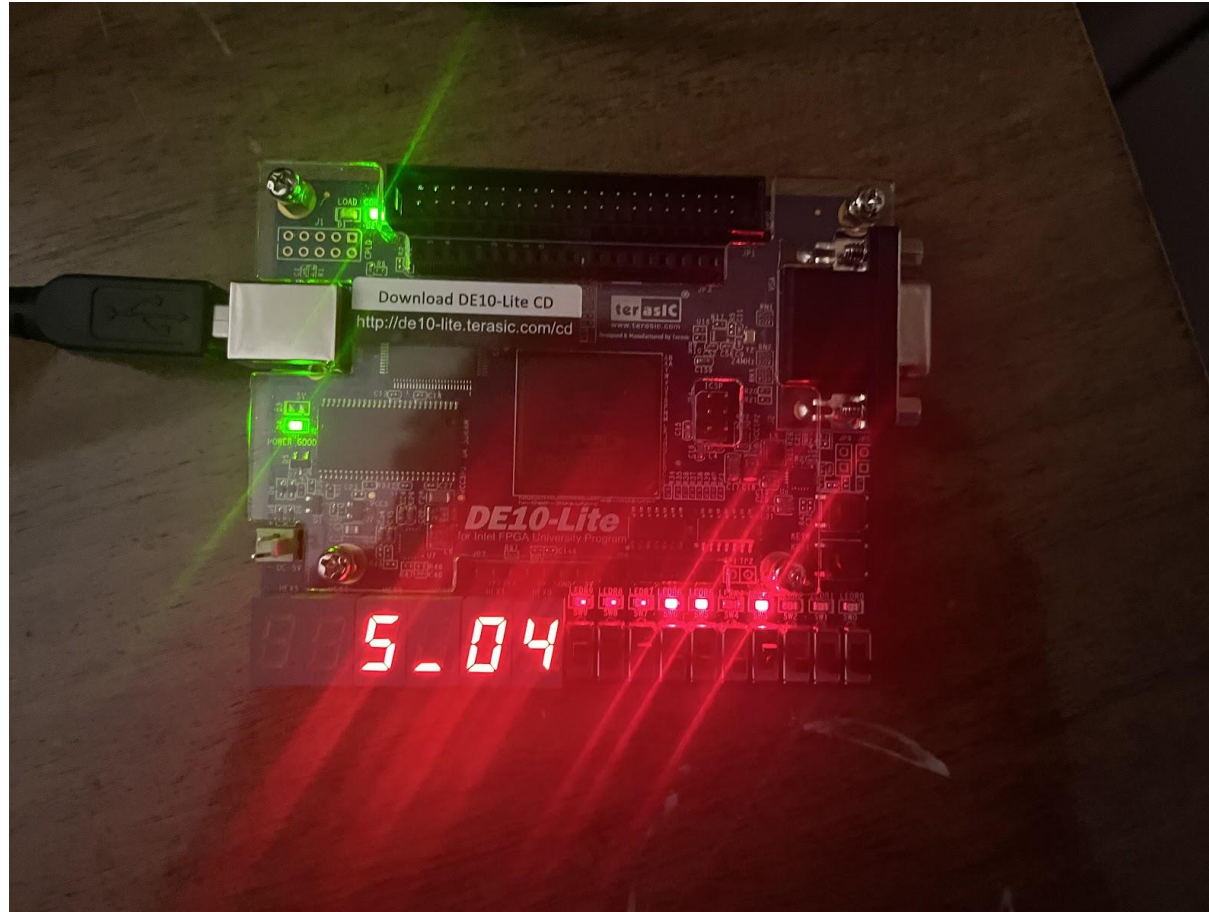
FPGA test SW3&SW4 = 1; Z=00 Step 4



FPGA Test SW4=1; Z=00 Step 5



FPGA Test SW3=1; Z=11 Step 6



FPGA Test SW4=1; Z=11 Step 7

