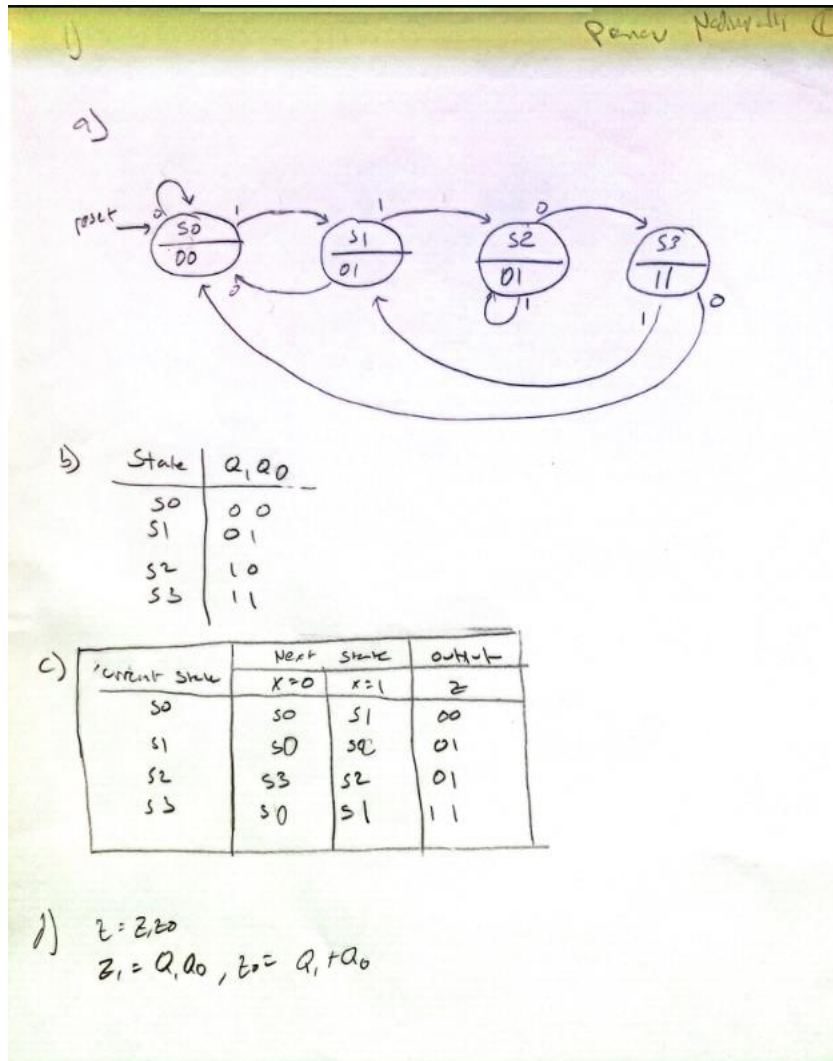


Homework 6

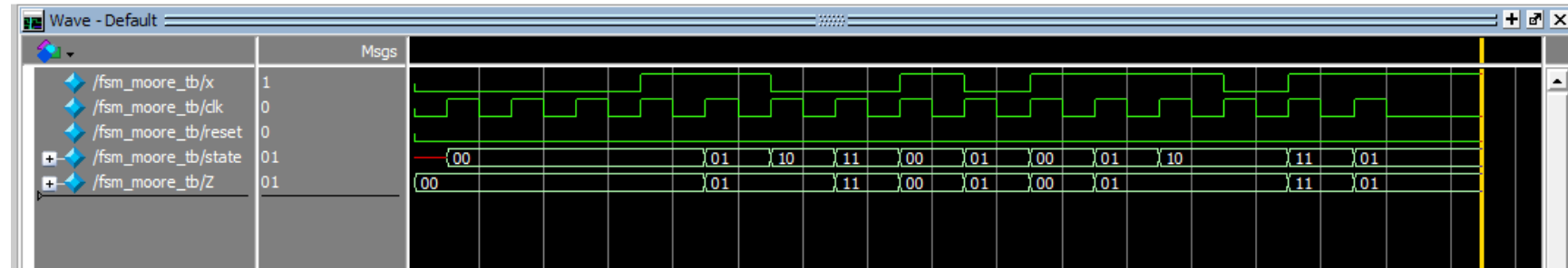
Pranav Nadimpalli

Problem 1 Moore Answers



Problem 2 Wave Forms + Transcript

```
/Z
VSIM 42> run
run
# State: 00, x: 0, Z: 00
run
run
# State: 00, x: 0, Z: 00
run
run
# State: 00, x: 0, Z: 00
run
run
# State: 00, x: 1, Z: 00
run
run
# State: 01, x: 1, Z: 01
run
run
# State: 10, x: 0, Z: 01
run
run
# State: 11, x: 0, Z: 11
run
run
# State: 00, x: 1, Z: 00
run
run
# State: 01, x: 0, Z: 01
run
run
# State: 00, x: 1, Z: 00
run
run
# State: 01, x: 1, Z: 01
run
run
# State: 10, x: 1, Z: 01
run
run
# State: 10, x: 0, Z: 01
run
run
# State: 11, x: 1, Z: 11
run
run
# State: 01, x: 1, Z: 01
run
run
VSIM 43> run
```

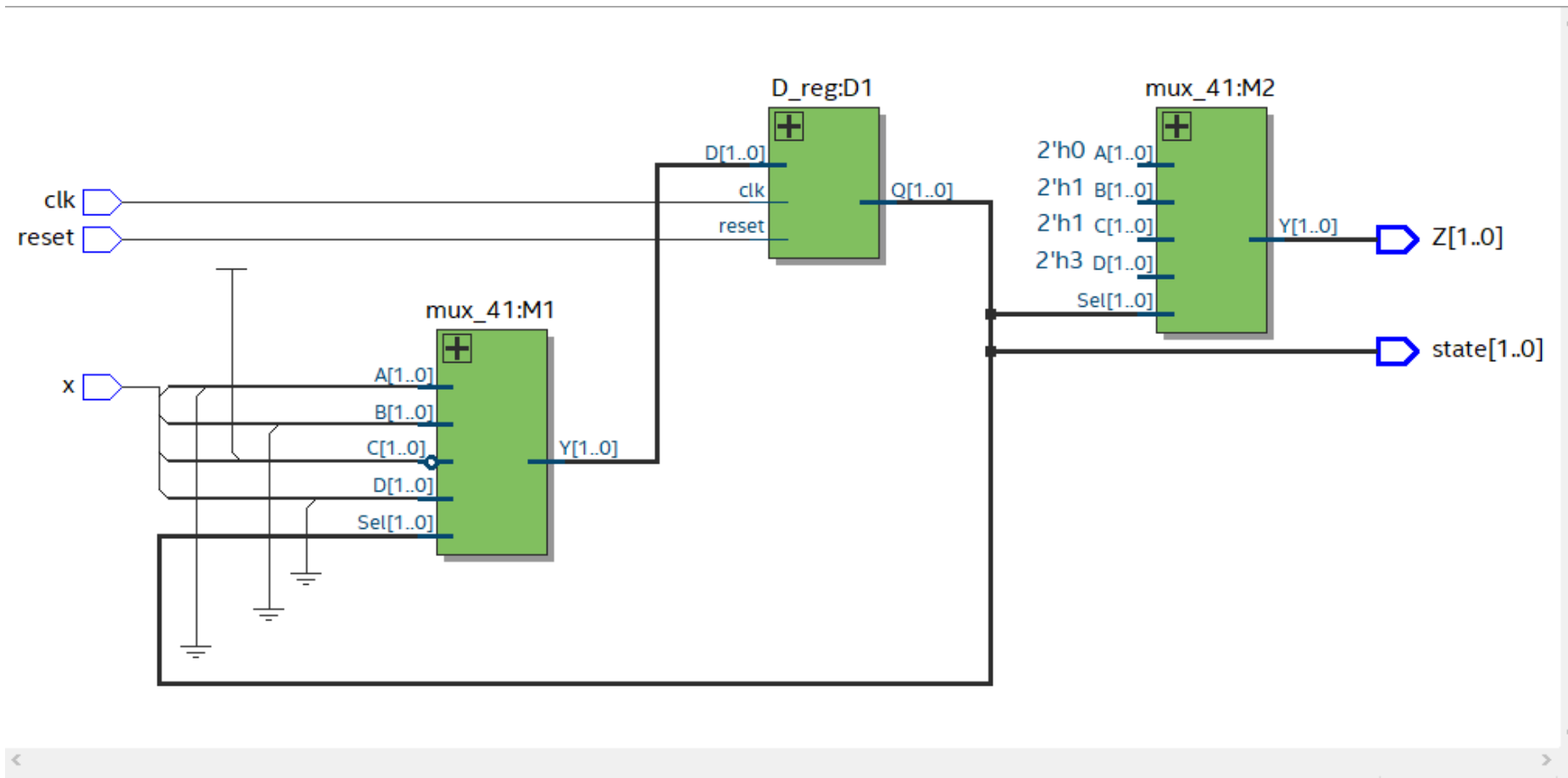


Problem 2 Moore Flow Summary

Table of Contents		Flow Summary	
<ul style="list-style-type: none">Flow SummaryFlow SettingsFlow Non-Default Global SettingsFlow Elapsed TimeFlow OS SummaryFlow Log> Analysis & Synthesis> FitterFlow MessagesFlow Suppressed Messages> Assembler> Timing Analyzer		<<Filter>>	
		Flow Status	Successful - Wed Feb 28 15:43:22 2024
		Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
		Revision Name	fsm_moore
		Top-level Entity Name	fsm_moore
		Family	MAX 10
		Device	10M50DAF484C6GES
		Timing Models	Preliminary
		Total logic elements	5 / 49,760 (< 1 %)
		Total registers	2
		Total pins	7 / 360 (2 %)
		Total virtual pins	0
		Total memory bits	0 / 1,677,312 (0 %)
		Embedded Multiplier 9-bit elements	0 / 288 (0 %)
		Total PLLs	0 / 4 (0 %)
		UFM blocks	0 / 1 (0 %)
		ADC blocks	0 / 2 (0 %)

Problem 2 Moore Net List

- The main difference is that my output logic is made through a mux

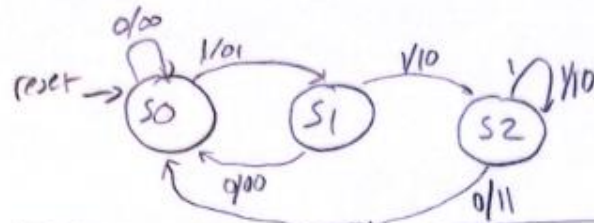


Problem 3 Mealy Answers

3) a)

Paras
Aradipati

②

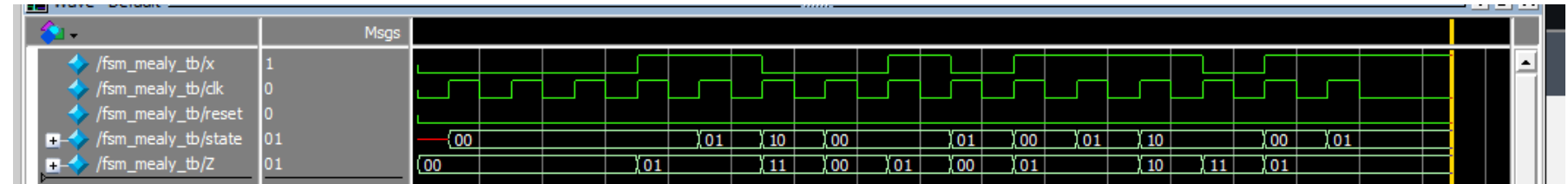


	Output Z		Next State	
	X=0	X=1	X=0	X=1
S0	00	01	S0	S1
S1	00	01	S0	S2
S2	11	10	S0	S2

	Q ₁	Q ₀
S0	0	0
S1	0	1
S2	1	0

Problem 3 Mealy Transcript + Waveforms

```
gvc
add wave -position end sim:/fsm_mealy_tb/Z
VSIM 21> run
run
# State: 00, x: 0, Z: 00
run
# State: 00, x: 0, Z: 00
run
# State: 00, x: 0, Z: 00
run
# State: 00, x: 1, Z: 01
run
# State: 01, x: 1, Z: 01
run
# State: 10, x: 0, Z: 11
run
# State: 00, x: 0, Z: 00
run
# State: 00, x: 1, Z: 01
run
# State: 01, x: 0, Z: 00
run
# State: 00, x: 1, Z: 01
run
# State: 01, x: 1, Z: 01
run
# State: 10, x: 1, Z: 10
run
# State: 10, x: 0, Z: 11
run
# State: 00, x: 1, Z: 01
run
# State: 01, x: 1, Z: 01
run
VSIM 22> run
VSIM 22>
```



Problem 3 Mealy Flow Summary

Table of Contents		Flow Summary	
Table of Contents		<<Filter>>	
Flow Summary		Flow Status	
Flow Settings		Successful - Wed Feb 28 18:52:08 2024	
Flow Non-Default Global Settings		Quartus Prime Version	
Flow Elapsed Time		20.1.1 Build 720 11/11/2020 SJ Lite Edition	
Flow OS Summary		Revision Name	
Flow Log		fsm_mealy	
> Analysis & Synthesis		Top-level Entity Name	
> Fitter		fsm_mealy	
Flow Messages		Family	
Flow Suppressed Messages		MAX 10	
> Assembler		Device	
> Timing Analyzer		10M50DAF484C6GES	
		Timing Models	
		Preliminary	
		Total logic elements	
		4 / 49,760 (< 1 %)	
		Total registers	
		2	
		Total pins	
		7 / 360 (2 %)	
		Total virtual pins	
		0	
		Total memory bits	
		0 / 1,677,312 (0 %)	
		Embedded Multiplier 9-bit elements	
		0 / 288 (0 %)	
		Total PLLs	
		0 / 4 (0 %)	
		UFM blocks	
		0 / 1 (0 %)	
		ADC blocks	
		0 / 2 (0 %)	

Problem 3 Mealy Net List

The main difference is that the output calculation involves the input X, and there is one less state in the design which should be expected.

