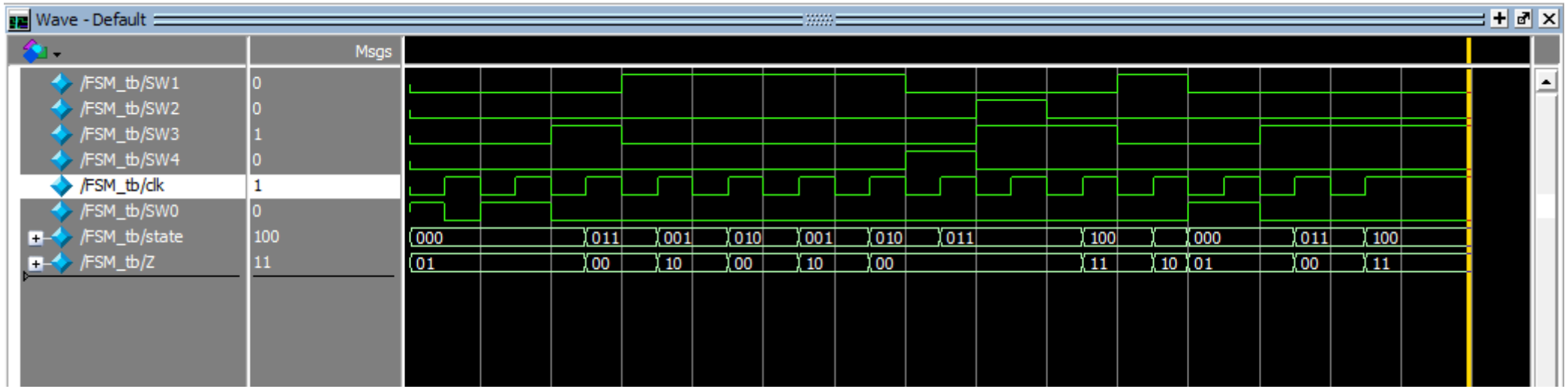
# Lab 3

Pranav Nadimpalli

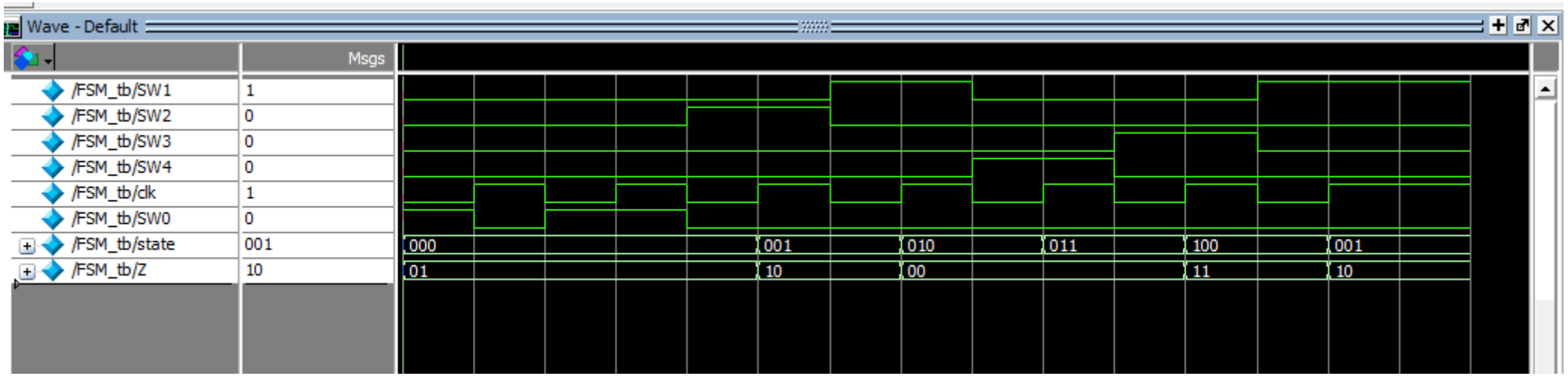
# FSM Simulation Demo Part 1

First  clock pulse is reset

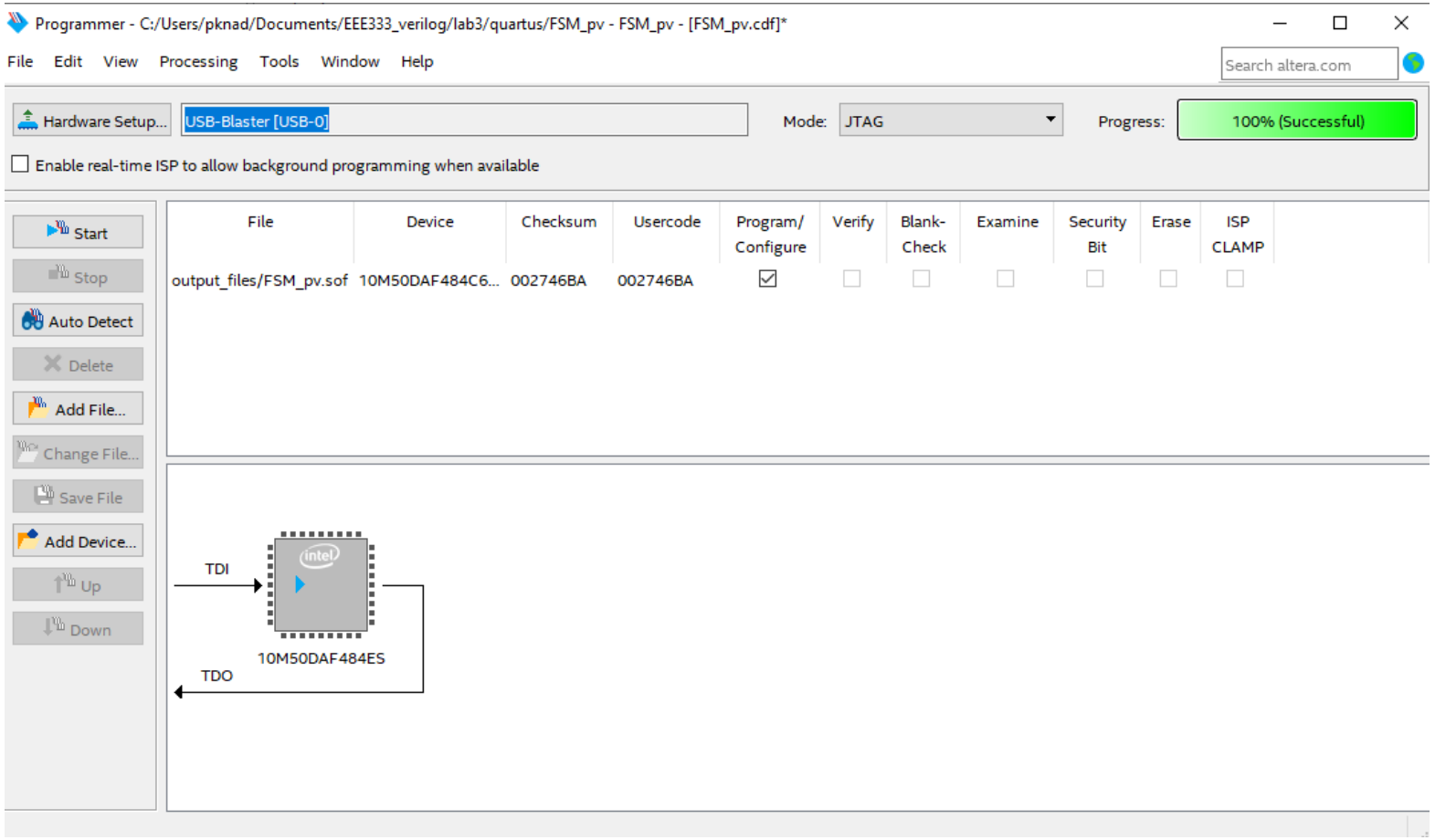


# FSM Simulation Demo Part 2

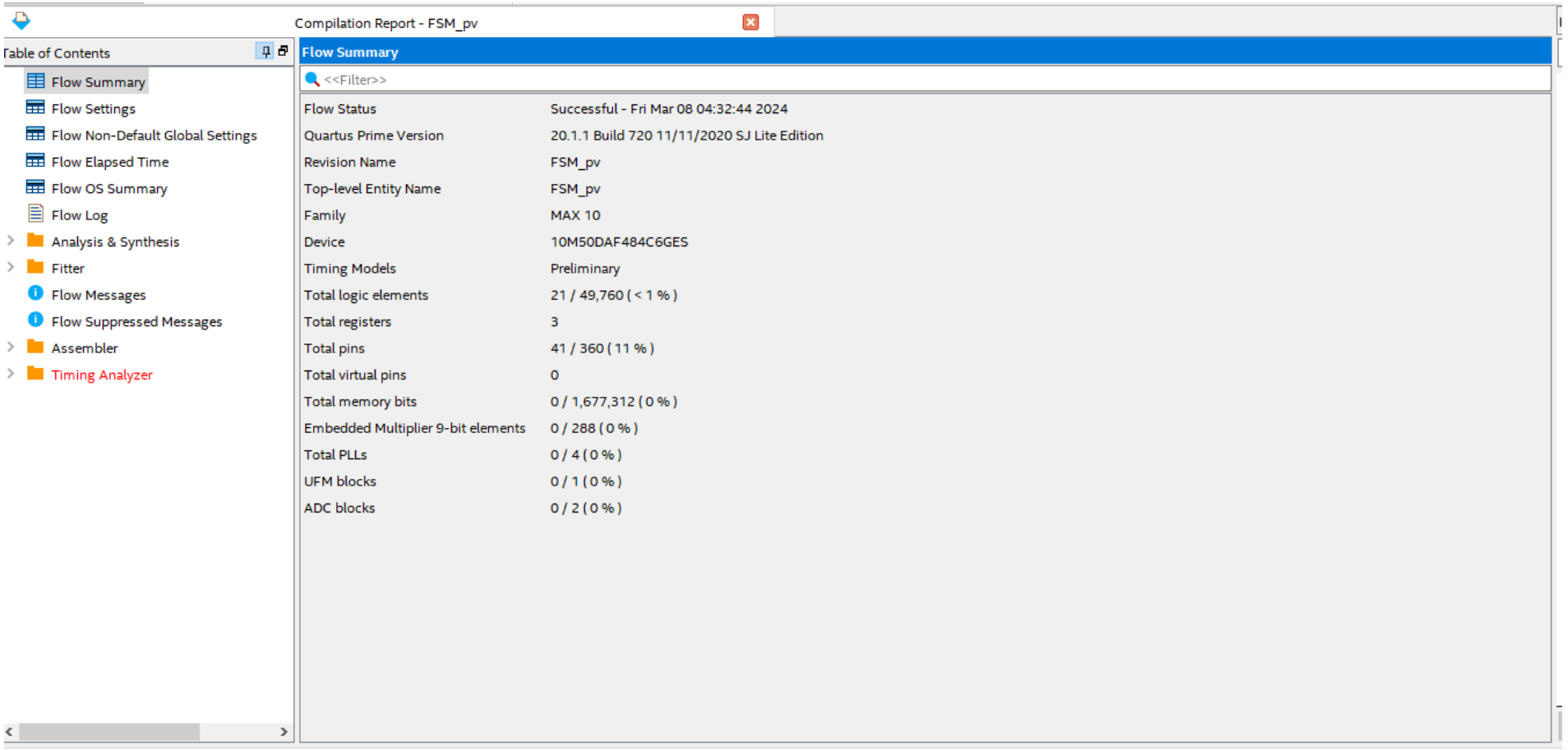
First  clock pulse is reset



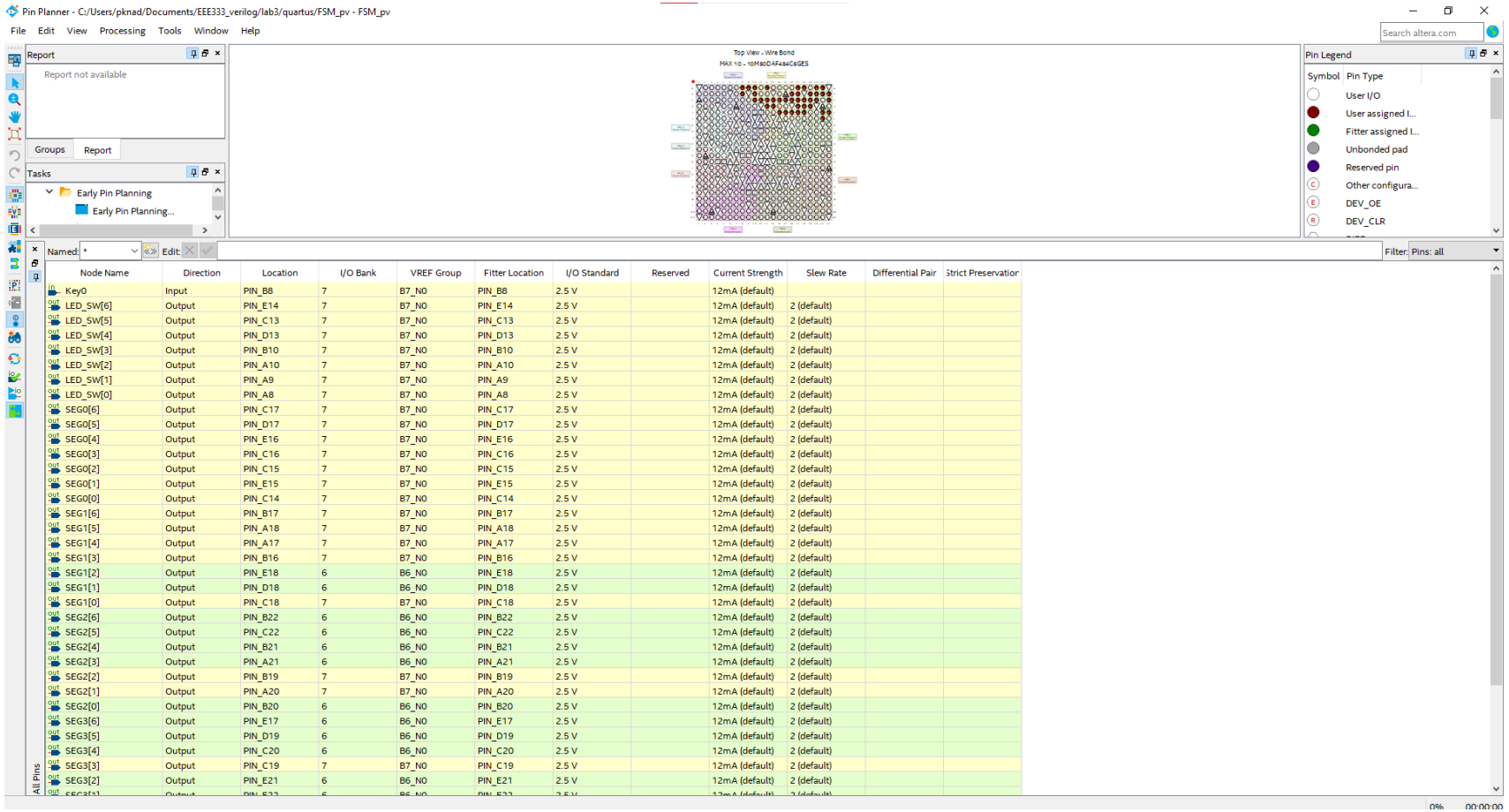
# FPGA Progarammed



# FPGA Flow Summary

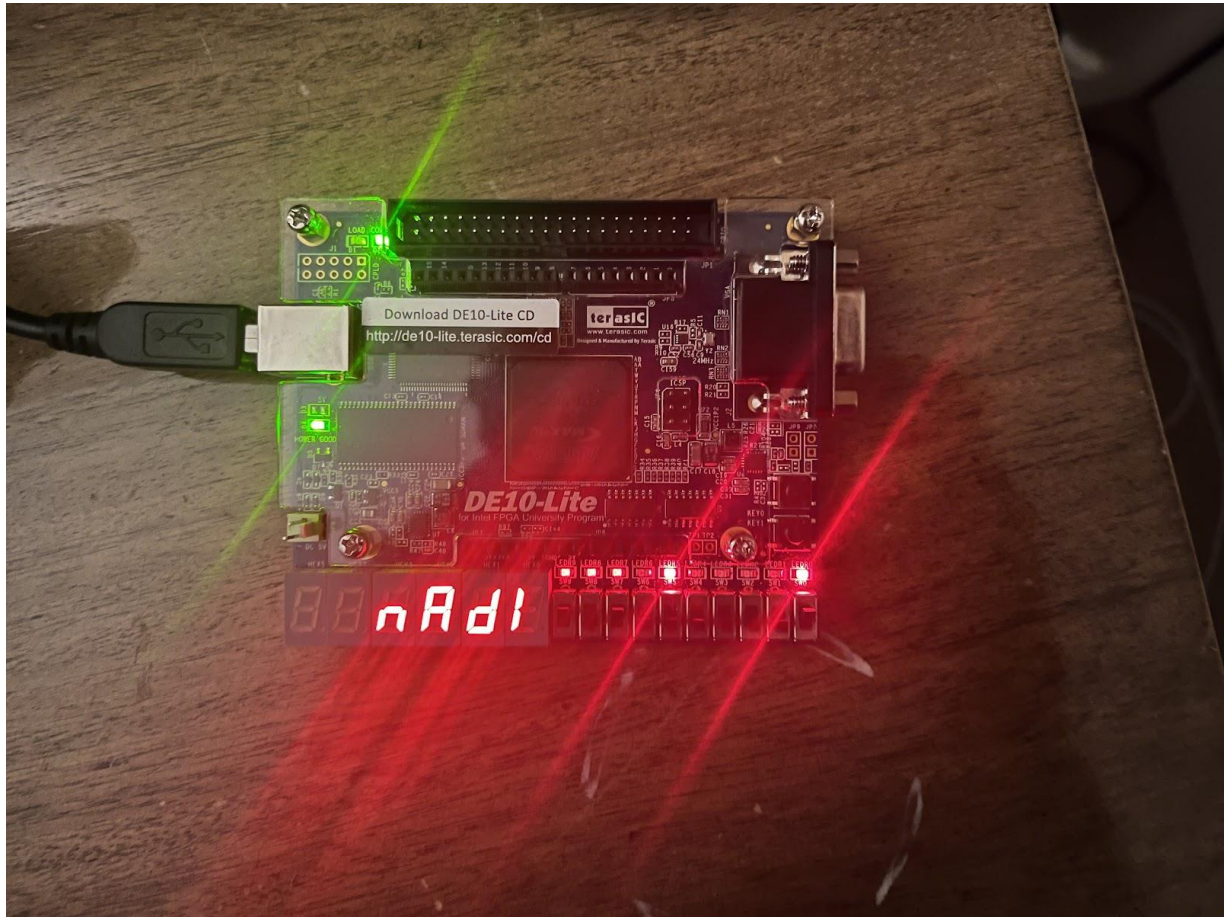


# FPGA Pin Assignment

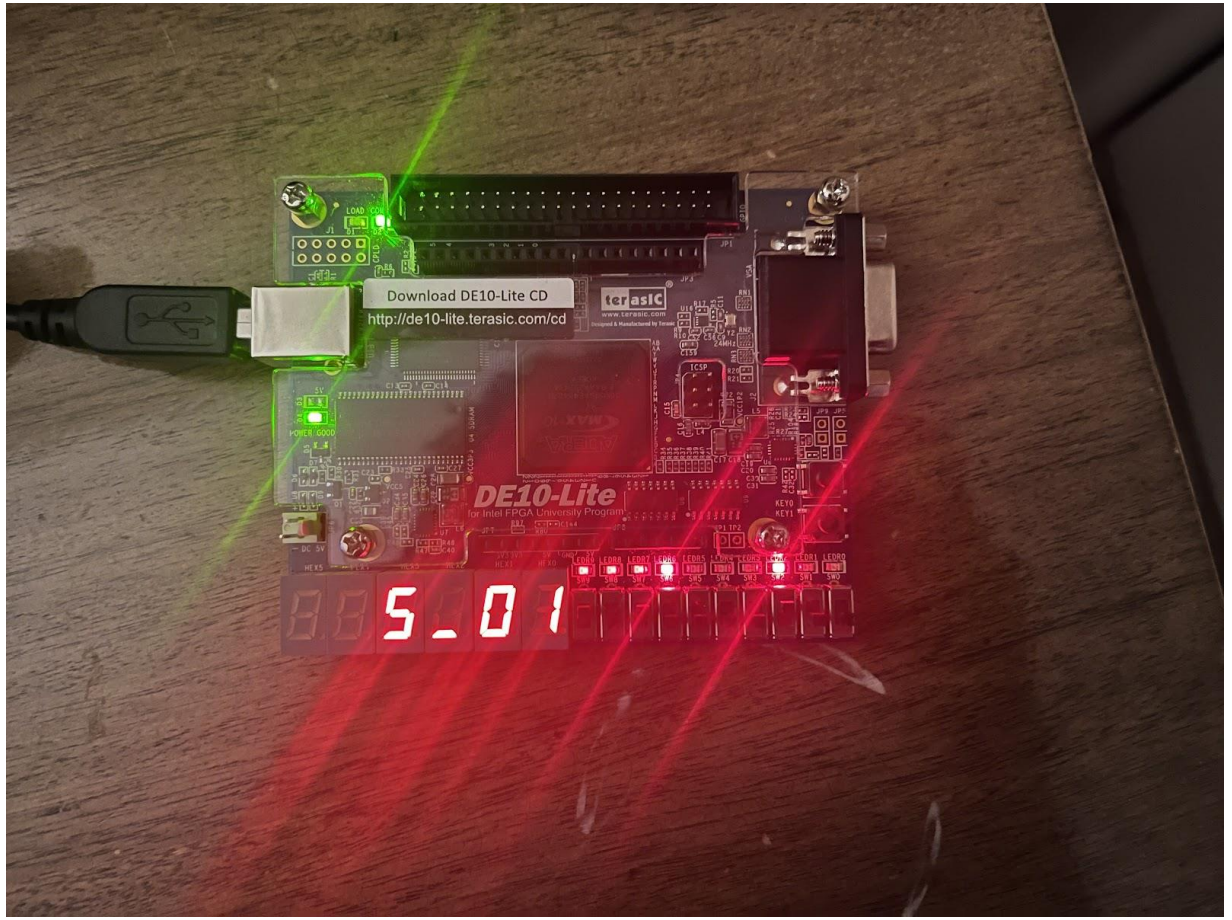



| Node Name | Direction | Location | I/O Bank | VREF Group | Fitter Location | I/O Standard | Reserved | Current Strength | Slew Rate | Differential Pair | Strict Preservation |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Key0 | Input | PIN_B8 | 7 | B7_N0 | PIN_B8 | 2.5 V | | 12mA (default) | | | |
| LED_SW[6] | Output | PIN_E14 | 7 | B7_N0 | PIN_E14 | 2.5 V | | 12mA (default) | 2 (default) | | |
| LED_SW[5] | Output | PIN_C13 | 7 | B7_N0 | PIN_C13 | 2.5 V | | 12mA (default) | 2 (default) | | |
| LED_SW[4] | Output | PIN_D13 | 7 | B7_N0 | PIN_D13 | 2.5 V | | 12mA (default) | 2 (default) | | |
| LED_SW[3] | Output | PIN_B10 | 7 | B7_N0 | PIN_B10 | 2.5 V | | 12mA (default) | 2 (default) | | |
| LED_SW[2] | Output | PIN_A10 | 7 | B7_N0 | PIN_A10 | 2.5 V | | 12mA (default) | 2 (default) | | |
| LED_SW[1] | Output | PIN_A9 | 7 | B7_N0 | PIN_A9 | 2.5 V | | 12mA (default) | 2 (default) | | |
| LED_SW[0] | Output | PIN_A8 | 7 | B7_N0 | PIN_A8 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG0[6] | Output | PIN_C17 | 7 | B7_N0 | PIN_C17 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG0[5] | Output | PIN_D17 | 7 | B7_N0 | PIN_D17 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG0[4] | Output | PIN_E16 | 7 | B7_N0 | PIN_E16 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG0[3] | Output | PIN_C16 | 7 | B7_N0 | PIN_C16 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG0[2] | Output | PIN_C15 | 7 | B7_N0 | PIN_C15 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG0[1] | Output | PIN_E15 | 7 | B7_N0 | PIN_E15 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG0[0] | Output | PIN_C14 | 7 | B7_N0 | PIN_C14 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG1[6] | Output | PIN_B17 | 7 | B7_N0 | PIN_B17 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG1[5] | Output | PIN_A18 | 7 | B7_N0 | PIN_A18 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG1[4] | Output | PIN_A17 | 7 | B7_N0 | PIN_A17 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG1[3] | Output | PIN_B16 | 7 | B7_N0 | PIN_B16 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG1[2] | Output | PIN_E18 | 6 | B6_N0 | PIN_E18 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG1[1] | Output | PIN_D18 | 6 | B6_N0 | PIN_D18 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG1[0] | Output | PIN_C18 | 7 | B7_N0 | PIN_C18 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG2[6] | Output | PIN_B22 | 6 | B6_N0 | PIN_B22 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG2[5] | Output | PIN_C22 | 6 | B6_N0 | PIN_C22 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG2[4] | Output | PIN_B21 | 6 | B6_N0 | PIN_B21 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG2[3] | Output | PIN_A21 | 6 | B6_N0 | PIN_A21 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG2[2] | Output | PIN_B19 | 7 | B7_N0 | PIN_B19 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG2[1] | Output | PIN_A20 | 7 | B7_N0 | PIN_A20 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG2[0] | Output | PIN_B20 | 6 | B6_N0 | PIN_B20 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG3[6] | Output | PIN_E17 | 6 | B6_N0 | PIN_E17 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG3[5] | Output | PIN_D19 | 6 | B6_N0 | PIN_D19 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG3[4] | Output | PIN_C20 | 6 | B6_N0 | PIN_C20 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG3[3] | Output | PIN_C19 | 7 | B7_N0 | PIN_C19 | 2.5 V | | 12mA (default) | 2 (default) | | |
| SEG3[2] | Output | PIN_E21 | 6 | B6_N0 | PIN_E21 | 2.5 V | | 12mA (default) | 2 (default) | | |

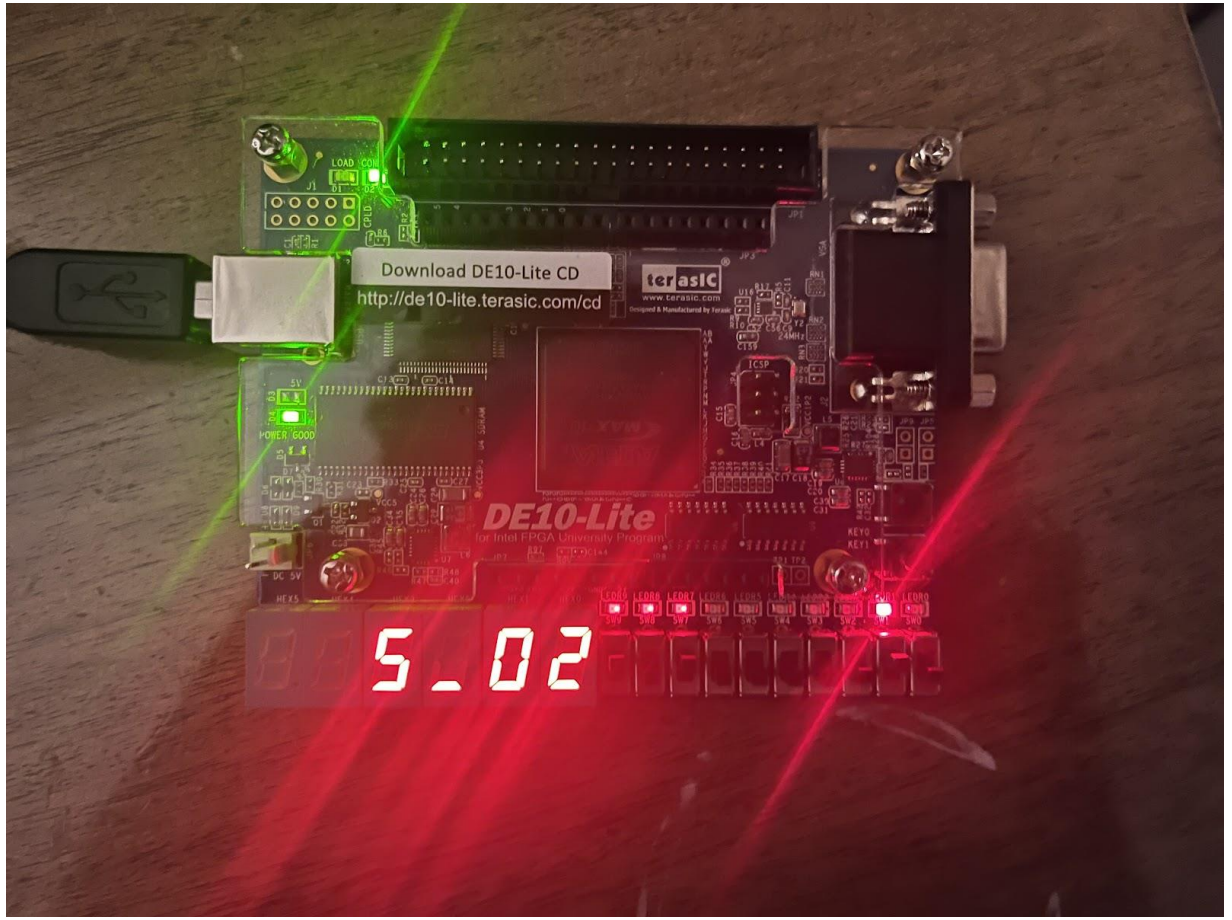
# FPGA Test SW0=1; Z=01; Step 1



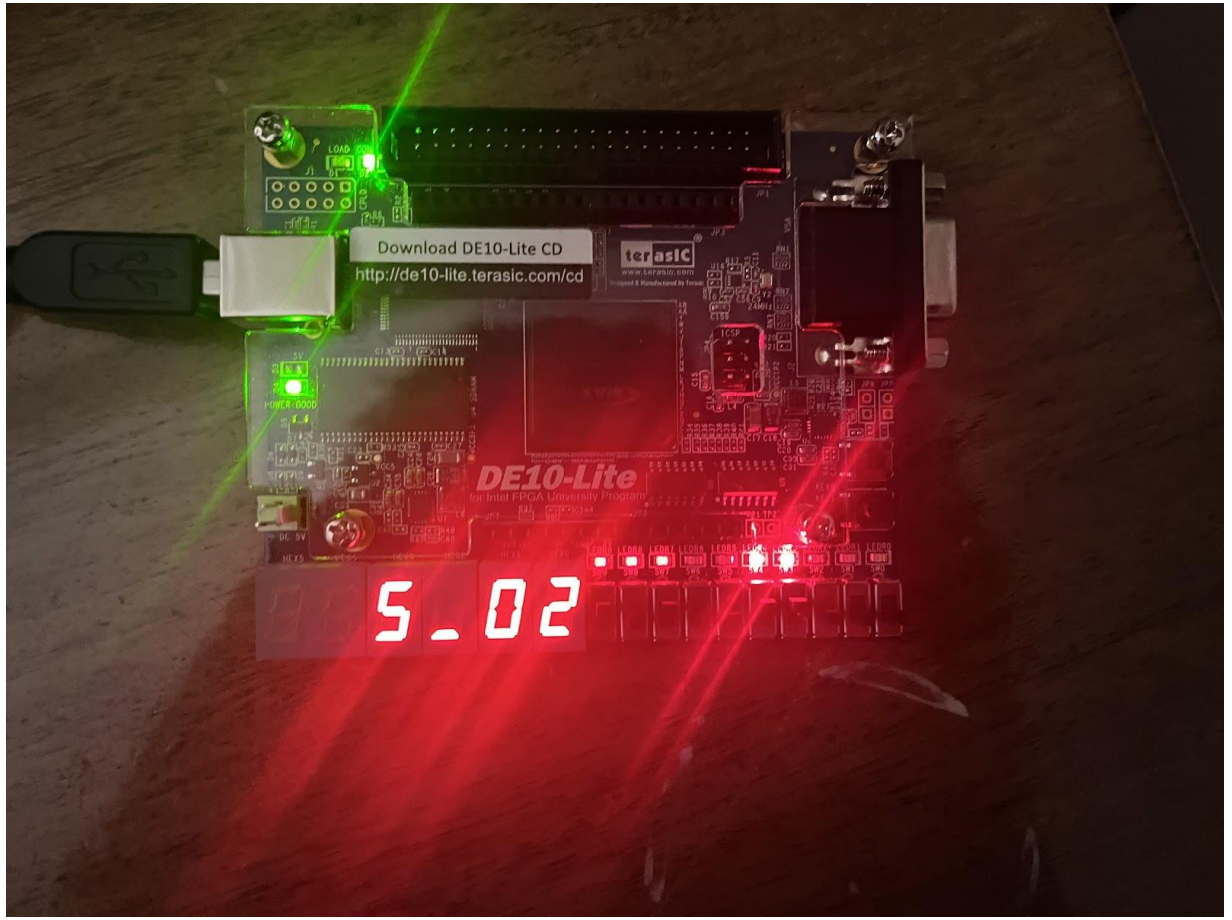
# FPGA Test SW2=1; Z=10 Step 2



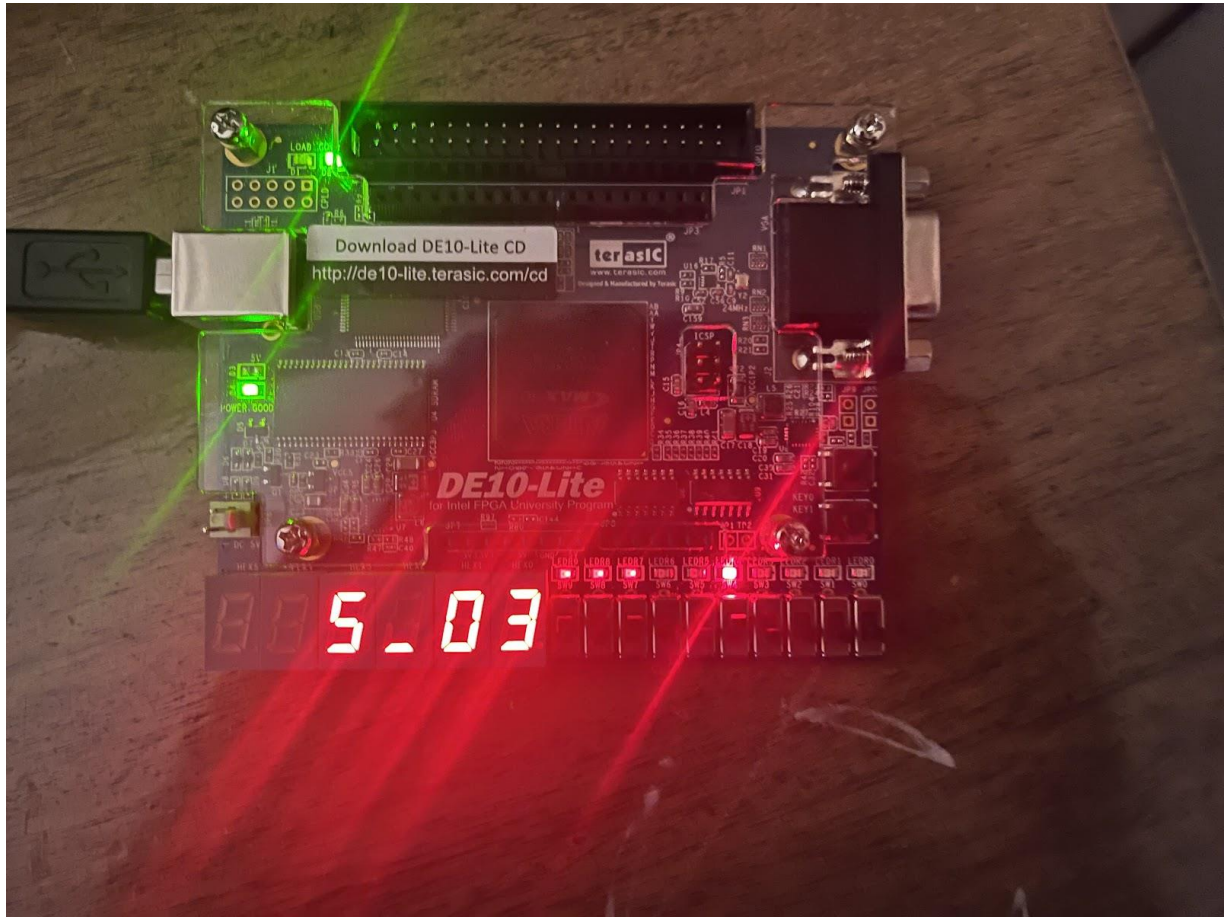
# FPGA Test SW1=1; Z=00 Step 3



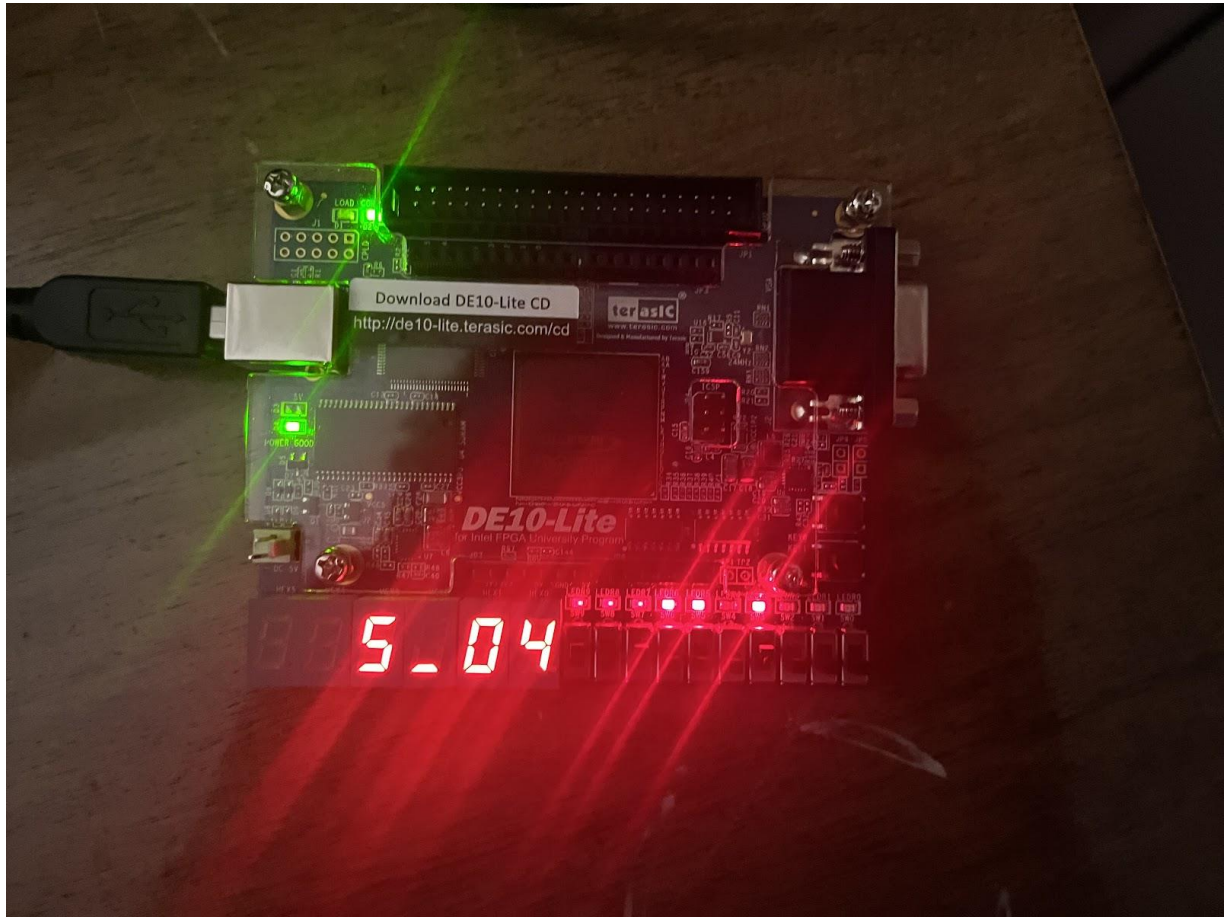
# FPGA test SW3&SW4 = 1; Z=00 Step 4



# FPGA Test SW4=1; Z=00 Step 5



# FPGA Test SW3=1; Z=11 Step 6



# FPGA Test SW4=1; Z=11 Step 7