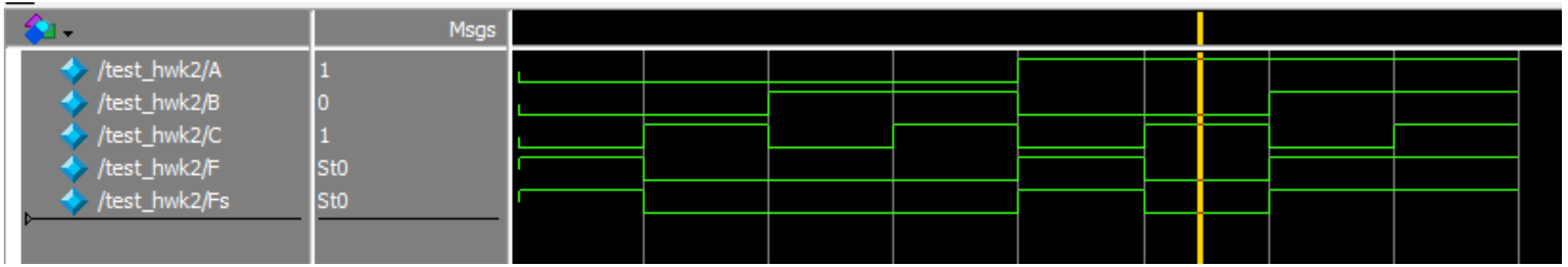
Homework 2 Problems

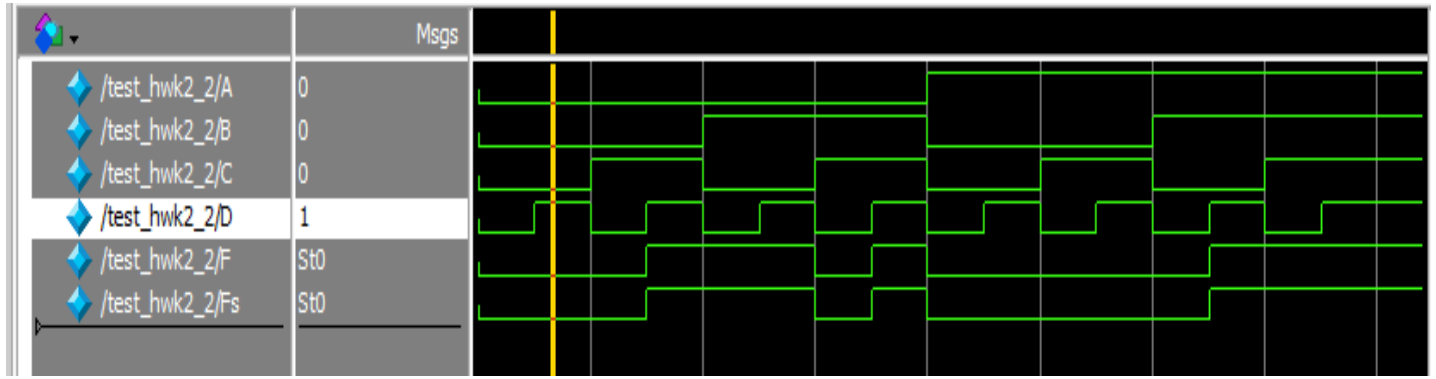
Pranav Nadimpalli

Problem 1



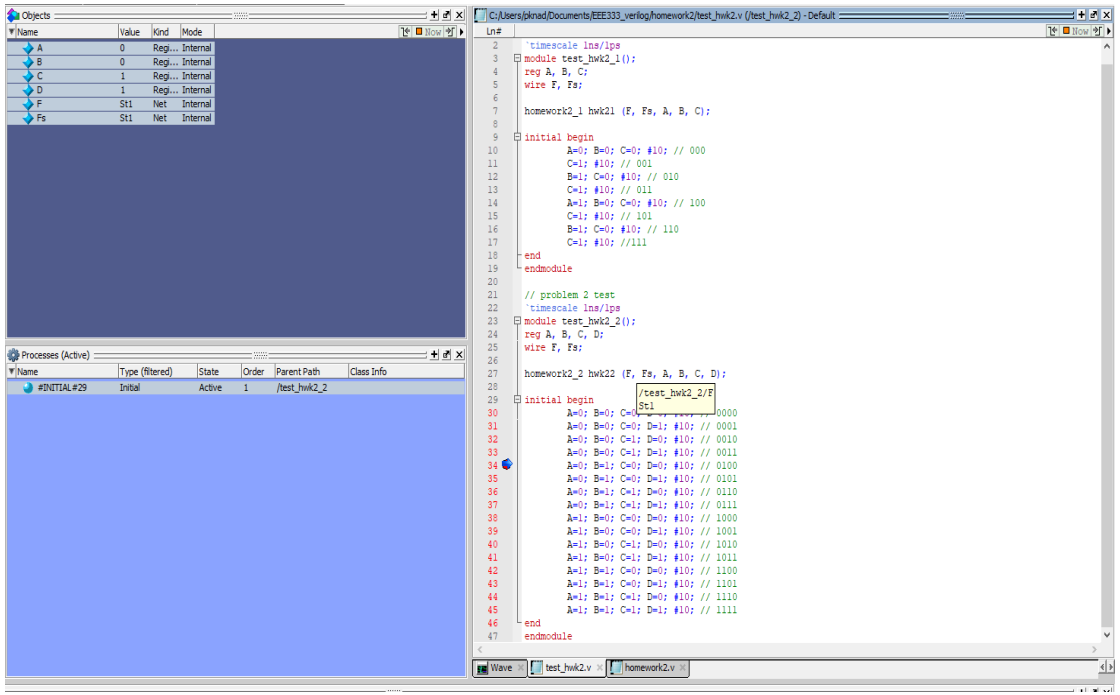
A	B	C	F	Fs
0	0	0	1	1
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	1	1
1	1	1	1	1

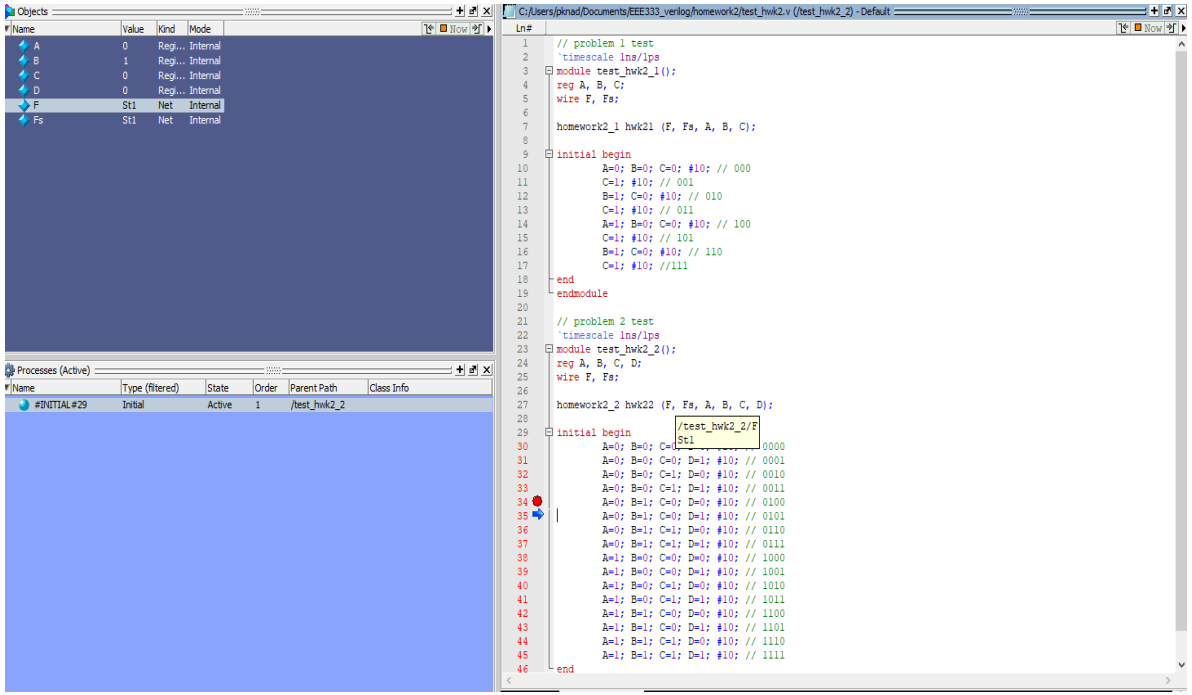
Problem 2



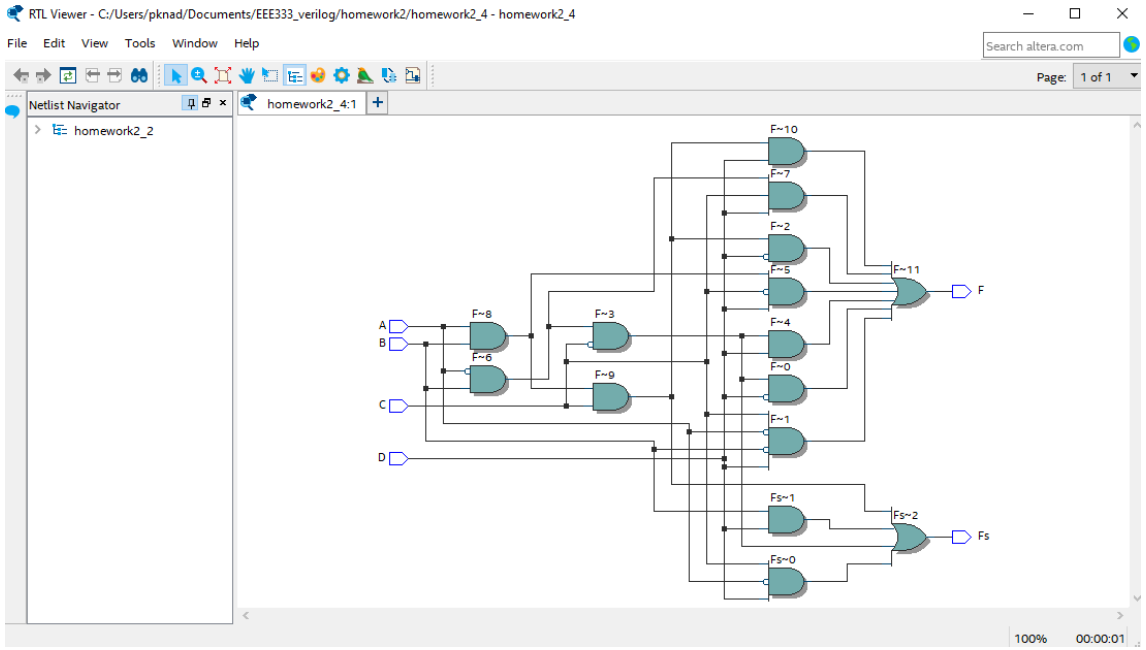
A	B	C	D	F	Fs
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	1	1
0	1	0	0	1	1
0	1	0	1	1	1
0	1	1	0	0	0
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	0	0
1	0	1	1	0	0
1	1	0	0	0	0
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

Problem 3


Objects
Name Value Kind Mode
A 0 Regi... Internal
B 0 Regi... Internal
C 1 Regi... Internal
D 1 Regi... Internal
F St1 Net Internal
Fs St1 Net Internal
Processes (Active)
Name Type (filtered) State Order Parent Path Class Info
#INITIAL#29 Initial Active 1 /test_hwk2_2
C:/Users/pknad/Documents/EEE333_verilog/homework2/test_hwk2.v (/test_hwk2_2) - Default
Ln#
`timescale 1ns/1ps
module test_hwk2_1();
reg A, B, C;
wire F, Fs;
homework2_1 hwk21 (F, Fs, A, B, C);
initial begin
A=0; B=0; C=0; #10; // 000
C=1; #10; // 001
B=1; C=0; #10; // 010
C=1; #10; // 011
A=1; B=0; C=0; #10; // 100
C=1; #10; // 101
B=1; C=0; #10; // 110
C=1; #10; //111
end
endmodule
// problem 2 test
`timescale 1ns/1ps
module test_hwk2_2();
reg A, B, C, D;
wire F, Fs;
homework2_2 hwk22 (F, Fs, A, B, C, D);
/test_hwk2_2/F
St1
initial begin
A=0; B=0; C=0; D=0; #10; // 0000
A=0; B=0; C=0; D=1; #10; // 0001
A=0; B=0; C=1; D=0; #10; // 0010
A=0; B=0; C=1; D=1; #10; // 0011
A=0; B=1; C=0; D=0; #10; // 0100
A=0; B=1; C=0; D=1; #10; // 0101
A=0; B=1; C=1; D=0; #10; // 0110
A=0; B=1; C=1; D=1; #10; // 0111
A=1; B=0; C=0; D=0; #10; // 1000
A=1; B=0; C=0; D=1; #10; // 1001
A=1; B=0; C=1; D=0; #10; // 1010
A=1; B=0; C=1; D=1; #10; // 1011
A=1; B=1; C=0; D=0; #10; // 1100
A=1; B=1; C=0; D=1; #10; // 1101
A=1; B=1; C=1; D=0; #10; // 1110
A=1; B=1; C=1; D=1; #10; // 1111
end
endmodule
Wave
test_hwk2.v
homework2.v


Objects
Name Value Kind Mode
A 0 Regi... Internal
B 1 Regi... Internal
C 0 Regi... Internal
D 0 Regi... Internal
F St1 Net Internal
Fs St1 Net Internal
Processes (Active)
Name Type (filtered) State Order Parent Path Class Info
#INITIAL#29 Initial Active 1 /test_hwk2_2
C:/Users/pknad/Documents/EEE333_verilog/homework2/test_hwk2.v (/test_hwk2_2) - Default
Ln#
// problem 1 test
`timescale 1ns/1ps
module test_hwk2_1();
reg A, B, C;
wire F, Fs;
homework2_1 hwk21 (F, Fs, A, B, C);
initial begin
A=0; B=0; C=0; #10; // 000
C=1; #10; // 001
B=1; C=0; #10; // 010
C=1; #10; // 011
A=1; B=0; C=0; #10; // 100
C=1; #10; // 101
B=1; C=0; #10; // 110
C=1; #10; //111
end
endmodule
// problem 2 test
`timescale 1ns/1ps
module test_hwk2_2();
reg A, B, C, D;
wire F, Fs;
homework2_2 hwk22 (F, Fs, A, B, C, D);
/test_hwk2_2/F
St1
initial begin
A=0; B=0; C=0; D=0; #10; // 0000
A=0; B=0; C=0; D=1; #10; // 0001
A=0; B=0; C=1; D=0; #10; // 0010
A=0; B=0; C=1; D=1; #10; // 0011
A=0; B=1; C=0; D=0; #10; // 0100
A=0; B=1; C=0; D=1; #10; // 0101
A=0; B=1; C=1; D=0; #10; // 0110
A=0; B=1; C=1; D=1; #10; // 0111
A=1; B=0; C=0; D=0; #10; // 1000
A=1; B=0; C=0; D=1; #10; // 1001
A=1; B=0; C=1; D=0; #10; // 1010
A=1; B=0; C=1; D=1; #10; // 1011
A=1; B=1; C=0; D=0; #10; // 1100
A=1; B=1; C=0; D=1; #10; // 1101
A=1; B=1; C=1; D=0; #10; // 1110
A=1; B=1; C=1; D=1; #10; // 1111
end
endmodule

Problem 4


RTL Viewer - C:/Users/pknad/Documents/EEE333_verilog/homework2/homework2_4 - homework2_4
File Edit View Tools Window Help
Search altera.com
Page: 1 of 1
Netlist Navigator
homework2_2
homework2_4:1
A
B
C
D
F~8
F~3
F~6
F~9
F~10
F~7
F~2
F~5
F~11
F
F~4
F~0
F~1
Fs~1
Fs~2
Fs
Fs~0
100%
00:00:01

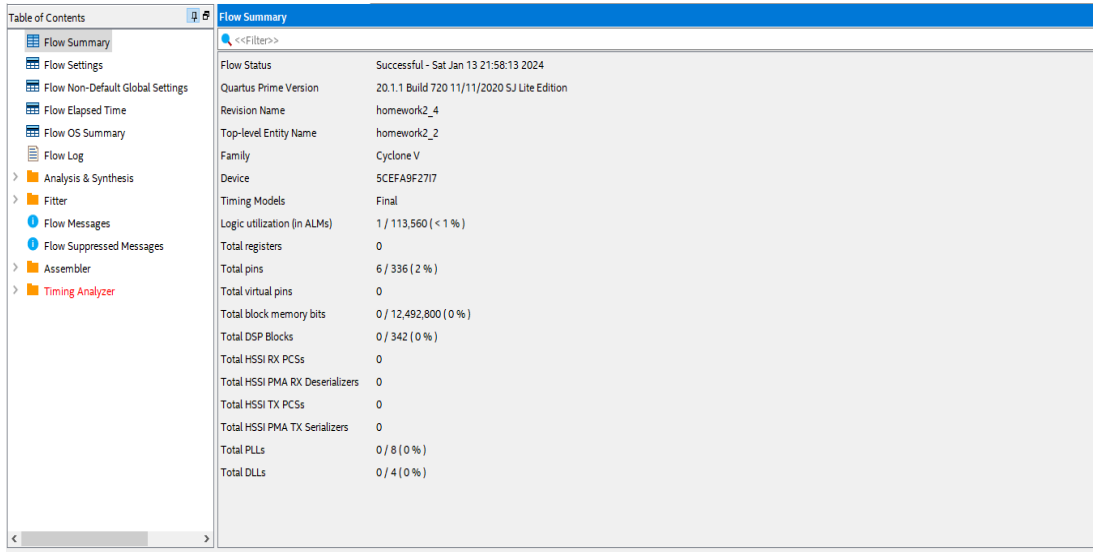


Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Global Settings
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Flow Messages
Flow Suppressed Messages
Assembler
Timing Analyzer
Flow Summary
<<Filter>>
Flow Status Successful - Sat Jan 13 21:58:13 2024
Quartus Prime Version 20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name homework2_4
Top-level Entity Name homework2_2
Family Cyclone V
Device 5CEFA9F27I7
Timing Models Final
Logic utilization (in ALMs) 1 / 113,560 (< 1 %)
Total registers 0
Total pins 6 / 336 (2 %)
Total virtual pins 0
Total block memory bits 0 / 12,492,800 (0 %)
Total DSP Blocks 0 / 342 (0 %)
Total HSSI RX PCSs 0
Total HSSI PMA RX Deserializers 0
Total HSSI TX PCSs 0
Total HSSI PMA TX Serializers 0
Total PLLs 0 / 8 (0 %)
Total DLLs 0 / 4 (0 %)