Homework 5

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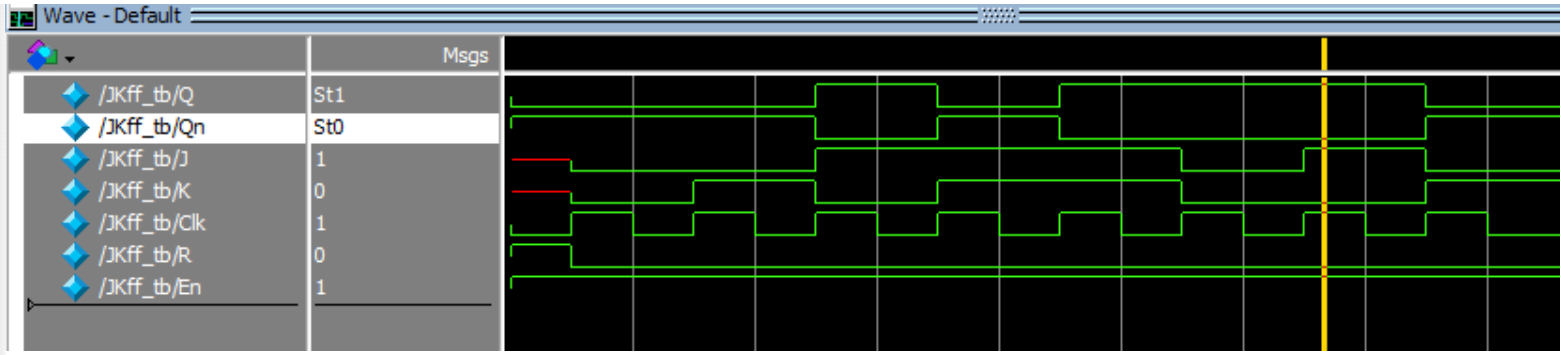
SR Testing Waveform + Transcript

```
run
# Time  Clk     En      S       R       Q       Qn
run
# 20    1       1       0       0       0       1
run
# 30    0       1       0       0       0       1
run
# 40    1       1       1       0       1       0
run
# 50    0       1       1       0       1       0
run
# 60    1       1       0       1       0       1
run
# 70    0       1       0       1       0       1
run
# 80    1       1       1       1       x       x
run
# 90    0       1       1       1       x       x
run
# 100   1       1       1       0       1       0
run
# 110   0       1       1       0       1       0
run
# 120   1       1       1       0       1       0
run
# 130   0       1       1       0       1       0
run
# 140   1       1       0       0       1       0
run
# 150   0       1       0       0       1       0
run
# 160   1       1       0       1       0       1
run
# 170   0       1       0       1       0       1
run
# 180   1       1       1       0       1       0
run
# 190   0       1       1       0       1       0
run
# 200   1       1       1       1       x       x
VSIM 43> run
# 210   0       1       1       1       x       x

VSIM 43>
```

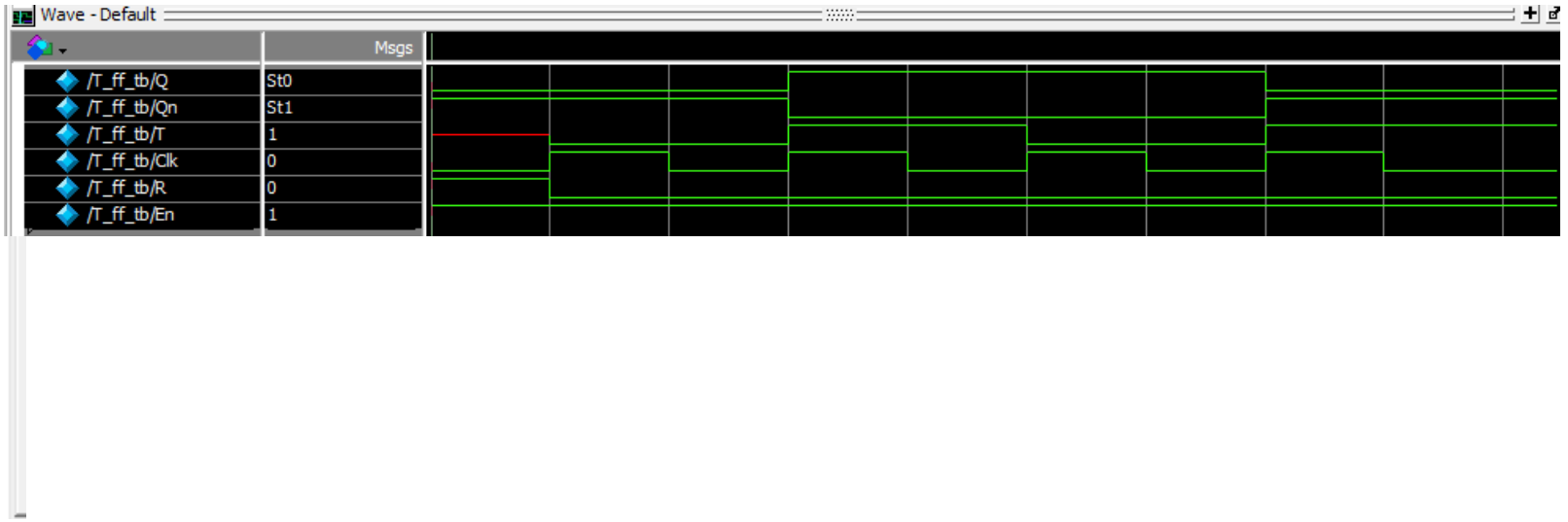
JK Testing Waveform + Transcript

```
VSIM 52> run
# Time   J       K       R       Q       Qn
run
# 10     0       0       0       0       1
run
run
# 30     0       1       0       0       1
run
run
# 50     1       0       0       1       0
run
run
# 70     1       1       0       0       1
run
run
# 90     1       1       0       1       0
run
run
# 110    0       0       0       1       0
run
run
# 130    1       0       0       1       0
run
run
# 150    0       1       0       0       1
run
run
run
run
VSIM 53> run
```



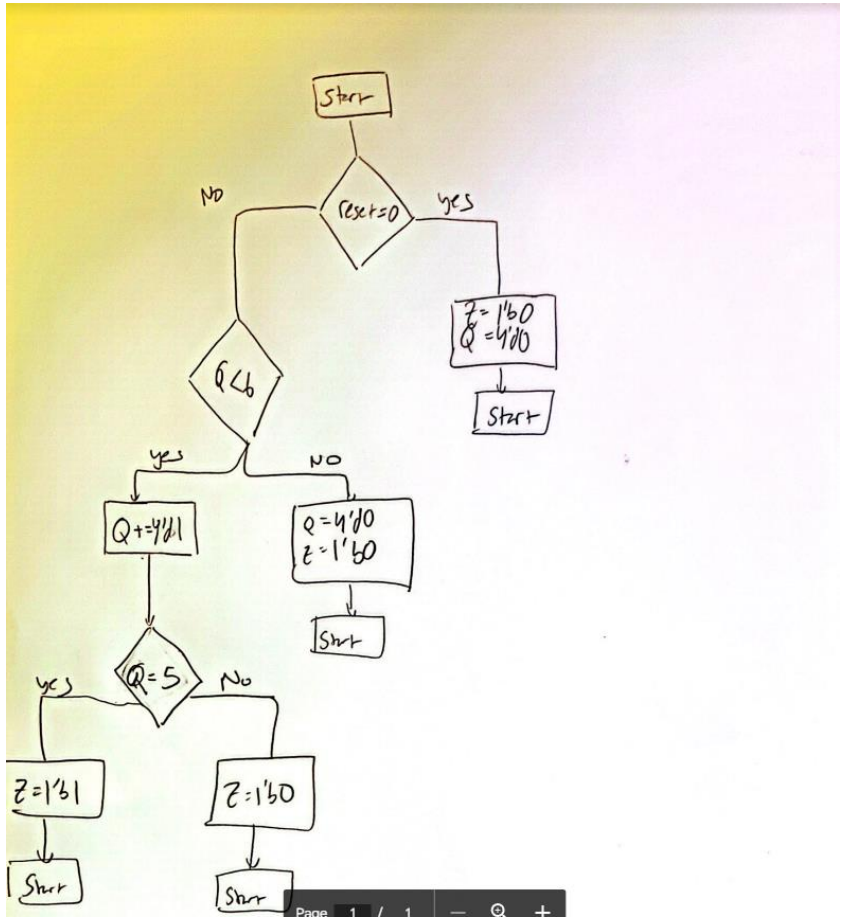
T Testing Waveform + Transcript

```
add wave -position end  sim:/T_ff_tb/En
VSIM 61> run
# Time  T       Q*      Qn*
run
# 10    0       0       1
run
run
# 30    1       1       0
run
run
# 50    0       1       0
run
run
# 70    1       0       1
run
run
VSIM 62> run
```



Problem 6 Flow Diagram

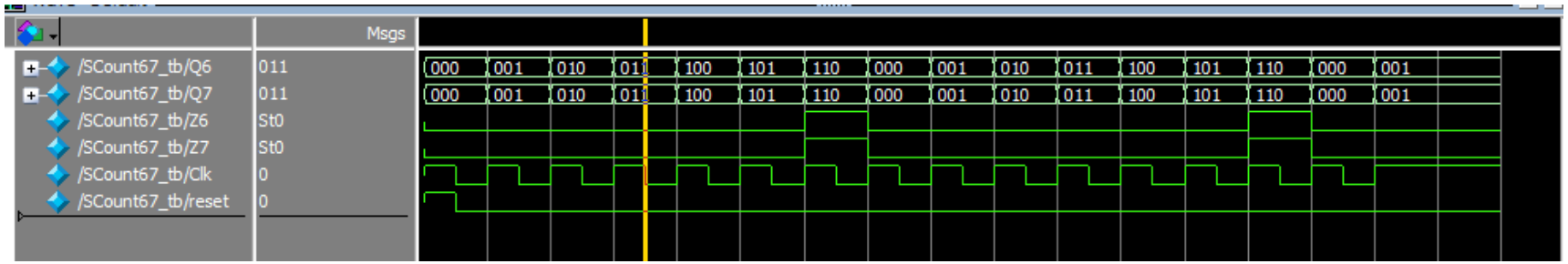
We evaluate Q=5 so we can get Z=1'b1 output when Q=6



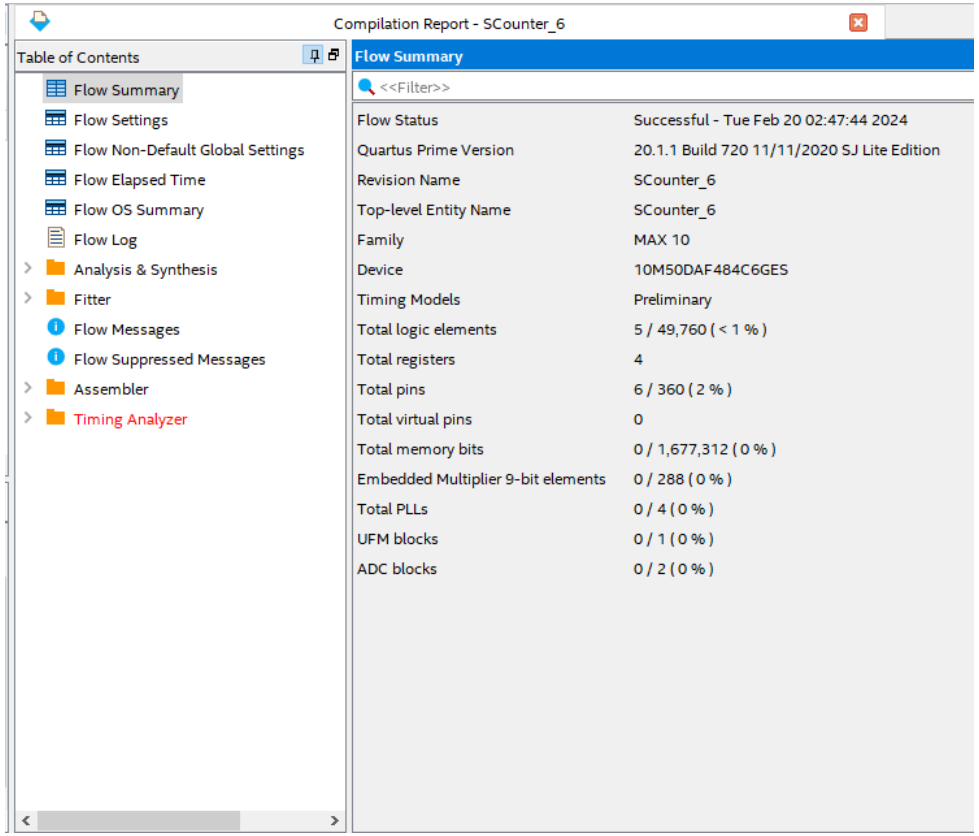
Waveforms & Transcript for Problem 6 and 7

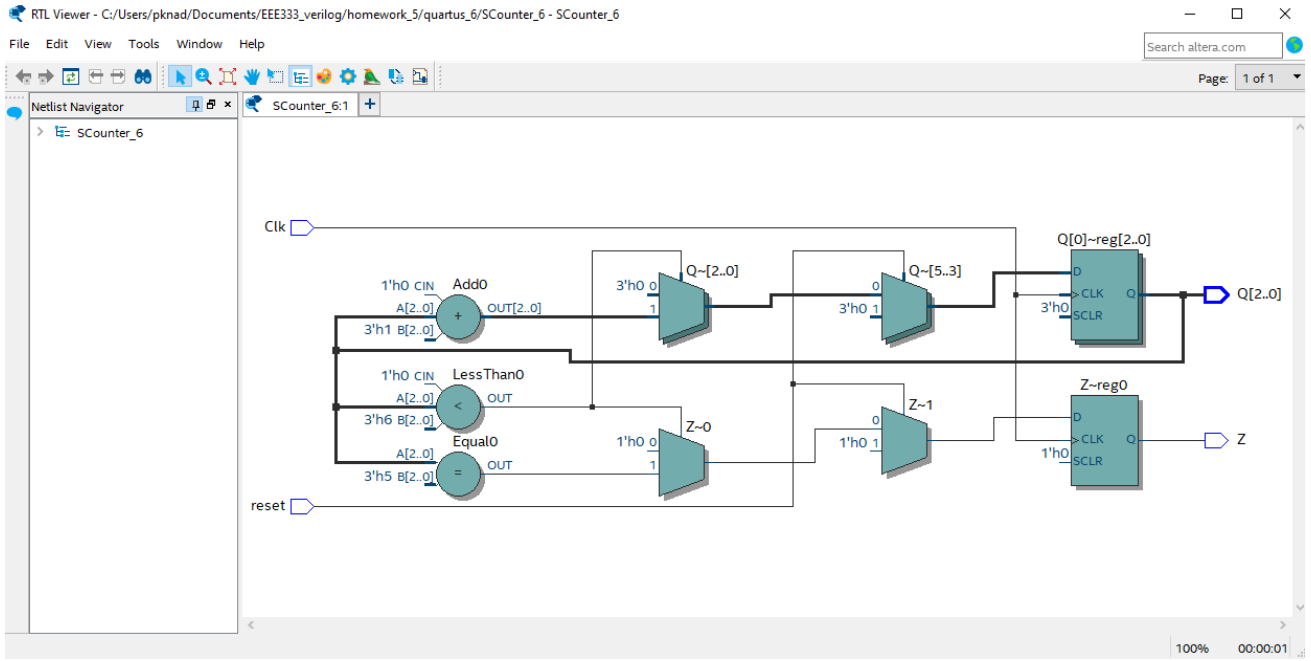
Q6 and Z6 correspond to output for problem 6
Q7 and Z7 correspond to output for problem 7

```
run
# Time=              10000, Q6=0, Z6=0, Q7=0, Z7=0
run
# Time=              20000, Q6=1, Z6=0, Q7=1, Z7=0
run
run
# Time=              40000, Q6=2, Z6=0, Q7=2, Z7=0
run
run
# Time=              60000, Q6=3, Z6=0, Q7=3, Z7=0
run
run
# Time=              80000, Q6=4, Z6=0, Q7=4, Z7=0
run
run
# Time=             100000, Q6=5, Z6=0, Q7=5, Z7=0
run
run
# Time=             120000, Q6=6, Z6=1, Q7=6, Z7=1
run
run
# Time=             140000, Q6=0, Z6=0, Q7=0, Z7=0
run
run
# Time=             160000, Q6=1, Z6=0, Q7=1, Z7=0
run
run
# Time=             180000, Q6=2, Z6=0, Q7=2, Z7=0
run
run
# Time=             200000, Q6=3, Z6=0, Q7=3, Z7=0
run
run
# Time=             220000, Q6=4, Z6=0, Q7=4, Z7=0
run
run
# Time=             240000, Q6=5, Z6=0, Q7=5, Z7=0
run
run
# Time=             260000, Q6=6, Z6=1, Q7=6, Z7=1
run
run
# Time=             280000, Q6=0, Z6=0, Q7=0, Z7=0
run
run
# Time=             300000, Q6=1, Z6=0, Q7=1, Z7=0
run
```



Problem 6 RTL Netlist + Flow Diagram





Problem 7 RTL Netlist + Flow Diagram

Compilation Report - SCounter_7

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- Timing Analyzer

Flow Summary

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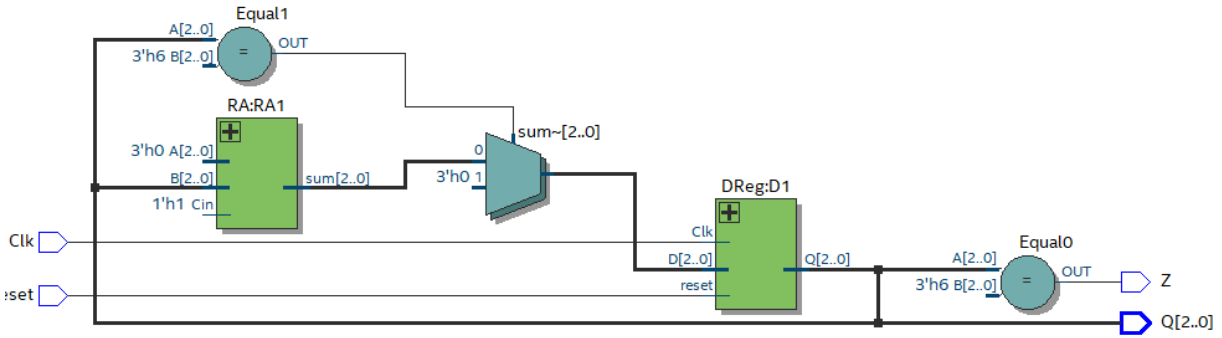
Flow Status	Successful - Tue Feb 20 02:53:05 2024
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	SCounter_7
Top-level Entity Name	SCounter_7
Family	MAX 10
Device	10M50DAF484C6GES
Timing Models	Preliminary
Total logic elements	5 / 49,760 (< 1 %)
Total registers	3
Total pins	6 / 360 (2 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)



Problem 9 Questions

a) Some of the differences between the two designs based on the RTL netlist is that the design in problem 6 uses many more muxes and uses its own implementation for the addition. The design from problem 7 uses fewer muxes but relies more heavily from our own implementation of the D Register and the Ripple Adder. Based on the Flow Summary the only difference is the number of registers used Problem 7 uses 1 less than the problem 6 design.
b) Problem 6 design used 4 registers and the problem 7 design only used 3
c) Both of the designs used 5 logical elements
d) I think the design from problem 7 is the best. Not only does it use fewer registers because it relies on our implementation of the ripple adder and D Register we can expect the performance and implementation to be similar across various different types of FPGAs.