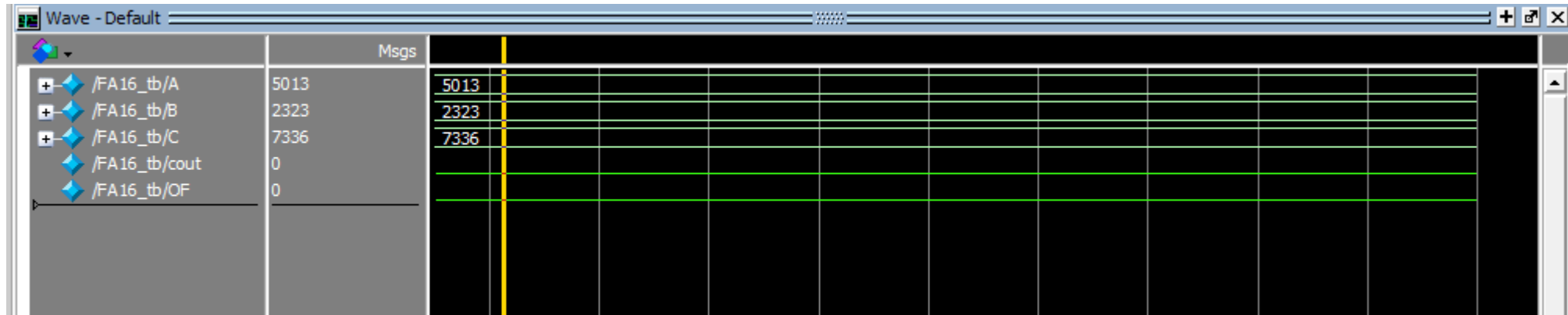


# Homework 9

Pranav Nadimpalli

# Problem 2 Test Bench Wave Form



# Problem 3

- Synchronous
  - Control
  - W Register
  - 16 8-bit registers
  - PC
- Combinatorial
  - Instruction Memory
  - Instruction Register
  - ALU
  - Next Addr

# Problem 4

```
332140 No Setup paths to report
332140 No Hold paths to report
332140 No Recovery paths to report
332140 No Removal paths to report
332140 No Minimum Pulse width paths to report
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
> 332102 Quartus Prime Timing Analyzer was successful. 0 errors, 6 warnings
332102 293000 Quartus Prime Full Compilation was successful. 0 errors, 20 warnings
```

# Problem 5

```
293000 332140 No Hold paths to report
293000 332140 No Recovery paths to report
293000 332140 No Removal paths to report
293000 332148 Timing requirements not met
293000 332146 worst-case minimum pulse width slack is -3.000
293000 332102 Design is not fully constrained for setup requirements
293000 332102 Design is not fully constrained for hold requirements
293000      Quartus Prime Timing Analyzer was successful. 0 errors, 6 warnings
293000 293000 Quartus Prime Full Compilation was successful. 0 errors, 15 warnings
```

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