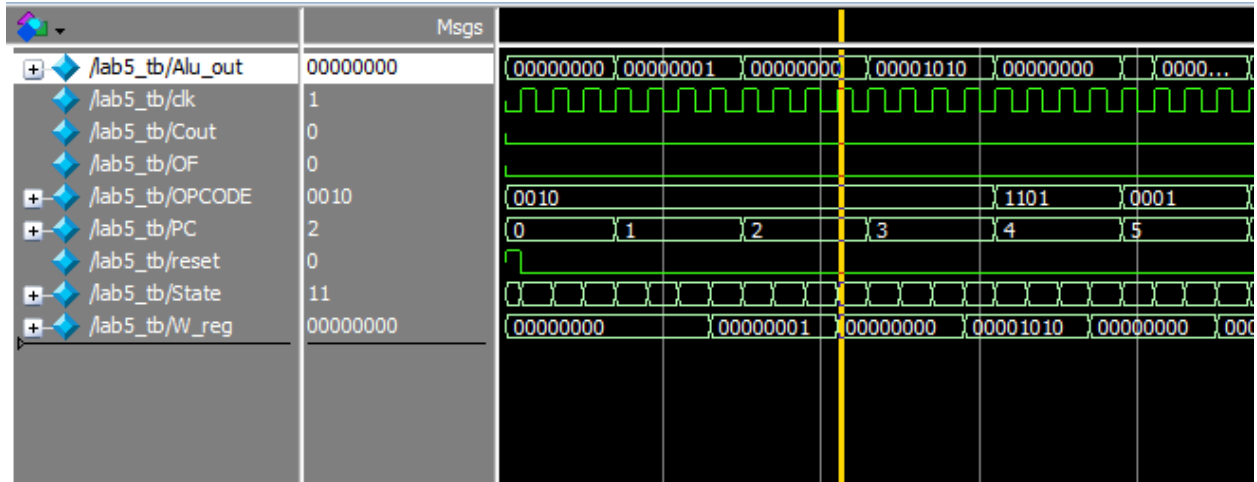


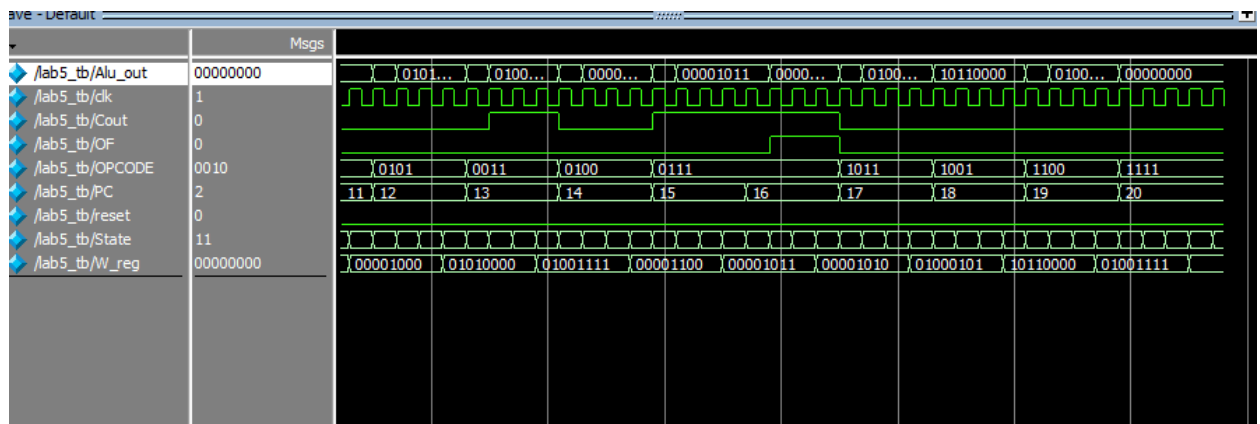
3. CSV values in a file called test1.csv

4.

First 5 values of PC for the simulated MCU



Last 5 values of PC for the simulated MCU



6. Pin Planner

Pin Planner - C:\Users\pknad\Documents\EEE333_verilog\lab5\Quartus\lab5_pv - lab5_pv

File Edit View Processing Tools Window Help

Report not available

Top View - Wire Bond
MAX 10 - 10M50DAF484C6GES

Pin Legend

- Symbol Pin Type
- User I/O
- User assigned I...
- Fitter assigned L...
- Unbonded pad
- Reserved pin
- Other configura...
- DEV_DE
- DEV_CLR
- DIFF_n
- DIFF_p
- DQ
- DQS
- DQSB
- CLK_n
- CLK_p
- Other PLL
- Other dual purp...
- TDI
- TCK
- TMS
- TDO
- VREF
- VCCP/VCCB/V...
- VCCA
- VCCINT
- VCCIO
- VCCIO2

Groups Report

Tasks

- Early Pin Planning...
 - Early Pin Planning...
 - Run I/O Assignment Analysis...
 - Export Pin Assignments...
- Pin Finder...
 - Highlight Pins
 - I/O Banks
 - VREF Groups
 - Edges

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	Strict Preservation
SevSeg[2]	Output	PH_E19	6	B6_NO	PH_E19	2.5 V		12mA (default)	2 (default)		
SevSeg[1]	Output	PH_E20	6	B6_NO	PH_E20	2.5 V		12mA (default)	2 (default)		
SevSeg[0]	Output	PH_F18	6	B6_NO	PH_F18	2.5 V		12mA (default)	2 (default)		
SevSeg[5]	Output	PH_N20	6	B6_NO	PH_N20	2.5 V		12mA (default)	2 (default)		
SevSeg[3]	Output	PH_N19	6	B6_NO	PH_N19	2.5 V		12mA (default)	2 (default)		
SevSeg[4]	Output	PH_M20	6	B6_NO	PH_M20	2.5 V		12mA (default)	2 (default)		
SevSeg[2]	Output	PH_N18	6	B6_NO	PH_N18	2.5 V		12mA (default)	2 (default)		
SevSeg[2]	Output	PH_L18	6	B6_NO	PH_L18	2.5 V		12mA (default)	2 (default)		
SevSeg[1]	Output	PH_K20	6	B6_NO	PH_K20	2.5 V		12mA (default)	2 (default)		
SevSeg[0]	Output	PH_J20	6	B6_NO	PH_J20	2.5 V		12mA (default)	2 (default)		
clk	Input	PH_P11	3	B5_NO	PH_P11	2.5 V		12mA (default)	2 (default)		
<<new node>>											

Filter: Pins: all

0% 00:00:00

7. Board Programmed & Flow Summary

Programmer - C:\Users\pknad\Documents\EEE333_verilog\lab5\Quartus\lab5_pv - lab5_pv - [lab5_pv.cdf]*

File Edit View Processing Tools Window Help

Hardware Setup... USB-Blaster [USB-0] Mode: JTAG Progress: 100% (Successful)

☐ Enable real-time ISP to allow background programming when available

File	Device	Checksum	Usercode	Program/Configure	Verify	Blank-Check	Examine	Security Bit	Erase	ISP CLAMP
output_files/lab5_pv.sof	10M50DAF484C6...	0031253A	0031253A	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Start Stop Auto Detect Delete Add File... Change File... Save File Add Device... Up Down

TDI

10M50DAF484ES

TDO

Table of Contents	
Flow Summary	
Flow Settings	
Flow Non-Default Global Settings	
Flow Elapsed Time	
Flow OS Summary	
Flow Log	
Analysis & Synthesis	
Fitter	
Flow Messages	
Flow Suppressed Messages	
Assembler	
Timing Analyzer	

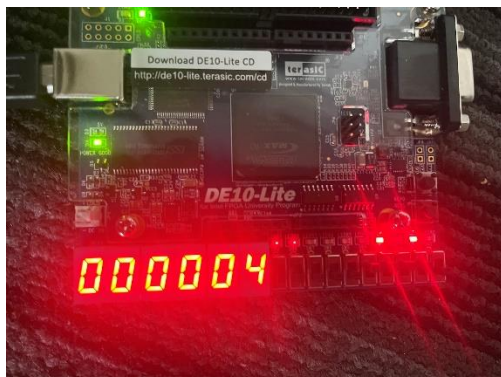
Flow Summary	
Flow Status	Successful - Fri Apr 26 17:22:30 2024
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	lab5_pv
Top-level Entity Name	lab5_pv
Family	MAX 10
Device	10M50DAF484C6GES
Timing Models	Preliminary
Total logic elements	1,132 / 49,760 (2 %)
Total registers	189
Total pins	57 / 360 (16 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	1 / 288 (< 1 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

8. Images For PC Address: 10

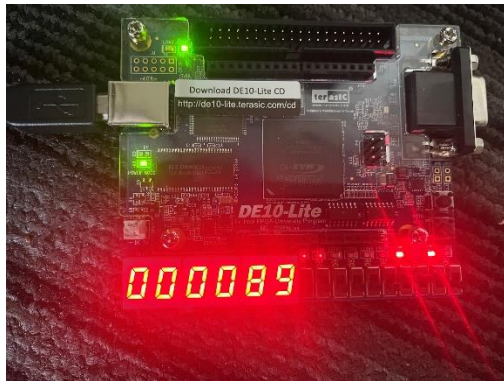
PC Address (PC 10):



OPCODE:

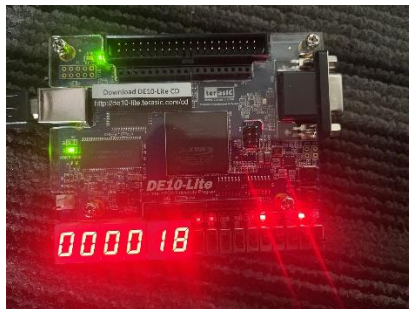


ALUOUT:

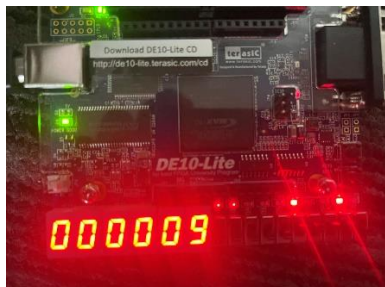


Images for PC Address: 18

PC Address:



OPCODE:

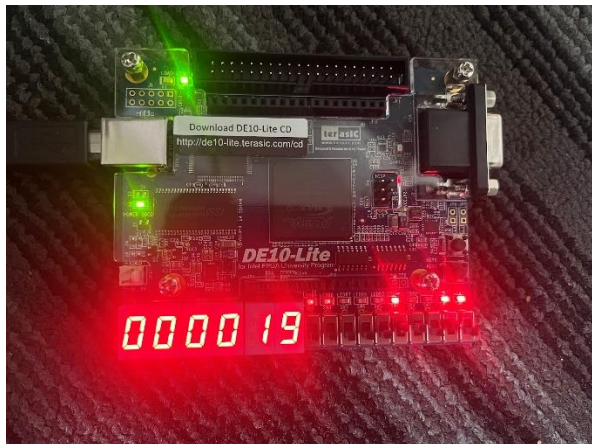


ALUOUT:

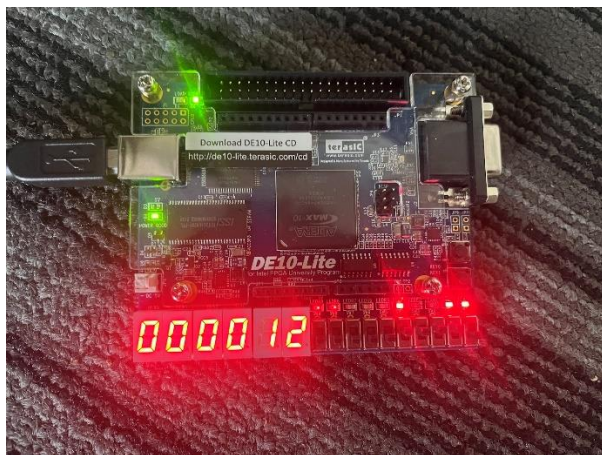


Images for PC Address: 19

PC Address:



OPCODE:

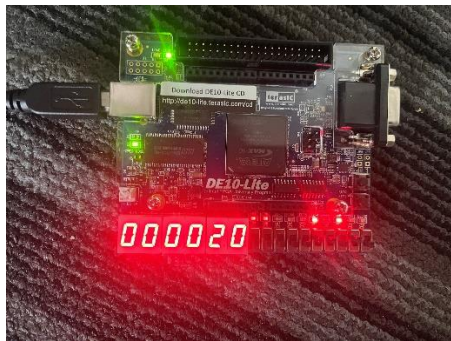


ALUOUT:

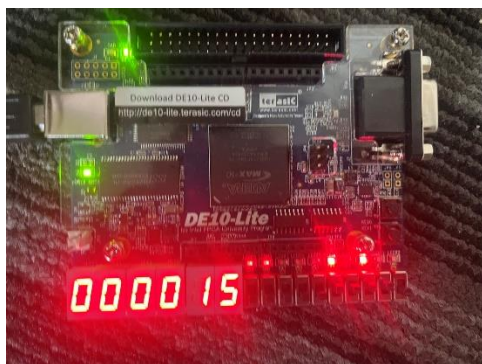


Images for PC Address: 20

PC Address:



OPCODE:



ALUOUT:

