Computer Organization and Architecture Laboratory

Assignment 3

Group 55:-

Kulkarni Pranav Suryakant - 20CS30029
Vineet Amol Pippal - 20CS30058

Question 1

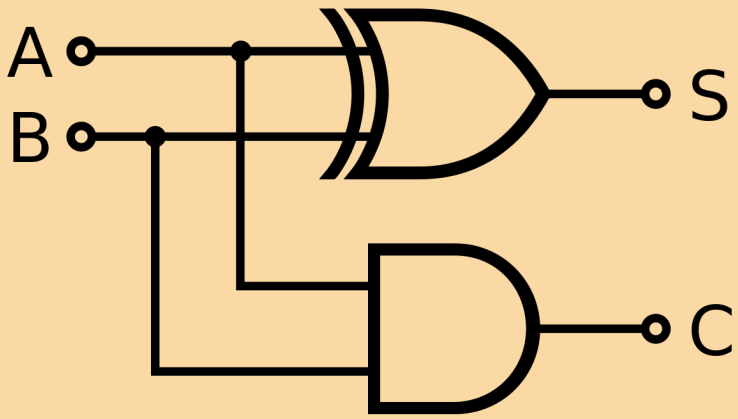
a). Half Adder

A Half Adder takes two bits (a and b) as input and gives the sum bit, s and the carry-out bit, c as output.

Truth Table for Half Adder:

a	b	s	c
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

- Circuit Diagram:



- The boolean expressions for Sum and Carry bit can be deduced using the truth table:

Sum = A XOR B
Carry = A AND B

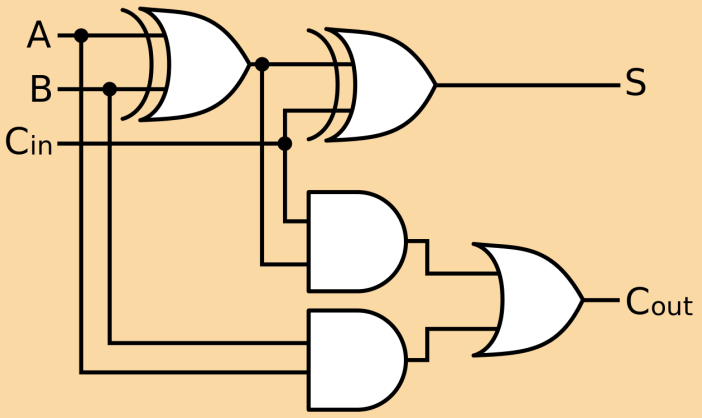
b). Full Adder

A Full Adder takes three bits (a, b and carry-in bit c_0) as input and gives the sum, s and the carry, c as output.

Truth Table for Full Adder:

a	b	c_0	s	c
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

- Circuit Diagram:



- The boolean expressions for Sum and Carry bit can be deduced using the truth table:

Sum = Cin XOR (A XOR B)
Carry = A AND B + Cin AND (A XOR B)

c). Longest Delays in the circuits

1. 64 Bit Full Adder:
   Net Delay: 22.343ns
   Logic Delay: 2.969ns
   Route Delay: 18.374ns

```
                          Gate     Net
Cell:in->out      fanout  Delay    Delay  Logical Name (Net Name)
----------------------------------------  ------------
 IBUF:I->O             2   0.001   0.925  a_1_IBUF (a_1_IBUF)
 LUT5:I0->O            3   0.124   0.550  s1/s1/s1/f2/cout1 (s1/s1/s1/tempCarry<1>)
 LUT5:I3->O            3   0.124   0.550  s1/s1/s1/f4/cout1 (s1/s1/s1/tempCarry<3>)
 LUT5:I3->O            3   0.124   0.550  s1/s1/s1/f6/cout1 (s1/s1/s1/tempCarry<5>)
 LUT5:I3->O            3   0.124   0.550  s1/s1/s1/f8/cout1 (s1/s1/tempCarry)
 LUT5:I3->O            3   0.124   0.550  s1/s1/s2/f2/cout1 (s1/s1/s2/tempCarry<1>)
 LUT5:I3->O            3   0.124   0.550  s1/s1/s2/f4/cout1 (s1/s1/s2/tempCarry<3>)
 LUT5:I3->O            3   0.124   0.550  s1/s1/s2/f6/cout1 (s1/s1/s2/tempCarry<5>)
 LUT5:I3->O            3   0.124   0.550  s1/s1/s2/f8/cout1 (s1/tempCarry)
 LUT5:I3->O            3   0.124   0.550  s1/s2/s1/f2/cout1 (s1/s2/s1/tempCarry<1>)
 LUT5:I3->O            3   0.124   0.550  s1/s2/s1/f4/cout1 (s1/s2/s1/tempCarry<3>)
 LUT5:I3->O            3   0.124   0.550  s1/s2/s1/f6/cout1 (s1/s2/s1/tempCarry<5>)
 LUT5:I3->O            3   0.124   0.550  s1/s2/s1/f8/cout1 (s1/s2/tempCarry)
 LUT5:I3->O            3   0.124   0.550  s1/s2/s2/f2/cout1 (s1/s2/s2/tempCarry<1>)
 LUT5:I3->O            3   0.124   0.550  s1/s2/s2/f4/cout1 (s1/s2/s2/tempCarry<3>)
 LUT5:I3->O            3   0.124   0.550  s1/s2/s2/f6/cout1 (s1/s2/s2/tempCarry<5>)
 LUT5:I3->O            3   0.124   0.550  s1/s2/s2/f8/cout1 (tempCarry)
 LUT5:I3->O            3   0.124   0.550  s2/s1/s1/f2/cout1 (s2/s1/s1/tempCarry<1>)
 LUT5:I3->O            3   0.124   0.550  s2/s1/s1/f4/cout1 (s2/s1/s1/tempCarry<3>)
 LUT5:I3->O            3   0.124   0.550  s2/s1/s1/f6/cout1 (s2/s1/s1/tempCarry<5>)
 LUT5:I3->O            3   0.124   0.550  s2/s1/s1/f8/cout1 (s2/s1/tempCarry)
 LUT5:I3->O            3   0.124   0.550  s2/s1/s2/f2/cout1 (s2/s1/s2/tempCarry<1>)
 LUT5:I3->O            3   0.124   0.550  s2/s1/s2/f4/cout1 (s2/s1/s2/tempCarry<3>)
 LUT5:I3->O            3   0.124   0.550  s2/s1/s2/f6/cout1 (s2/s1/s2/tempCarry<5>)
 LUT5:I3->O            3   0.124   0.550  s2/s1/s2/f8/cout1 (s2/tempCarry)
 LUT5:I3->O            3   0.124   0.550  s2/s2/s1/f2/cout1 (s2/s2/s1/tempCarry<1>)
 LUT5:I3->O            3   0.124   0.550  s2/s2/s1/f4/cout1 (s2/s2/s1/tempCarry<3>)
 LUT5:I3->O            3   0.124   0.550  s2/s2/s1/f6/cout1 (s2/s2/s1/tempCarry<5>)
 LUT5:I3->O            3   0.124   0.550  s2/s2/s1/f8/cout1 (s2/s2/tempCarry)
 LUT5:I3->O            3   0.124   0.550  s2/s2/s2/f2/cout1 (s2/s2/s2/tempCarry<1>)
 LUT5:I3->O            3   0.124   0.550  s2/s2/s2/f4/cout1 (s2/s2/s2/tempCarry<3>)
 LUT5:I3->O            3   0.124   0.550  s2/s2/s2/f6/cout1 (s2/s2/s2/tempCarry<5>)
 LUT5:I3->O            1   0.124   0.399  s2/s2/s2/f8/h2/Mxor_sum_xo<0>1 (sum_63_OBUF)
 OBUF:I->O                 0.000          sum_63_OBUF (sum<63>)
----------------------------------------
Total                     22.343ns (3.969ns logic, 18.374ns route)
                                   (17.8% logic, 82.2% route)
```

2. 32 Bit Full Adder:

   Net delay: 11.559ns

   Logic Delay: 1.985ns

   Route Delay: 9.574ns

```
                          Gate     Net
Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
----------------------------------------  ------------
 IBUF:I->O             2   0.001   0.925  a_1_IBUF (a_1_IBUF)
 LUT5:I0->O            3   0.124   0.550  s1/s1/f2/cout1 (s1/s1/tempCarry<1>)
 LUT5:I3->O            3   0.124   0.550  s1/s1/f4/cout1 (s1/s1/tempCarry<3>)
 LUT5:I3->O            3   0.124   0.550  s1/s1/f6/cout1 (s1/s1/tempCarry<5>)
 LUT5:I3->O            3   0.124   0.550  s1/s1/f8/cout1 (s1/tempCarry)
 LUT5:I3->O            3   0.124   0.550  s1/s2/f2/cout1 (s1/s2/tempCarry<1>)
 LUT5:I3->O            3   0.124   0.550  s1/s2/f4/cout1 (s1/s2/tempCarry<3>)
 LUT5:I3->O            3   0.124   0.550  s1/s2/f6/cout1 (s1/s2/tempCarry<5>)
 LUT5:I3->O            3   0.124   0.550  s1/s2/f8/cout1 (tempCarry)
 LUT5:I3->O            3   0.124   0.550  s2/s1/f2/cout1 (s2/s1/tempCarry<1>)
 LUT5:I3->O            3   0.124   0.550  s2/s1/f4/cout1 (s2/s1/tempCarry<3>)
 LUT5:I3->O            3   0.124   0.550  s2/s1/f6/cout1 (s2/s1/tempCarry<5>)
 LUT5:I3->O            3   0.124   0.550  s2/s1/f8/cout1 (s2/tempCarry)
 LUT5:I3->O            3   0.124   0.550  s2/s2/f2/cout1 (s2/s2/tempCarry<1>)
 LUT5:I3->O            3   0.124   0.550  s2/s2/f4/cout1 (s2/s2/tempCarry<3>)
 LUT5:I3->O            3   0.124   0.550  s2/s2/f6/cout1 (s2/s2/tempCarry<5>)
 LUT5:I3->O            1   0.124   0.399  s2/s2/f8/h2/Mxor_sum_xo<0>1 (sum_31_OBUF)
 OBUF:I->O                 0.000          sum_31_OBUF (sum<31>)
----------------------------------------
Total                     11.559ns (1.985ns logic, 9.574ns route)
                                   (17.2% logic, 82.8% route)
```

3. 16 Bit Full Adder:

   Net Delay: 6.167ns

   Logic Delay: 0.993ns

   Route Delay: 5.174ns

```
                          Gate     Net
Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
----------------------------------------  ------------
 IBUF:I->O             2   0.001   0.925  a_1_IBUF (a_1_IBUF)
 LUT5:I0->O            3   0.124   0.550  s1/f2/cout1 (s1/tempCarry<1>)
 LUT5:I3->O            3   0.124   0.550  s1/f4/cout1 (s1/tempCarry<3>)
 LUT5:I3->O            3   0.124   0.550  s1/f6/cout1 (s1/tempCarry<5>)
 LUT5:I3->O            3   0.124   0.550  s1/f8/cout1 (tempCarry)
 LUT5:I3->O            3   0.124   0.550  s2/f2/cout1 (s2/tempCarry<1>)
 LUT5:I3->O            3   0.124   0.550  s2/f4/cout1 (s2/tempCarry<3>)
 LUT5:I3->O            3   0.124   0.550  s2/f6/cout1 (s2/tempCarry<5>)
 LUT5:I3->O            1   0.124   0.399  s2/f8/h2/Mxor_sum_xo<0>1 (sum_15_OBUF)
 OBUF:I->O                 0.000          sum_15_OBUF (sum<15>)
----------------------------------------
Total                      6.167ns (0.993ns logic, 5.174ns route)
                                   (16.1% logic, 83.9% route)
```

4. 8 Bit Full Adder:

   Net Delay: 3.471ns

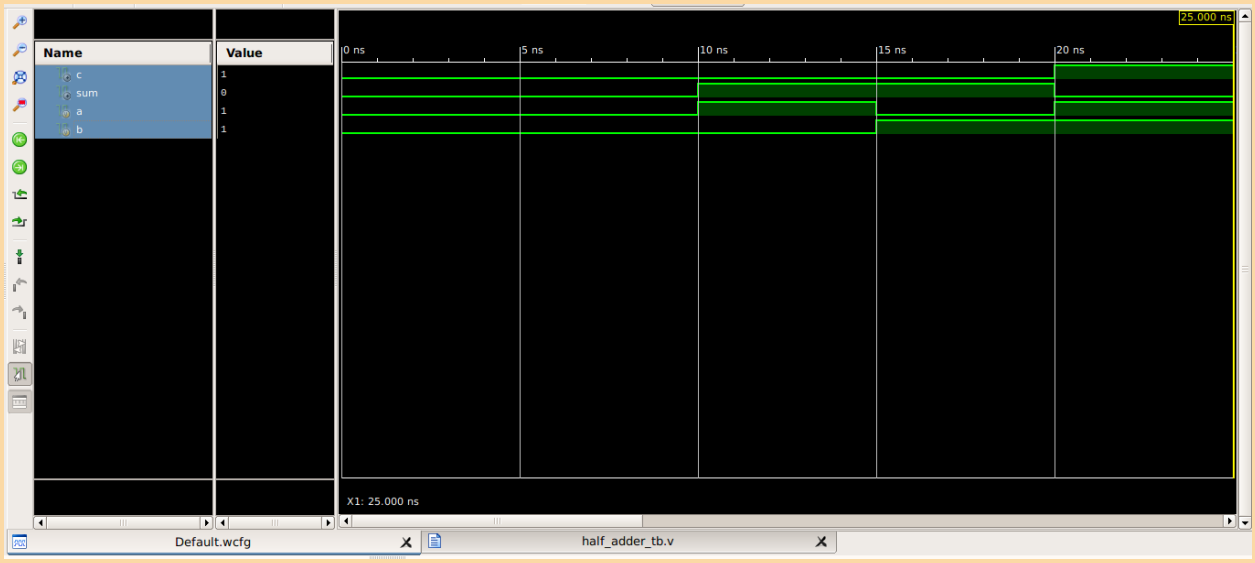
   Logic Delay: 0.497ns

   Route Delay: 2.974ns

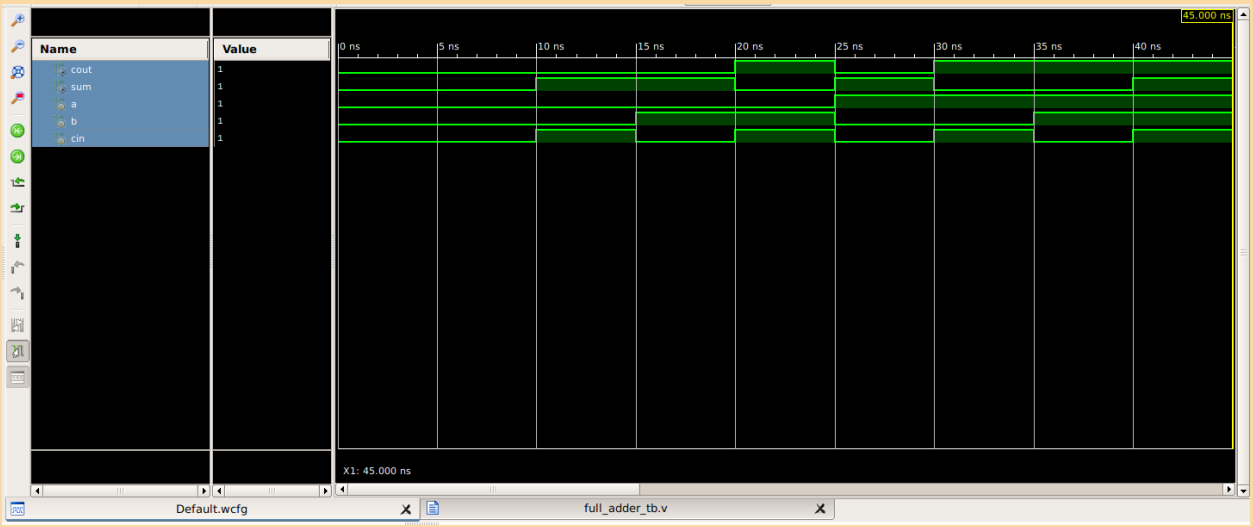
```
                              Gate     Net
Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
----------------------------------------  ------------
 IBUF:I->O             2   0.001   0.925  a_1_IBUF (a_1_IBUF)
 LUT5:I0->O            3   0.124   0.550  f2/cout1 (tempCarry<1>)
 LUT5:I3->O            3   0.124   0.550  f4/cout1 (tempCarry<3>)
 LUT5:I3->O            3   0.124   0.550  f6/cout1 (tempCarry<5>)
 LUT5:I3->O            1   0.124   0.399  f8/cout1 (cout_OBUF)
 OBUF:I->O                 0.000          cout_OBUF (cout)
----------------------------------------
Total                      3.471ns (0.497ns logic, 2.974ns route)
                                   (14.3% logic, 85.7% route)
```

Wave Outputs:

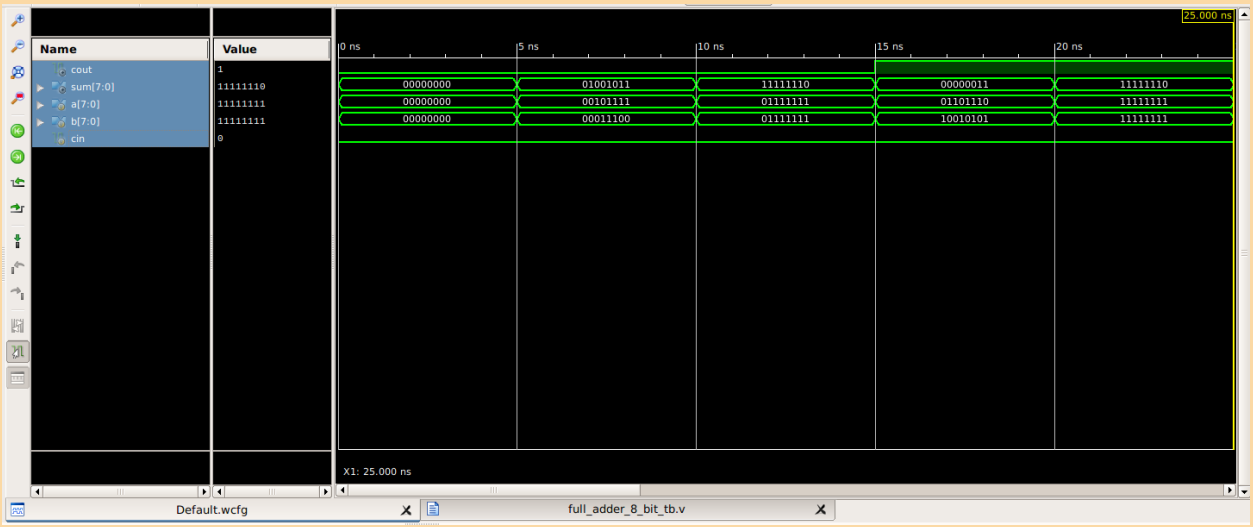
1. Half Adder:



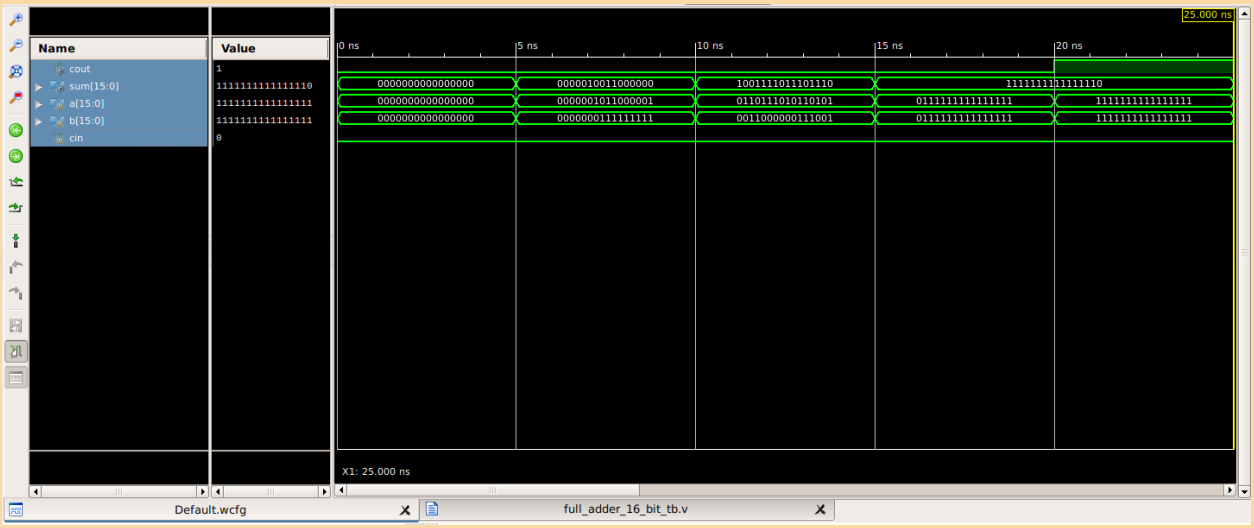
2. Full Adder:



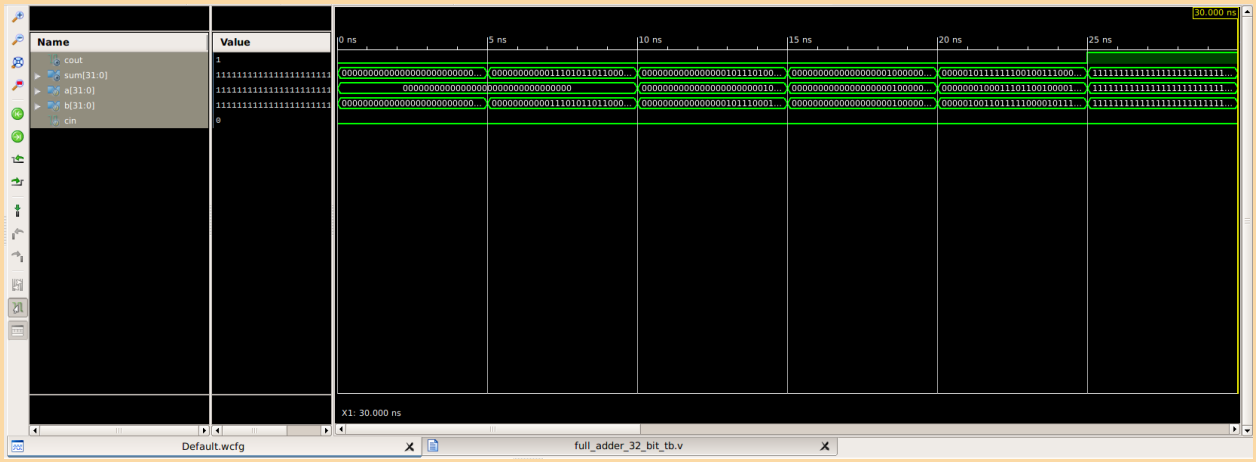
3. 8 bit Full Adder:



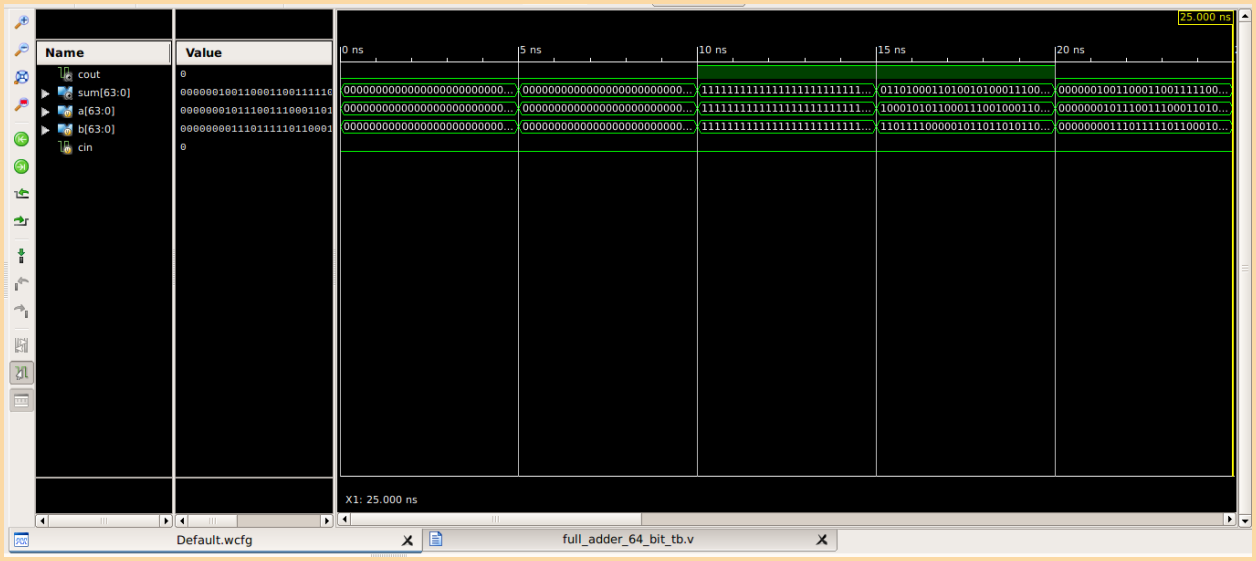
4. 16 bit Full Adder:



5. 32 bit Full Adder:



6. 64 bit Full Adder:



d). Difference between two n-bit numbers:

To calculate the difference between two numbers `a` and `b`, we can note that,

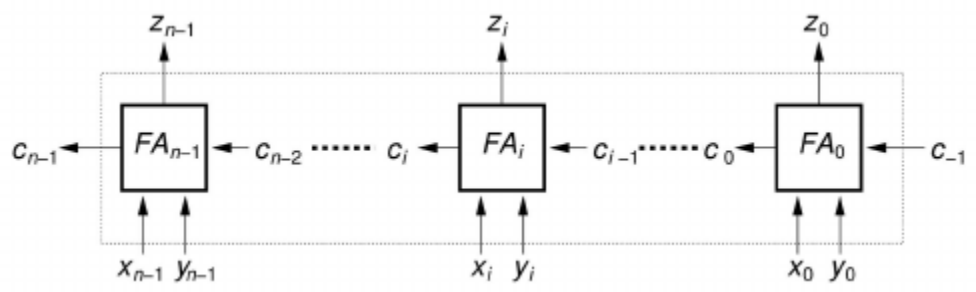
`a - b = a + (-b)`

Therefore, to perform a subtraction operation, we can add `a` with the 2's complement of `b`:

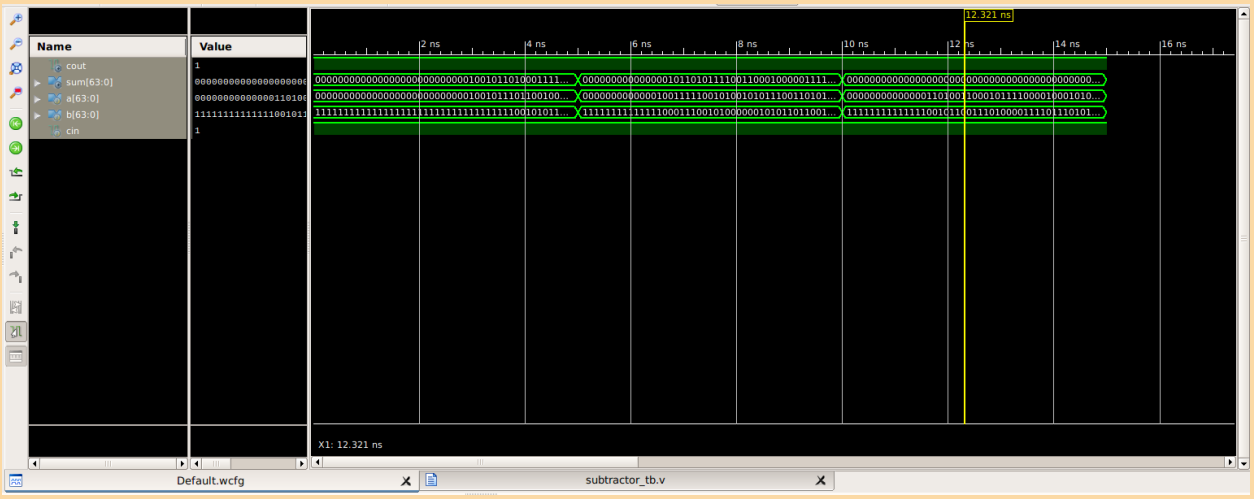
⇒ `a + (2's complement of b)`

= `a + (1's complement of b) + 1`

Therefore, a ripple carry adder can take `a`, `2's complement of b` as number inputs and `1 as the input carry` to calculate `a - b` i.e. the difference between two n-bit numbers.



Difference between two n-bit numbers using a ripple carry adder.




```
a =          81277482720, b =          446278127, carry_in = 1, carry_out = 1, a-b =          80831204593
a =  1400000000000000, b =  1000000000000000, carry_in = 1, carry_out = 1, a-b =  400000000000000
a =  928391830841483, b =  928391830841483, carry_in = 1, carry_out = 1, a-b =  0
```

Simulated output