KGP-RISC Instruction Format and Encoding

Register conventions

32 registers
All registers are 32-bit 2's complement, whereas addresses are unsigned in nature.

Register Number	Conventional Name	Usage
$0	$zero	Hard-wired to 0
$1	$pc	Program Counter stores the address of next instruction to be fetched
$2 - $3	$v0 - $v1	Return values from functions
$4 - $7	$a0 - $a3	Arguments to functions - not preserved by subprograms
$8	$ra	Return Address
$9 - $18	$t0 - $t9	Temporary data, not preserved by subprograms
$19, $20	$mfho, $mflo	Special registers used to store multiplication product. $19 stores most significant word and $20 stores least significant word. They can also be used for general purpose.
$21	$ir	Register to store the fetched instruction
$22	$fr	Flag register to store the value of flags. zero flag

		carry flag sign flag overflow flag
$23 - $31	$s0 - $s8	Saved registers, preserved by subprograms

NO register for named data like arrays

Instruction formats and encoding

R-format

Opcode	Rs (Source 1, Destination)	Rt (Source2)	Shift Amount	Function	Don't Care
6 bits	5 bits	5 bits	5 bits	6 bits	6 bits

Instruction	Opcode (6 bits)	Rs (5 bits)	Rt (5 bits)	Shift amount (5 bits)	Function (6 bits) [in decimal]
Add	000000	5 bit value	5 bit value	00000	0
Multiply (unsigned)	000000	5 bit value	5 bit value	00000	1
Multiply (signed)	000000	5 bit value	5 bit value	00000	2
Complement	000000	5 bit value	5 bit value	00000	3
and	000000	5 bit value	5 bit value	00000	4

xor	000000	5 bit value	5 bit value	00000	5
Shift left logical	000000	5 bit value	00000	5 bit value	6
Shift right logical	000000	5 bit value	00000	5 bit value	7
Shift left logical variable	000000	5 bit value	5 bit value	00000	8
Shift right logical variable	000000	5 bit value	5 bit value	00000	9
Shift right arithmetic	000000	5 bit value	00000	5 bit value	10
Shift right arithmetic variable	000000	5 bit value	5 bit value	5 bit value	11

I-format

Opcode	**Rs**	**Immediate**	**Function**	**Don't Care**
6 bits	5 bits	16 bits	2 bits	3 bits

Instruction	**Opcode (6 bits)**	**Rs (5 bits)**	**Immediate (16 bits)**	**Function (2 bits)**
Add immediate	000001	5 bit value	num	00
Complement immediate	000001	5 bit value	num	01

Memory

Opcode	Rs (Destination)	Rt (Source)	Offset Amount	Function
6 bits	5 bits	5 bits	14 bits	2 bits

Instruction	Opcode (6 bits)	Rs (5 bits)	Rt (5 bits)	Offset Amount	Function (2 bits)
Store word	000010	5 bit value	5 bit value	14 bit constant	00
Load Word	000010	5 bit value	5 bit value	14 bit constant	01

J-format

Opcode	Address	Function
6 bits	22 bits	4 bits

Instruction	Opcode (6 bits)	Address (22 bits)	Function (4 bits)
Call	000011	address	0000
Branch on No Overflow	000011	address	0001
Branch on Overflow	000011	address	0010
Branch on Not Sign	000011	address	0011
Branch on Sign	000011	address	0100

Branch on No Carry	000011	address	0101
Branch on Carry	000011	address	0110
Branch on not zero	000011	address	0111
Branch on zero	000011	address	1000
Unconditional branch	000011	address	1001
Return	000011	22 bit zero	1010
Branch Register	000011	5 bit register followed by 17'b0	1011