Pranav Dangi

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Education

- **National University of Singapore (NUS)** — Singapore
  PhD Student, School of Computing — 2024 - 2028
- **Birla Institute of Technology and Science, Pilani (BITS Pilani)** — Pilani, India
  B.E. Electrical and Electronics Engineering — 2019 - 2023
  Thesis: Addressing Sparsity through Algorithms, Memory and Compute

Publications (*equal contribution) (chronological order)

- **Pranav Dangi**, Bai Zhenyu, Rohan Juneja, Zhaoying Li, Tulika Mitra. "A Data-Driven Dynamic Execution Orchestration Architecture", **Under Review**
- Zhaoying Li*, **Pranav Dangi***, Chenyang Yin, Thilini Kaushalya Bandara, Rohan Juneja, Cheng Tan, Tulika Mitra. "Enhancing CGRA Efficiency through Aligned Compute and Communication Provisioning", **ASPLOS'25**
- **Pranav Dangi***, Thilini Kaushalya Bandara*, Saeideh Sheikhpour, Tulika Mitra, Lieven Eeckhout. "Sustainable Hardware Specialization", **ICCAD'24**
- **Pranav Dangi**, Bai Zhenyu, Rohan Juneja, Dhananjaya Wijerathne, Tulika Mitra. "A Generalized Accelerator for Variably Sparse Matrix Computations in ML", **PACT'24**
- Bai Zhenyu, Wu Dan, **Pranav Dangi**, Dhananjaya Wijerathne, Pavan Miriyala, Tulika Mitra. "Irregular Data-aware dynamic scheduling of workloads on heterogeneous systems", **Under Review**
- Bai Zhenyu, **Pranav Dangi**, Huize Li, Tulika Mitra. "Scalable, Efficient Window-Attention Based Transformer Acceleration", **DAC'24**

Grants, Scholarships and Achievements

- Singapore President's Graduate Fellowship (Highest Fellowship for Academic and Research Achievements)
- NUS Research Incentive Award (Award for Outstanding Research Potential)
- Travel Grant: ASPLOS 2025, DAC 2024
- BITS IPCD Undergraduate Thesis Award (Award for Outstanding Undergraduate Research)
- Google Summer of Code Fellowship, 2021
- BITS Institute Dean's MCN Scholarship, 2019-20, 2021-23 (Top 5% of the Department)

Research Experience

- **National University of Singapore (NUS) Computing** — Singapore
  Research Assistant — Jan 2023 - Aug 2024
  - A distributed memory architecture & compiler with support for dynamically orchestrated instruction execution
  - Tapeout of a 12nm ultra-low power novel reconfigurable fabric (work in progress)
  - Architectural considerations for sustainability through the use of reconfigurable logic
  - Analytical modeling and automatic hardware development for dense and sparse tensor computation algorithms.
  - Energy efficient algorithms, architectures, and pre-fetching techniques for sparse matrix computations.
  - Compiling, Mapping to physical hardware and data placement for CGRAs.
  - **With AMD Research**: Design space exploration and an input-aware predictive framework for scheduling irregular workloads on a scale-out heterogeneous cluster of CPUs, GPUs, and FPGAs.
- **TCS Research and Innovation Labs** — Mumbai/Remote
  Research Intern — Aug 2022 - Dec 2022
  - Performance modeling and profile-guided design of a heterogeneous architecture for a session-based recommendation system on a custom setup and AWS F1 cloud FPGAs.
- **Oysters Lab, EEE Department** — BITS Pilani
  Research Assistant — Jan 2022 - Nov 2022
  - Power-performance characterization and Pareto-optimal design for neural networks under hardware resource constraints.
  - Characterizing HLS frameworks against custom RTL implementations.
  - Better number systems, precision, and approximations in computing for Machine Learning applications.

Industry & Open-Source Experience

- **Intel** — Bangalore
  Intern — Jun 2022 - Aug 2022
  - Worked with the IP group for the verification of the interconnects for Intel XEON

- **Google Summer of Code - RTEMS** — Remote
  Fellow — May 2021 - Aug 2021
  - Worked in the Raspberry Pi BSP group for the Real-Time Executive for Multiprocessor Systems, extending support for UART, GPIO, I2C, SPI peripherals, and symmetric multiprocessing.

- **Nihon Communications** — Remote
  Intern — May 2020 - July 2020
  - Implemented and interfaced SDR with the Linux network stack and LiquidSDR.

Skills Summary

- **Languages**: C, C++, System Verilog, Python, Chisel
- **Tools/Tech**: Synopsys/Cadence toolchains, LTSpice, gem5, MATLAB, Vivado/Vitis HLS, KiCAD, Yosys, LLVM
- **Courses**: **Analog and Digital VLSI Design, Computer Architecture, Analog Electronics**, Discrete Math, Communication Systems, Power Electronics, Operating Systems

Projects

- **Adversarial Debiasing**: Leveraged Adversarial Debiasing to enhance an ML model's fairness with respect to caste and gender in the Indian context
- **RISC Processor**: Designed and tested a 16 Bit Multicycle RISC Processor with 21 custom instructions
- **Performance Evaluation of Branch Predictors**: Analyzed various branch predictors using the gem5 simulator
- **Floating Point Unit**: Designed and tested a half-precision (16 bit) IEEE 754 compliant floating point unit to be robust along with all exceptions as per the specifications
- **Card Game**: Built the functioning of an open-source card game named Bluff

Extra Curriculars

- **Teaching Assistant** — Singapore
  GEI1000 Computational Thinking — Sept 2024 – Dec 2024
  - Taught algorithmic intuition and explored the need (or lack thereof) for computers to Business, Music, Social Sciences, and Arts majors.

- **Undergraduate Teaching Assistant** — Pilani, India
  CS F342 Computer Architecture, EEE F313 Analog, Digital VLSI Design — Jan 2022 – Dec 2022
  - Conducted Labs for Processor Design and Spice Simulations

- **StuCCAn (Head of Cultural Fest)** — Pilani, India
  Department of Controls — August 2022 – December 2022
  - Supervised quizzing, music and literary competitions. Organized Jazz and Rock concerts.