Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Name: Pranav R. Hegde	SRN: PES1UG19CS343	Section: F

Date:09/04/2021

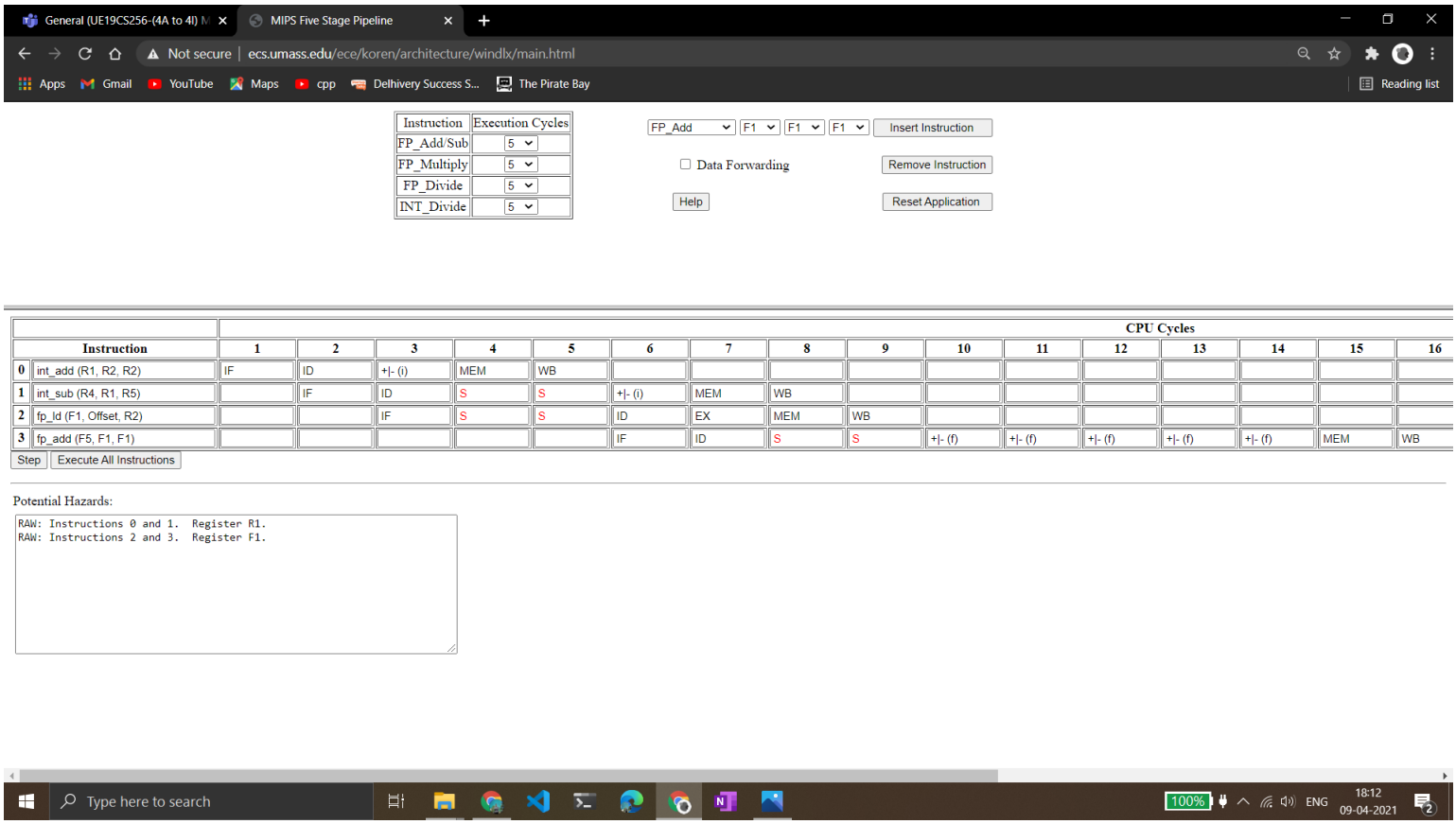
Week#____9_____Program Number: ____1___

Title of the Program:

5 Stage MIPS pipelined simulator

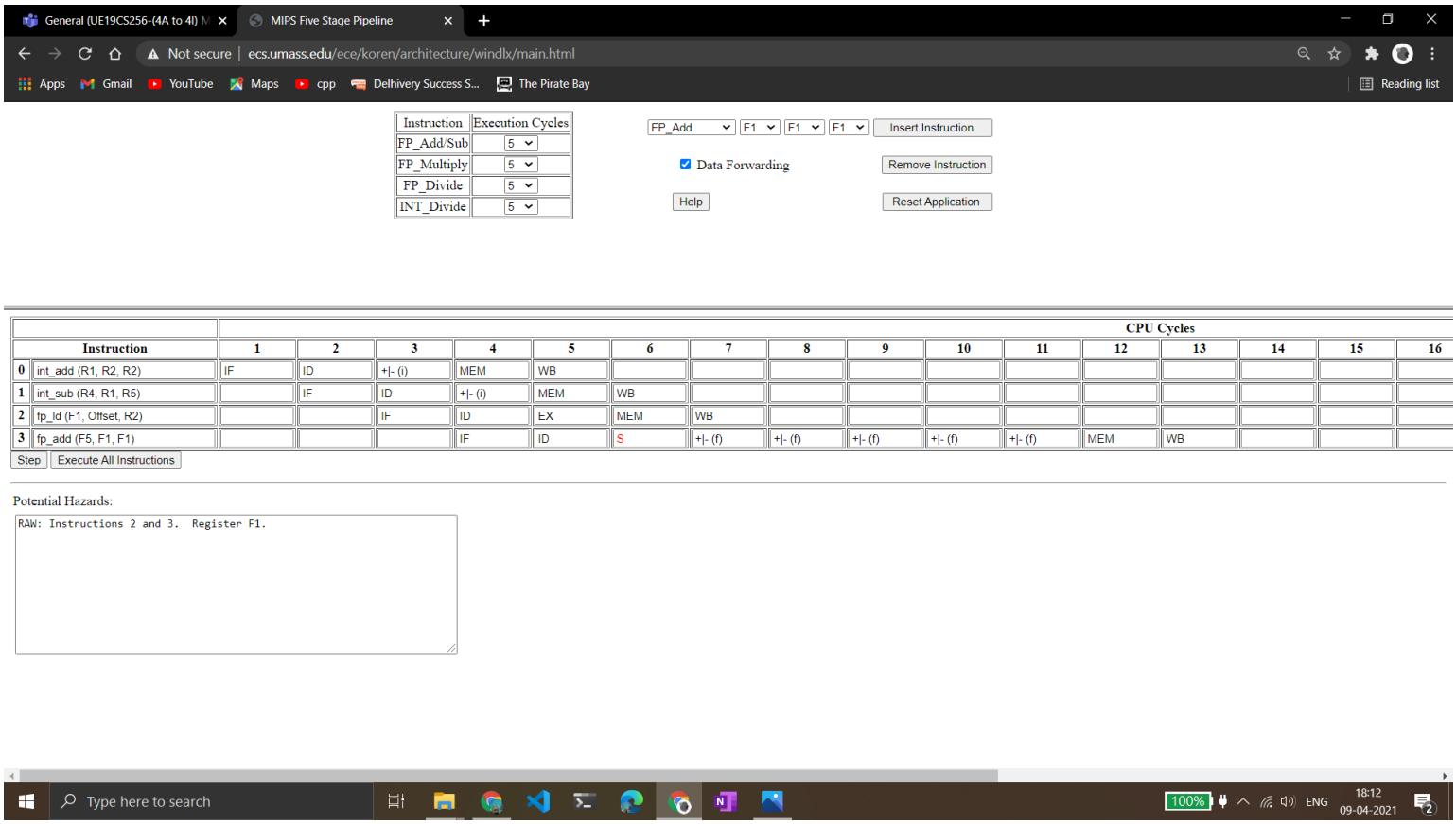
Observations:

Without data forwarding



- Yes, there is a data dependency between the instructions.
- The number of stalls introduced in the case without data forwarding are 6.
- And the number of clock cycles consumed are 16.

With data forwarding:



- In case of data forwarding, only 1 stall is introduced.
- And the number of clock cycles consumed are 13.

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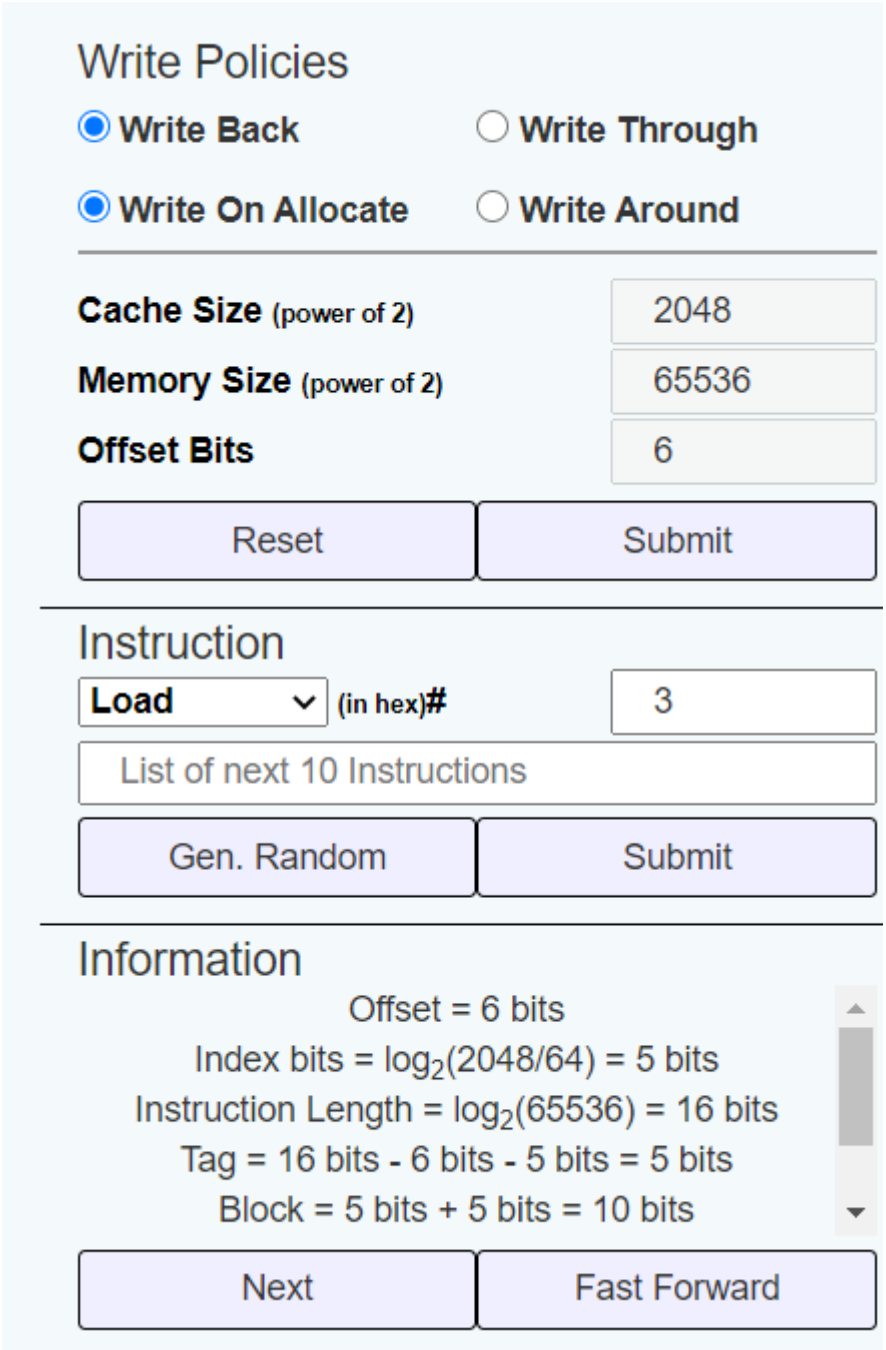
Week#____9_____Program Number: ____2___

Title of the Program:

Cache simulator

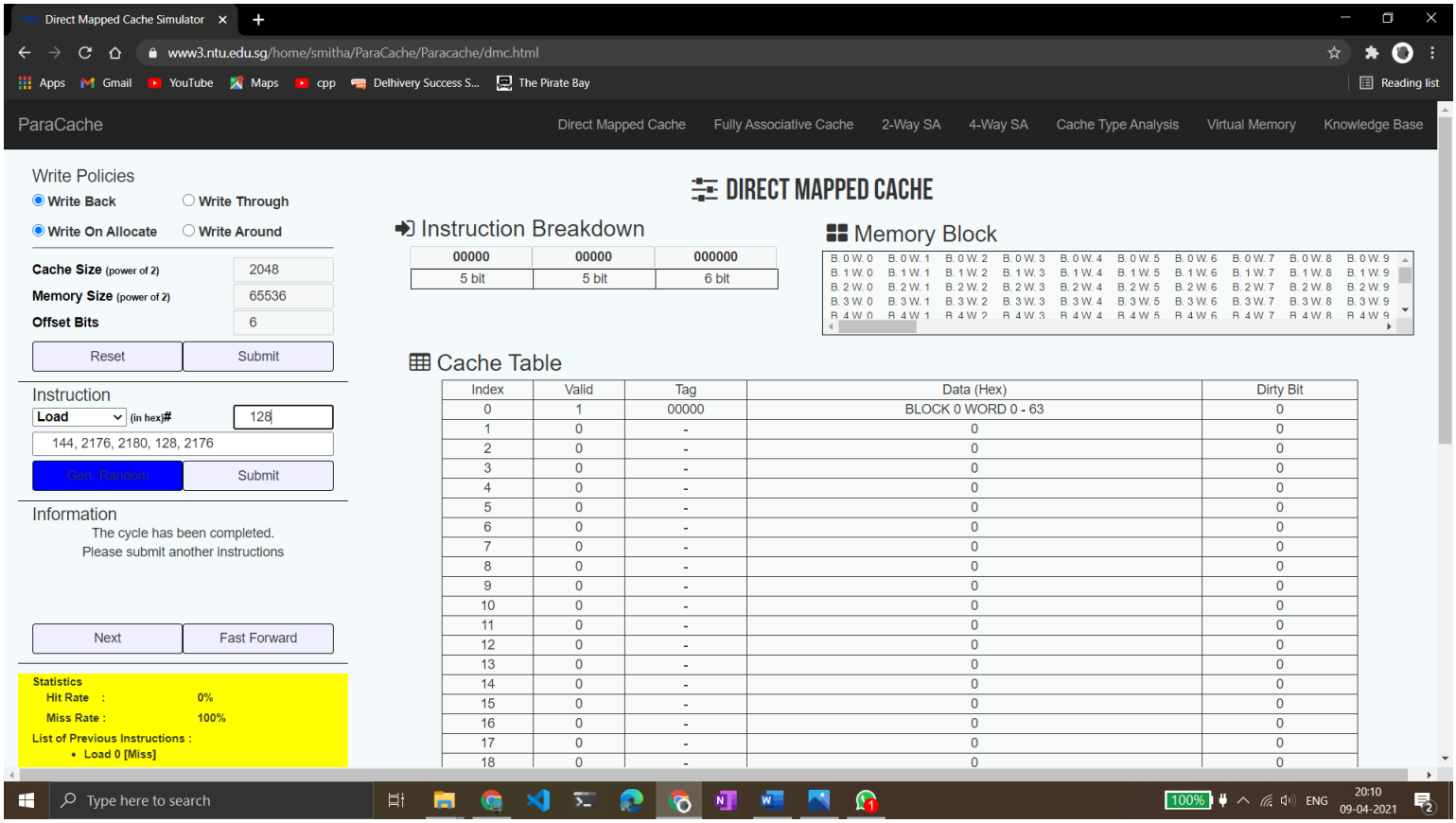
Part 1 – Direct mapping:



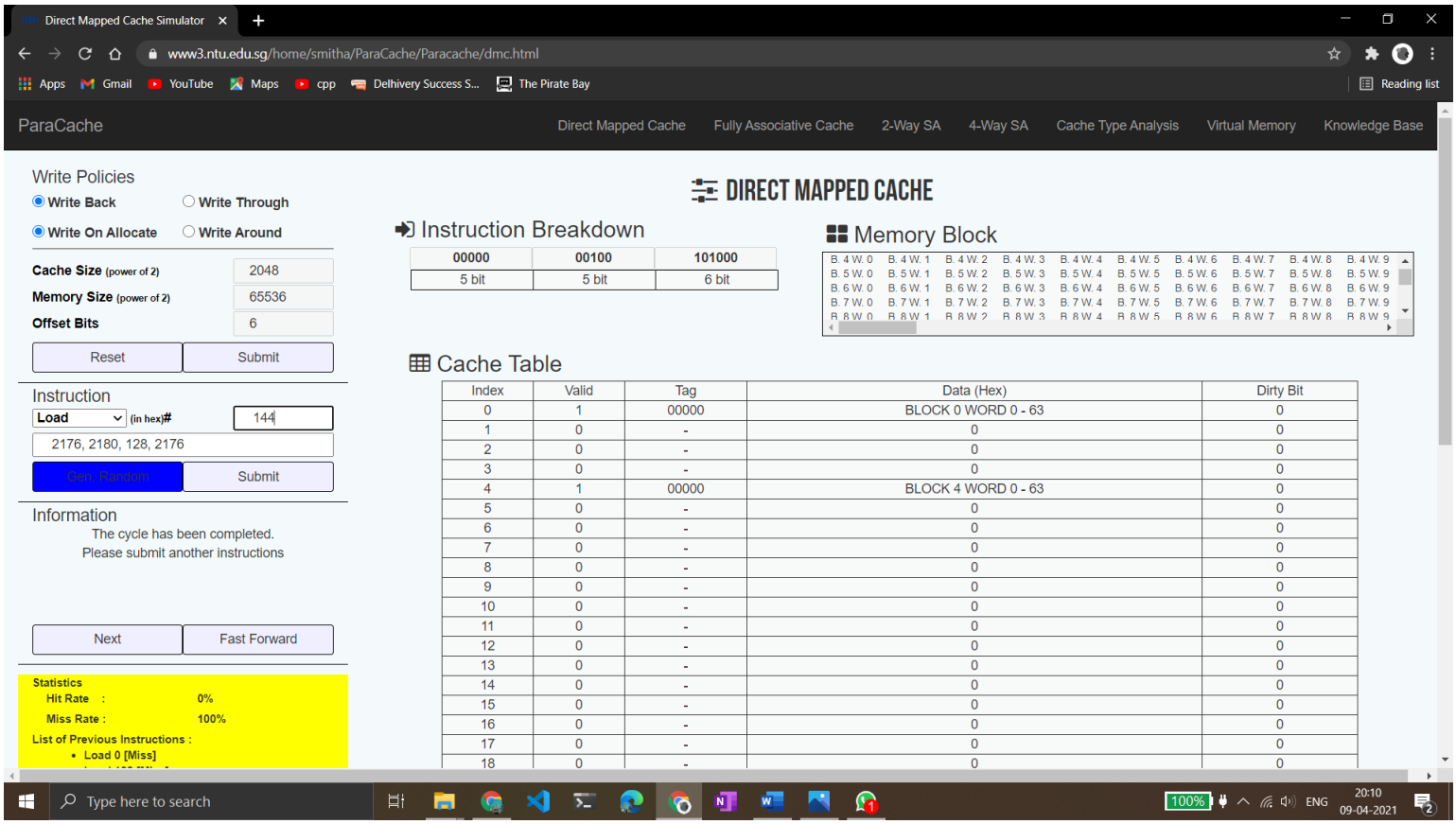
Based on the info given:

- Index bits: 5
- Tag bits: 5
- Block bits: 10

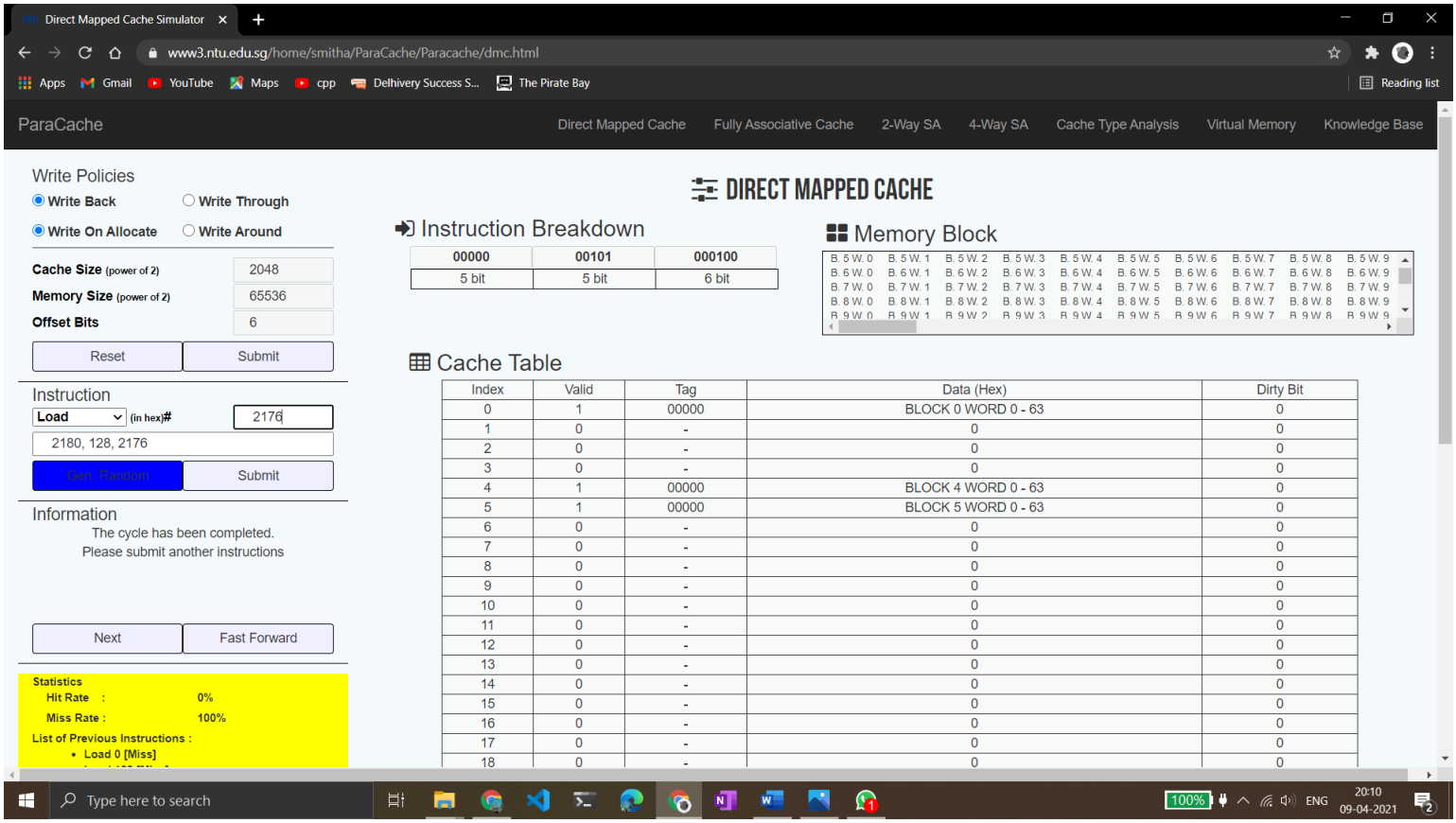
128 - Miss



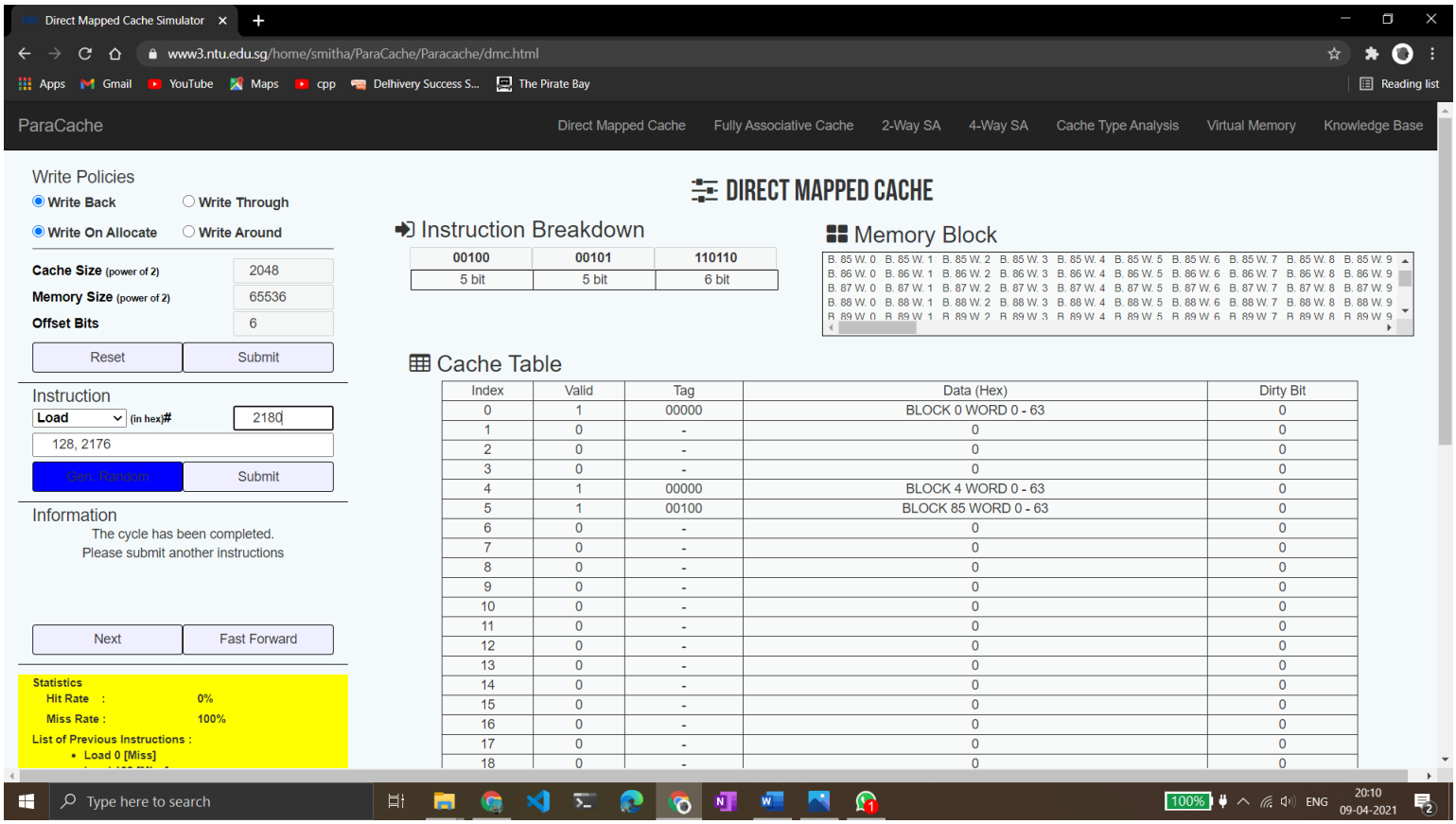
144 - Miss



2176 - Miss


Direct Mapped Cache Simulator
www3.ntu.edu.sg/home/smitha/ParaCache/Paracache/dmc.html
Apps Gmail YouTube Maps cpp Delhivery Success S... The Pirate Bay Reading list
ParaCache
Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base
Write Policies
Write Back Write Through
Write On Allocate Write Around
Cache Size (power of 2) 2048
Memory Size (power of 2) 65536
Offset Bits 6
Reset Submit
Instruction
Load (in hex)# 2176
2180, 128, 2176
Gen. Random Submit
Information
The cycle has been completed.
Please submit another instructions
Next Fast Forward
Statistics
Hit Rate : 0%
Miss Rate : 100%
List of Previous Instructions :
Load 0 [Miss]
DIRECT MAPPED CACHE
Instruction Breakdown
00000 00101 000100
5 bit 5 bit 6 bit
Memory Block
Cache Table
Index Valid Tag Data (Hex) Dirty Bit
0 1 00000 BLOCK 0 WORD 0 - 63 0
1 0 - 0 0
2 0 - 0 0
3 0 - 0 0
4 1 00000 BLOCK 4 WORD 0 - 63 0
5 1 00000 BLOCK 5 WORD 0 - 63 0
6 0 - 0 0
7 0 - 0 0
8 0 - 0 0
9 0 - 0 0
10 0 - 0 0
11 0 - 0 0
12 0 - 0 0
13 0 - 0 0
14 0 - 0 0
15 0 - 0 0
16 0 - 0 0
17 0 - 0 0
18 0 - 0 0
Type here to search
100% ENG 20:10 09-04-2021

2180 - Miss


Direct Mapped Cache Simulator
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List of Previous Instructions :
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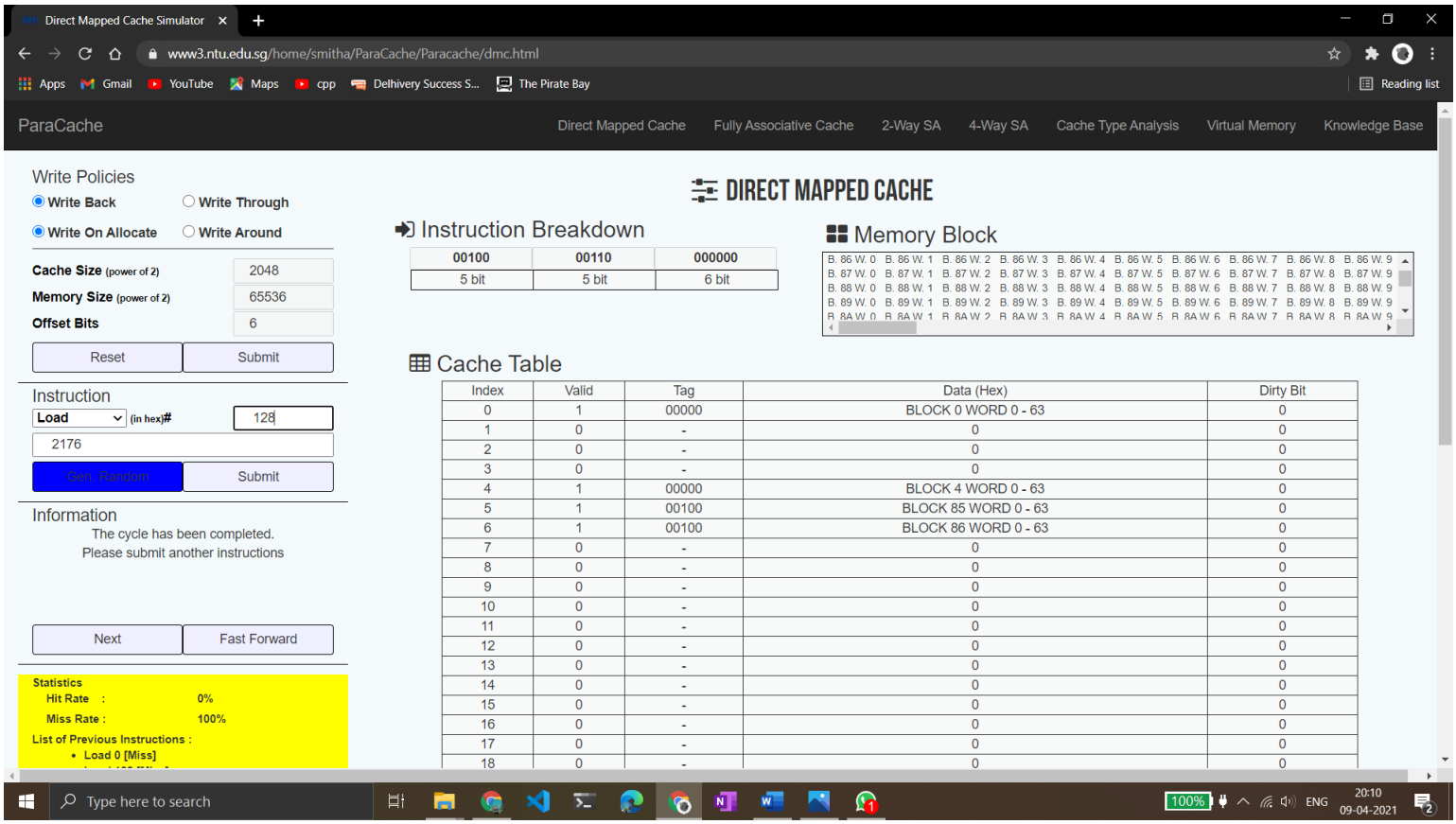
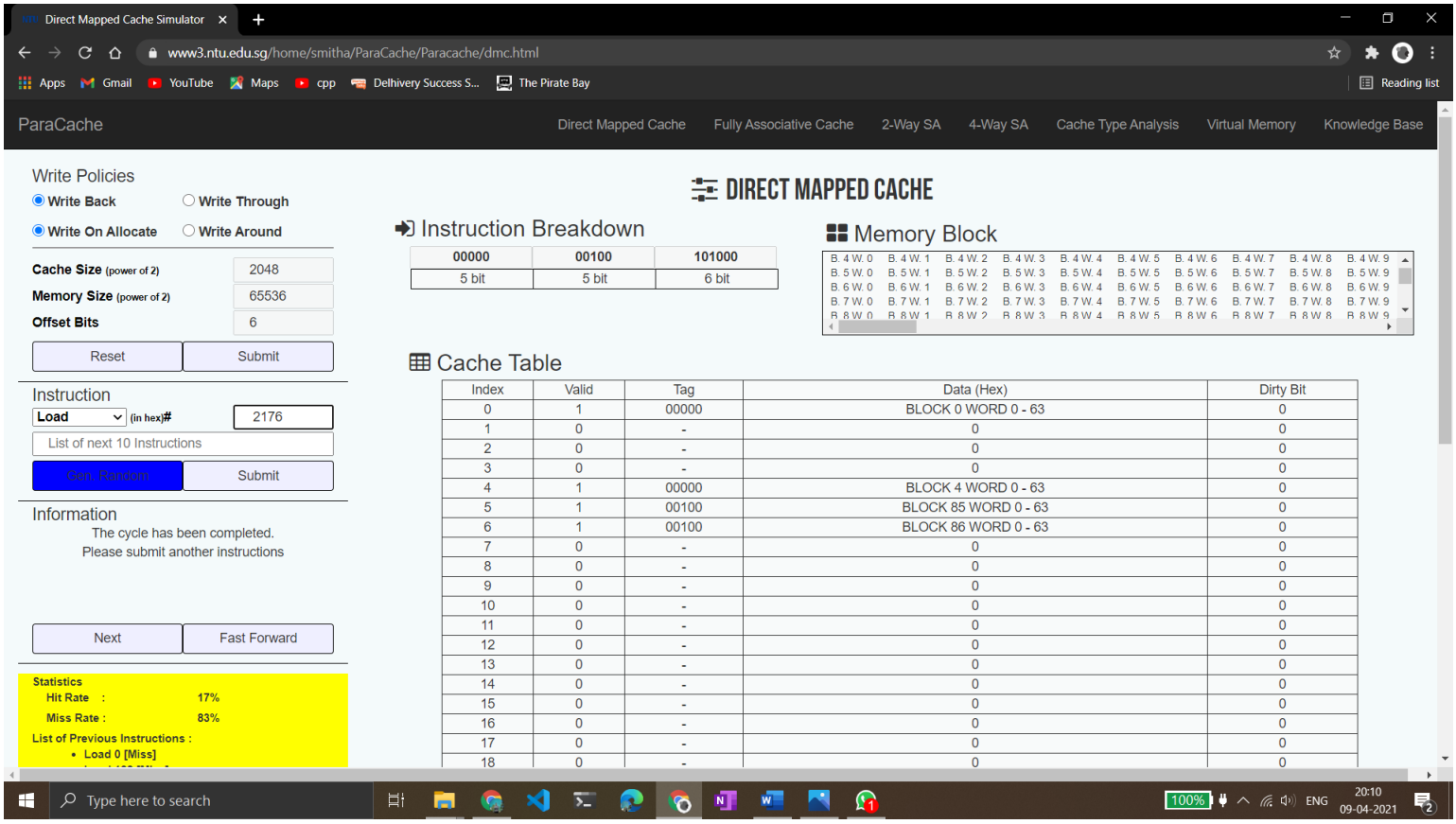
Instruction Breakdown
00100 00101 110110
5 bit 5 bit 6 bit
Memory Block
Cache Table
Index Valid Tag Data (Hex) Dirty Bit
0 1 00000 BLOCK 0 WORD 0 - 63 0
1 0 - 0 0
2 0 - 0 0
3 0 - 0 0
4 1 00000 BLOCK 4 WORD 0 - 63 0
5 1 00100 BLOCK 85 WORD 0 - 63 0
6 0 - 0 0
7 0 - 0 0
8 0 - 0 0
9 0 - 0 0
10 0 - 0 0
11 0 - 0 0
12 0 - 0 0
13 0 - 0 0
14 0 - 0 0
15 0 - 0 0
16 0 - 0 0
17 0 - 0 0
18 0 - 0 0
Type here to search
100% ENG 20:10 09-04-2021

128 - Hit



2176 – Hit



Final Hit and Miss rates:

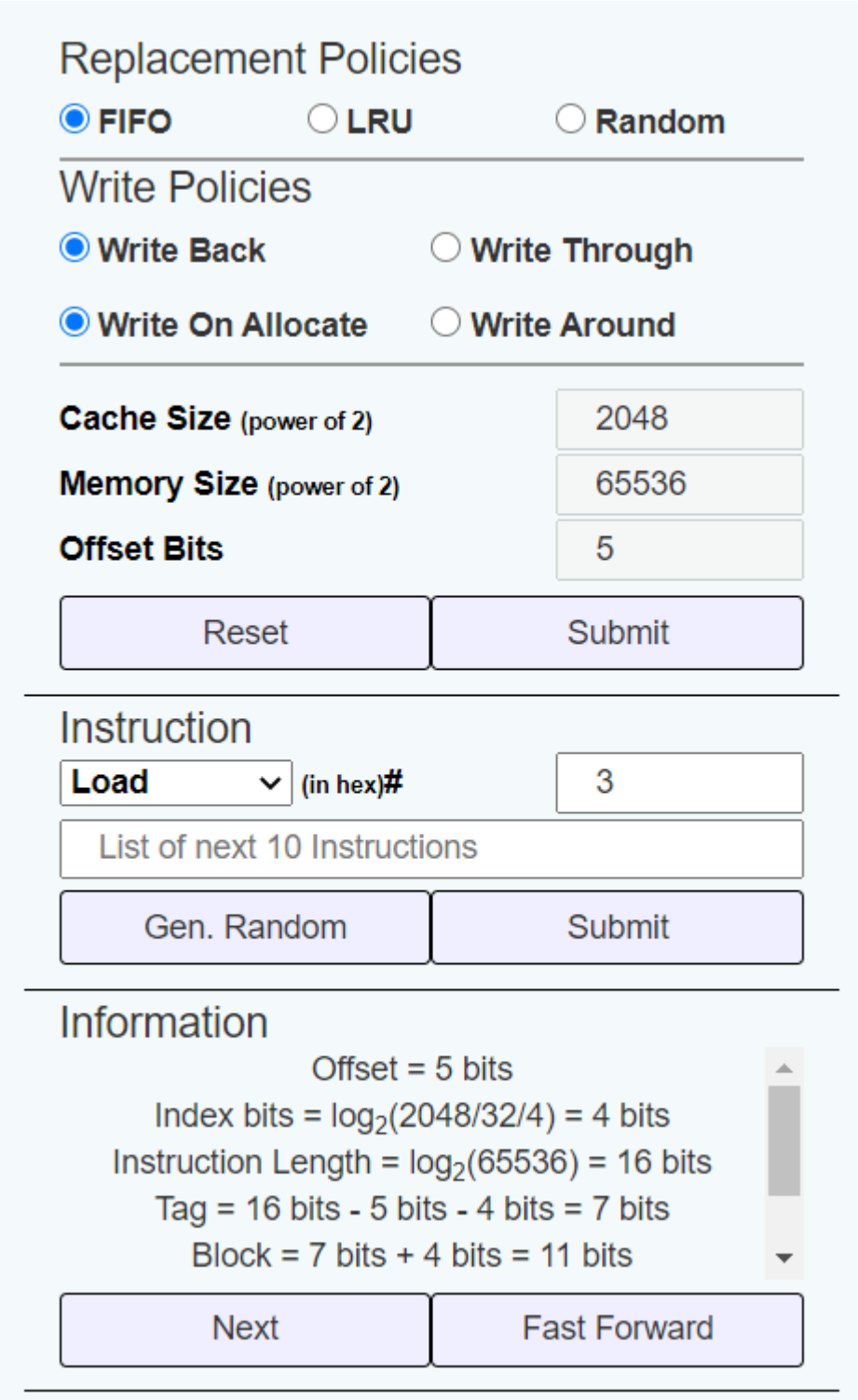
Statistics	
Hit Rate :	29%
Miss Rate :	71%

Total:

Hits: 2

Misses: 4

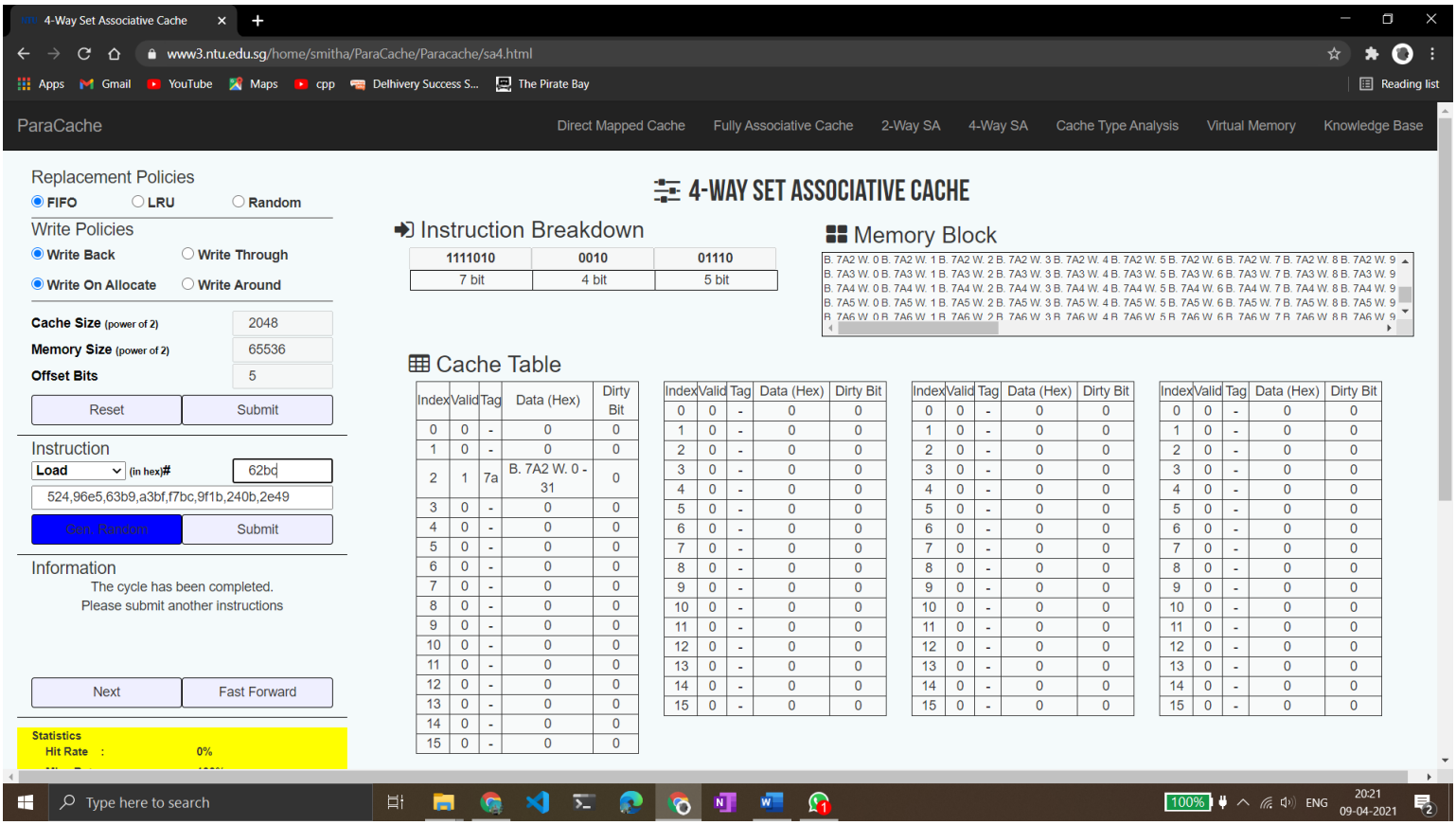
Part 2: 4 way set associative mapping



Observations based on given info:

- Index bits: 4
- Tag bits: 7
- Block bits: 11

Generated a random set of numbers:



All the numbers lead to misses.

Final statistics:

Misses = 10

Hits = 0

Statistics

Hit Rate : 0%

Miss Rate : 100%

List of Previous Instructions :

- **Load F44E [Miss]**
- **Load 62BC [Miss]**
- **Load 524 [Miss]**
- **Load 96E5 [Miss]**
- **Load 63B9 [Miss]**
- **Load A3BF [Miss]**
- **Load F7BC [Miss]**
- **Load 9F1B [Miss]**
- **Load 240B [Miss]**
- **Load 2E49 [Miss]**

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Date:09/04/2021

Week#____9_____Program Number: ____3___

Title of the Program:

Write the equivalent ARM assembly instructions for the given C code

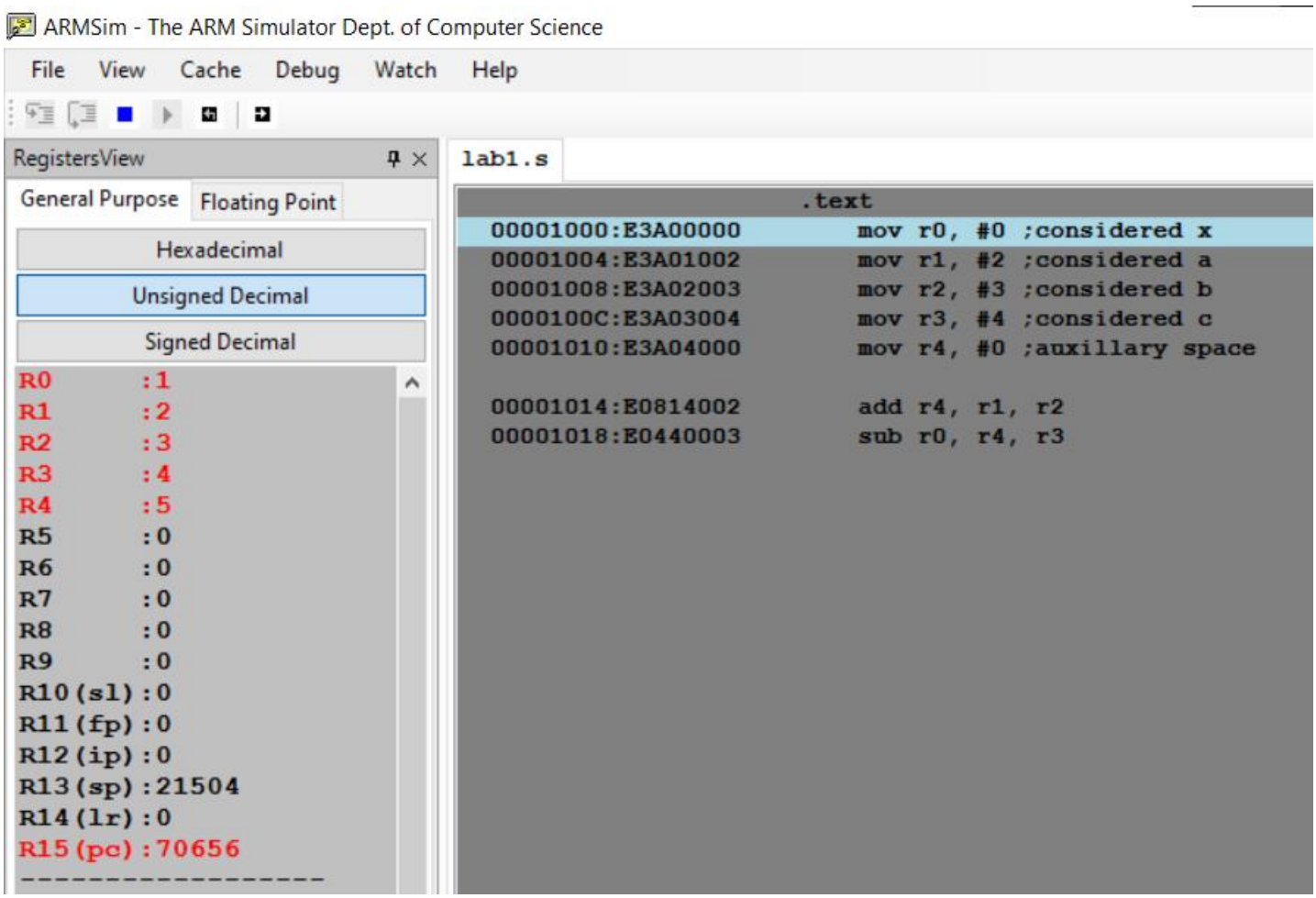
Part A - x = (a + b) – c:

The code:

```
.text
    mov r0, #0 ;considered x
    mov r1, #2 ;considered a
    mov r2, #3 ;considered b
    mov r3, #4 ;considered c
    mov r4, #0 ;auxillary space

    add r4, r1, r2
    sub r0, r4, r3
```

The arm sim executed screenshot:



Part B - $z = (a << 2) \mid (b \,\&\, 15)$:

The code:

```
.text
    mov r0, #0 ;considered z
    mov r1, #2 ;considered a
    mov r2, #3 ;considered b

    mov r3, #4 ;auxillary space 1
    mov r4, #0 ;auxillary space 2

    and r3, r2, #15
    mov r4, r1, LSL #2
    orr r0, r3, r4
```

The arm sim executed screenshot: