

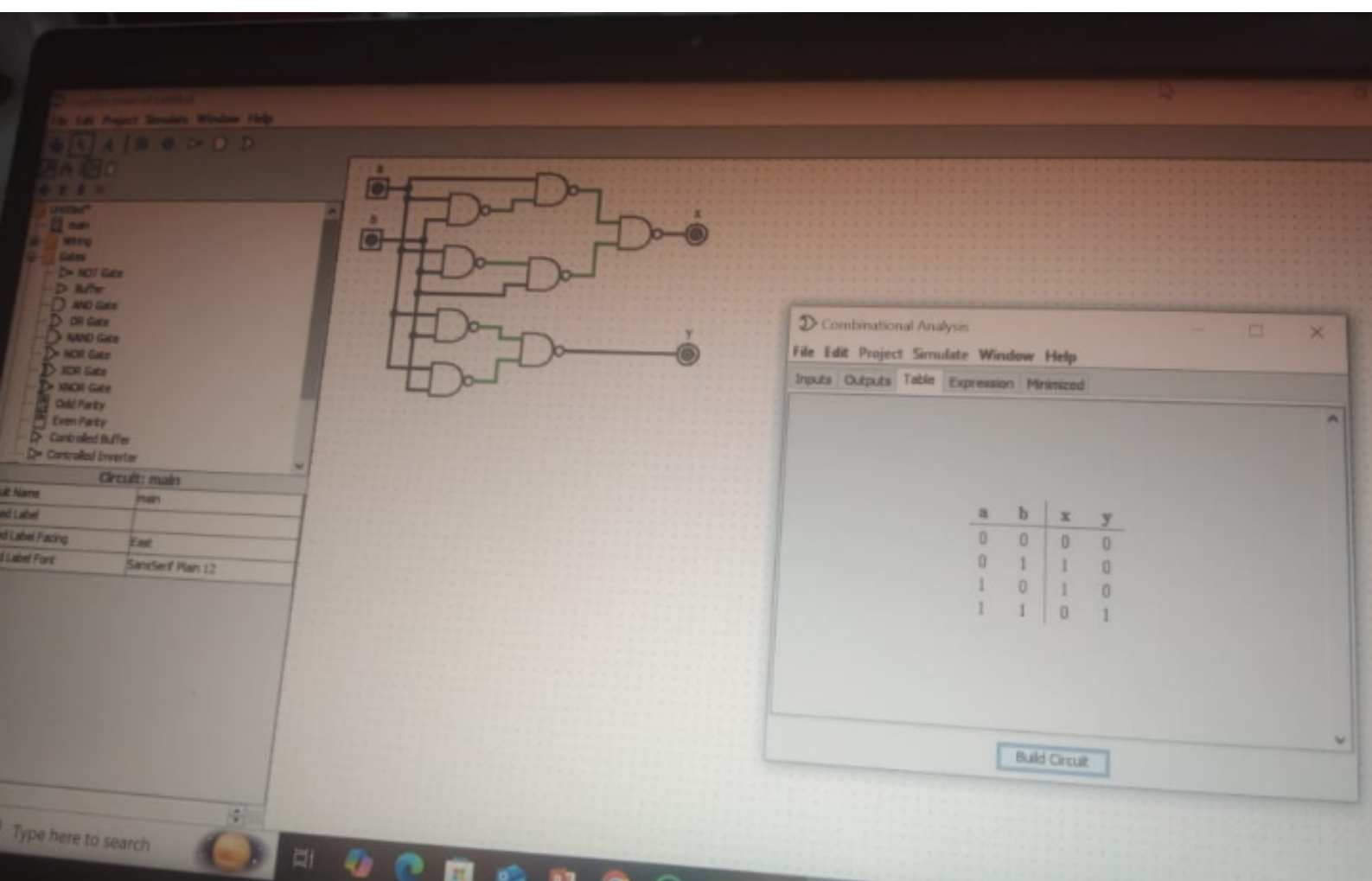
Start 8050

OK

Address (Hex)	Address	Data
1F72	8050	1
1F73	8051	2
1F74	8052	3
1F75	8053	0
1F76	8054	0
1F77	8055	0
1F78	8056	0
1F79	8057	0
1F7A	8058	0
1F7B	8059	0
1F7C	8060	0
1F7D	8061	0
1F7E	8062	0
1F7F	8063	0

Line No Assembler Message

0 Program assembled successfully



winutils - assembler and microprocessor emulator 4.08

file edit bookmarks assembler emulator math ascii codes help

new open examples save compile emulate calculator convertor options

```
01 MOV AX, [1100h]
02 MOV BX, [1102h]
03 ADD AX, BX
```

emulator: noname.bin

file math debug view external virtual devices virtual drive help

Load reload step back single step run step delay ms: 0

registers

	H	L
AX	00	7A
BX	00	67
CX	00	00
DX	00	00
CS	0100	
IP	000C	
SS	0100	
SP	FFFE	
BP	0000	
SI	0000	
DI	0000	
DS	0100	
ES	0100	

0100:0003

01000: A1 161 f
01001: 00 000 NULL
01002: 11 017 <
01003: 8B 139 f
01004: 1E 030 >
01005: 02 002 0
01006: 11 017 <
01007: 03 003 v
01008: C3 195 }
01009: A3 163 u
0100A: 00 000 NULL
0100B: 12 018 z
0100C: F4 244 f
0100D: 90 144 E
0100E: 90 144 E
0100F: 90 144 E
01010: 90 144 E
01011: 90 144 E
01012: 90 144 E
01013: 90 144 E
01014: 90 144 E
01015: 90 144 E

0100:0003

```
MOV BX, [01102h]
ADD AX, BX
MOV [01200h], AX
HLT
NOP
```

original source co...

```
01 MOV AX, [1100h]
02 MOV BX, [1102h]
03 ADD AX, BX
04 MOV [1200h], AX
05 HLT
06
07
08
```

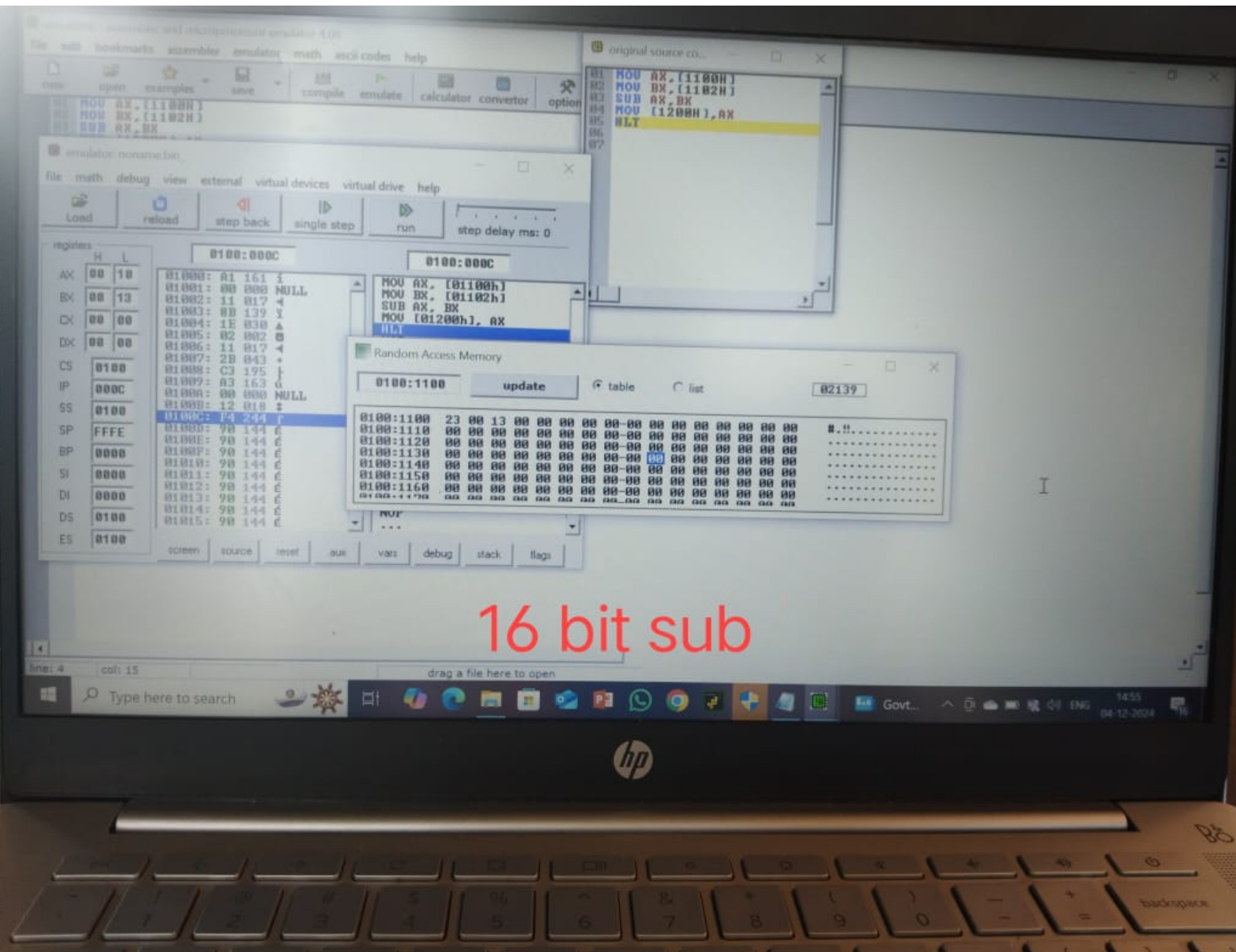
Random Access Memory

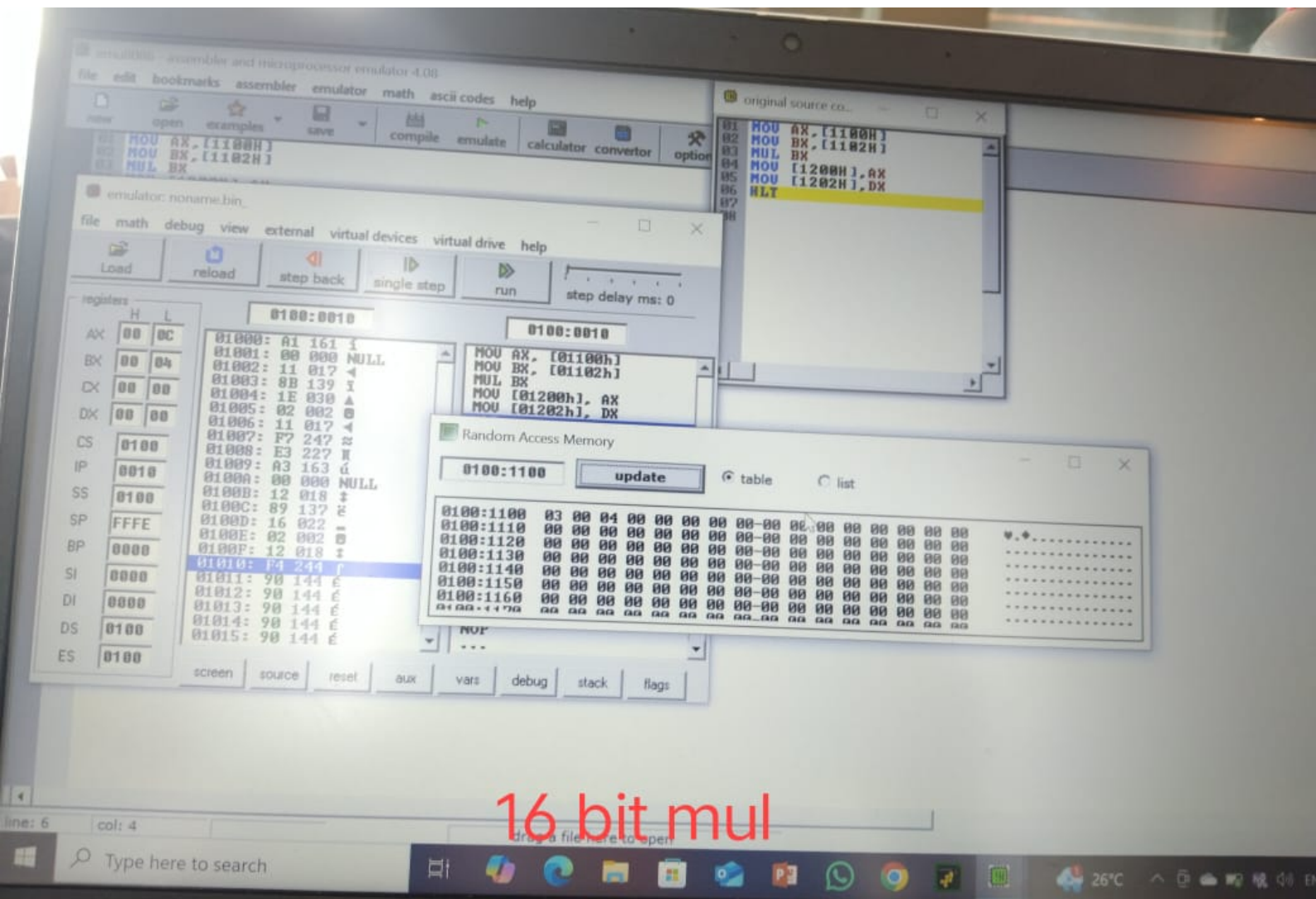
0100:1100 update table list

0100:1100	13 00 67 00 00 00 00 00 00 00 00 00 00 00 00 00	!!g.....
0100:1110	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0100:1120	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0100:1130	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0100:1140	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0100:1150	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0100:1160	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

16 bit add







16 bit mul

Logisim main of Untitled 2

File Edit Project Simulate Window Help

Combinational Analysis

File Edit Project Simulate Window Help

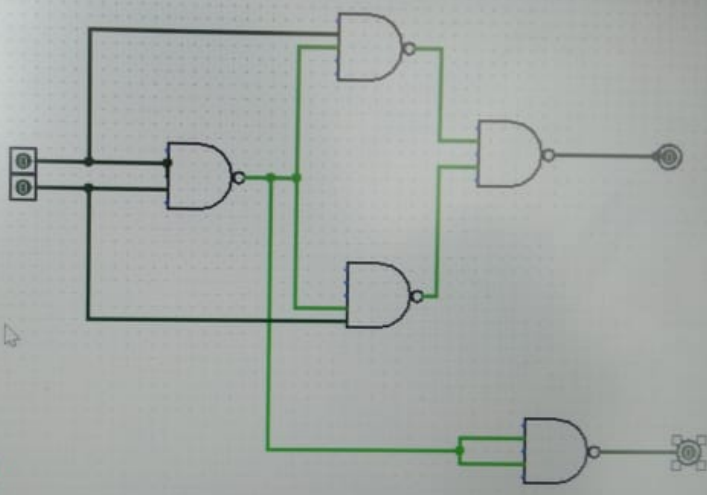
Inputs Outputs Table Expression Minimized

a	b	x	y
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Build Circuit

Facing: West
Output?: Yes
Data Bits: 1
Three-state?: Yes
Pull Behavior: Unchanged
Label:
Label Location: East
Label Font: SansSerif Plain 12

2 bit half adder



File Edit Project Simulate Window Help

Combinational Analysis

File Edit Project Simulate Window Help

Inputs Outputs Table Expression Minimized

a	b	x	y
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

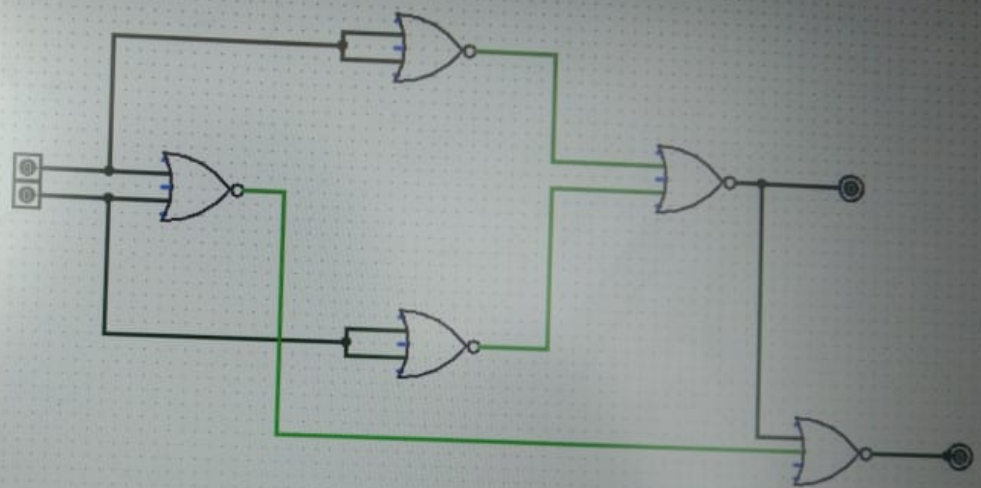
Build Circuit

Circuit Name: main

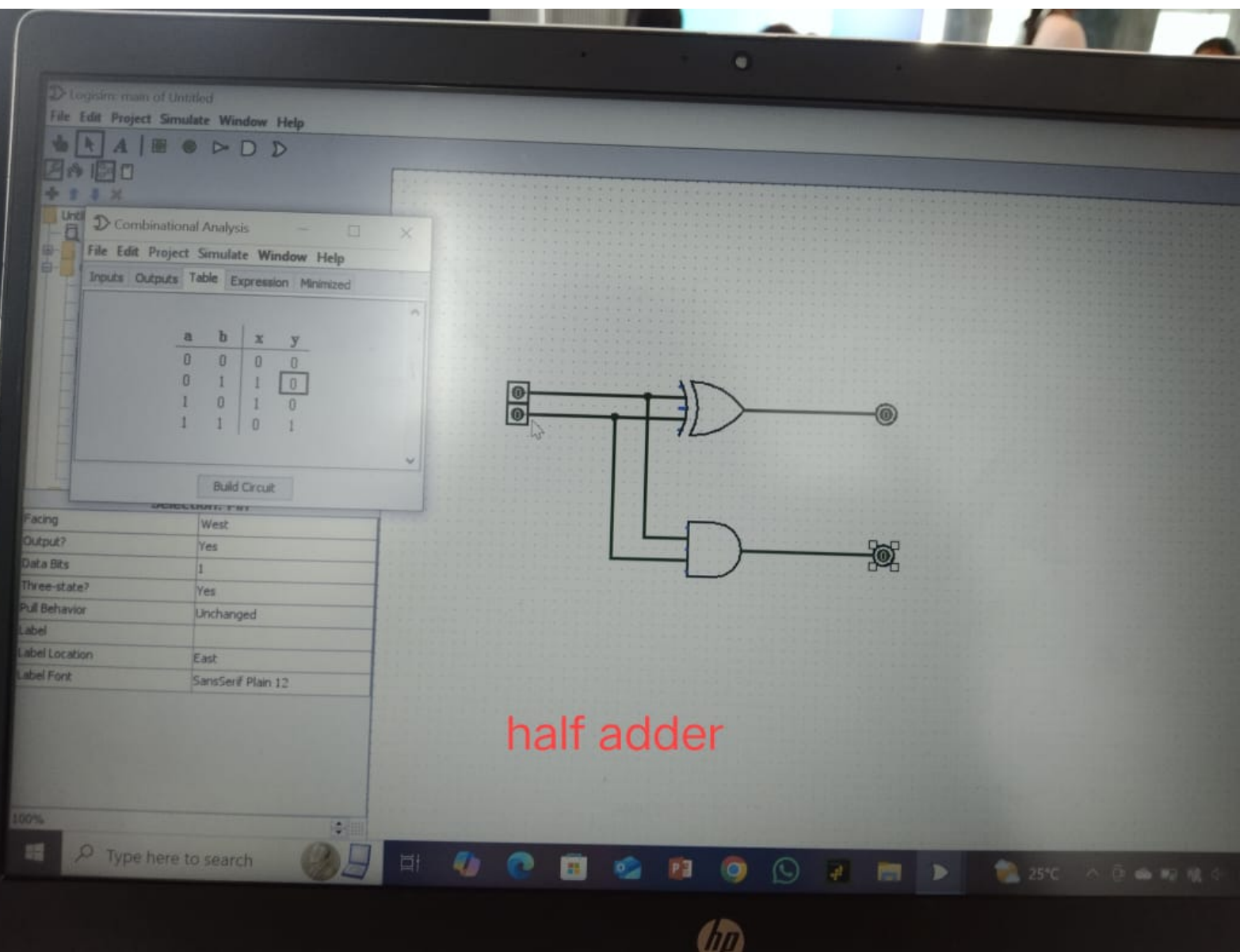
Shared Label

Shared Label Facing: East

Shared Label Font: SansSerif Plain 12



2 bit half
adder



half adder